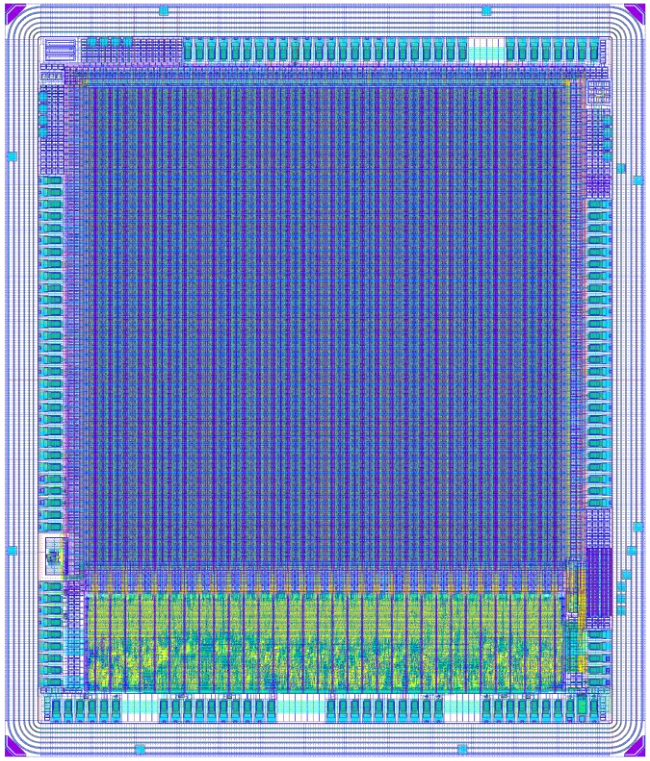


Latest Testbeam Results of RD50-MPW3 and Design of RD50-MPW4

Patrick Sieberer, on behalf of the RD50 CMOS working group

Before we start…

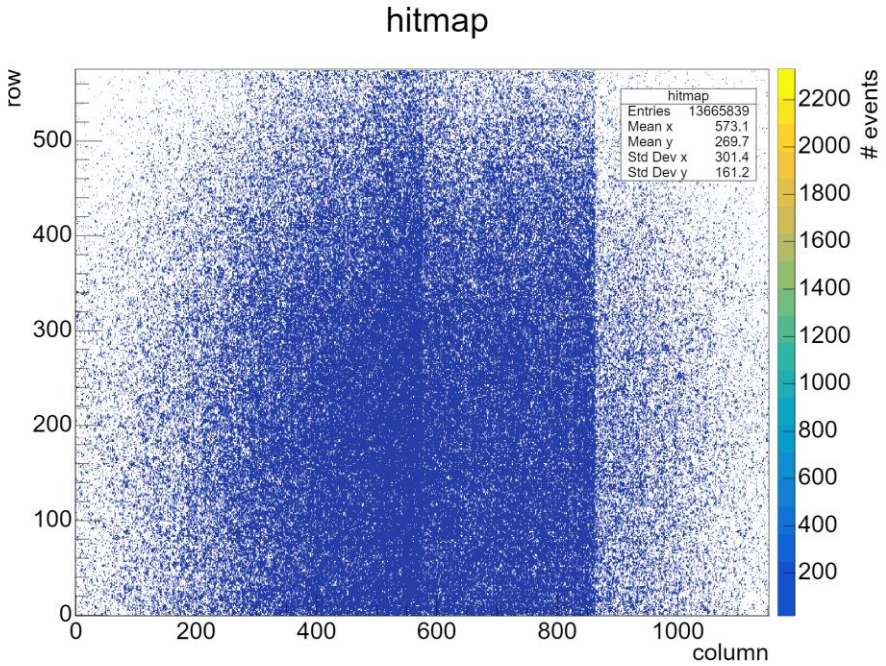
- Previous Talk: *Timing performance of the RD50 HV-CMOS*
  - Click
  - Introduction of the project and sensor can be found there

- Relevant talks from last meeting:
  - Initial testbeam measurements and setup: Click
  - Guard ring and biasing: Click

RECAP OF PREVIOUS RESULTS

Overview

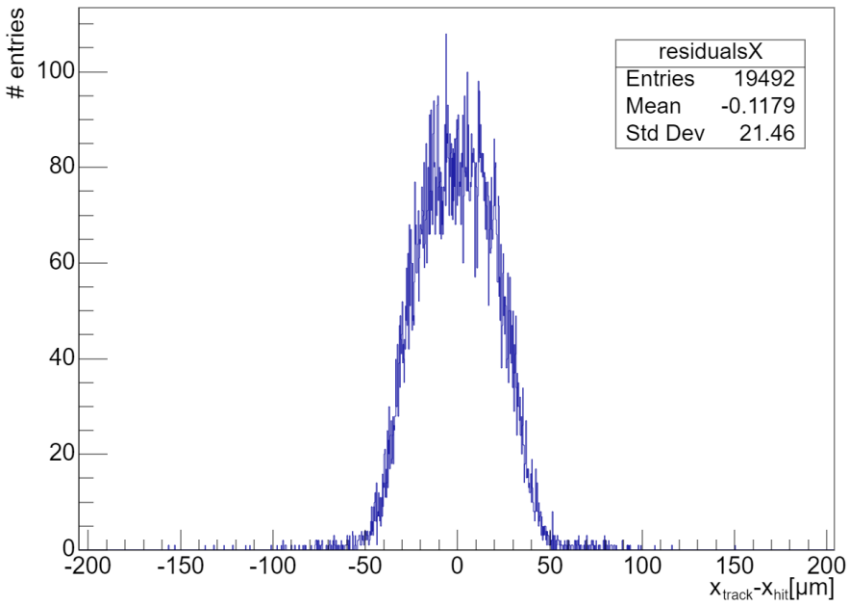
- Testbeam in October 2022 at CERN SPS
  - H6B (PPE 156) in the north area
  - 7 days of data taking
- Beam: 120GeV - “H6 mix”
  - Electrons, pions, …
  - Beam spot ~9mm
- Recorded data: around 16.2M Events
  - x10 = 160M tracks
    - track multiplicity of around 10, “pile-up”
    - Without timing and spatial cuts
  - Divided into 36 runs of ~30 min each



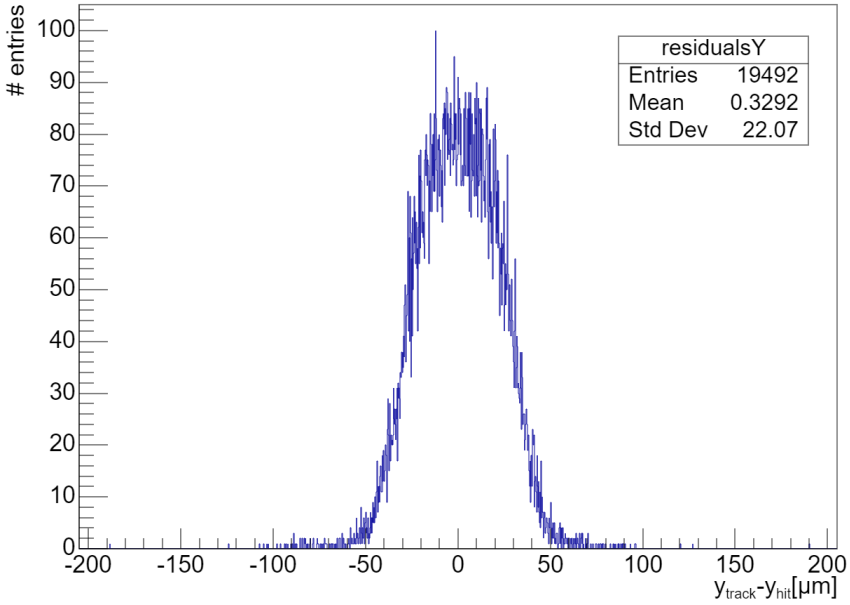
Single plane of telescope (pixel pitch18.4 x 18.4um)

Spatial Resolution - Update

RD50-MPW3 x-Direction



RD50-MPW3 y-Direction



Expected binary resolution: pitch / √12 = 18µm

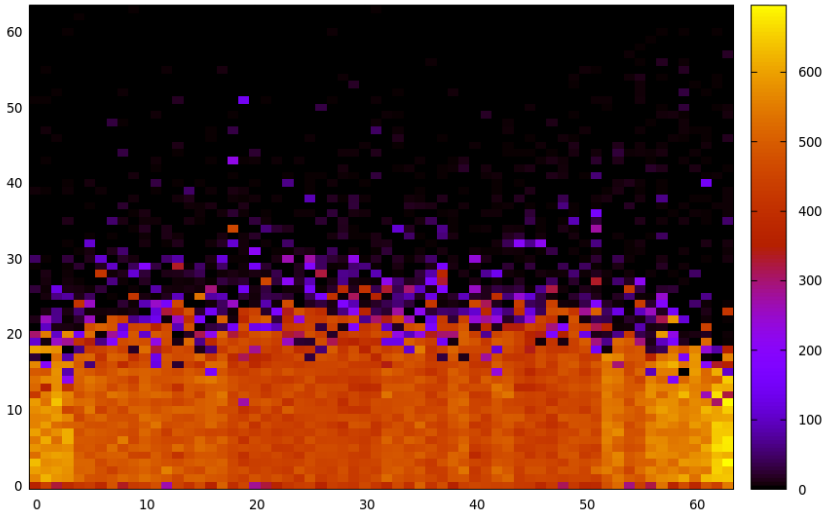
Efficiency - Update

Overflows shifted	Matched hits	Efficiency
-2	568	0.53%
-1	1439	1.34%
0	8540	7.93%
1	14869	13.81%
2	19033	17.67%
3	11106	10.31%
4	2879	2.67%
5	1054	0.98%

Sum: 55.24%.
Total Efficiency: 55.24% * 0.93 = **51.4%**

- Uncounted overflows lead to time shifts within the data set
  - 1 overflow = 3.2ms
  - Cannot be considered within one analysis run as an event of specific time
  - Multiple analysis runs on the same data set
    - All time shifts added for total efficiency
    - Probability of overlapping time bins subtracted

Observed Problems



Plain noise measurement of RD50-MPW3
(No testbeam data)

Huge noise observed

- Lower half of the matrix masked
- Calibration difficult
- High threshold needed
  - Also seen in cluster size
  - Reason for bad efficiency?
- Suspicion: Crosstalk from the digital periphery

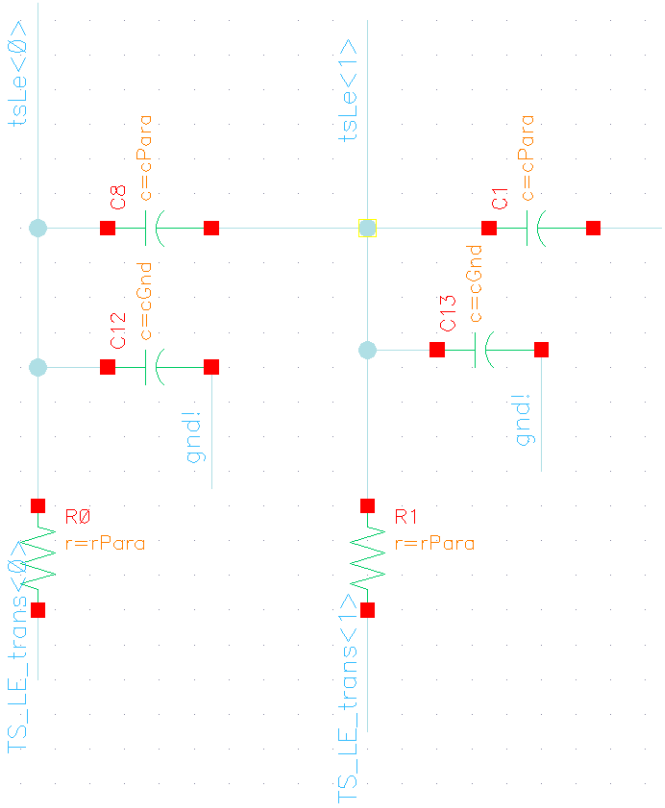
Minor Timestamp problem

- Timestamping incorrect at 40MHz
  - Need to slow down to 20MHz
  - Known and fixed before testbeam

SIMULATIONS OF RD50-MPW3 PROBLEMS

Timestamp Problem

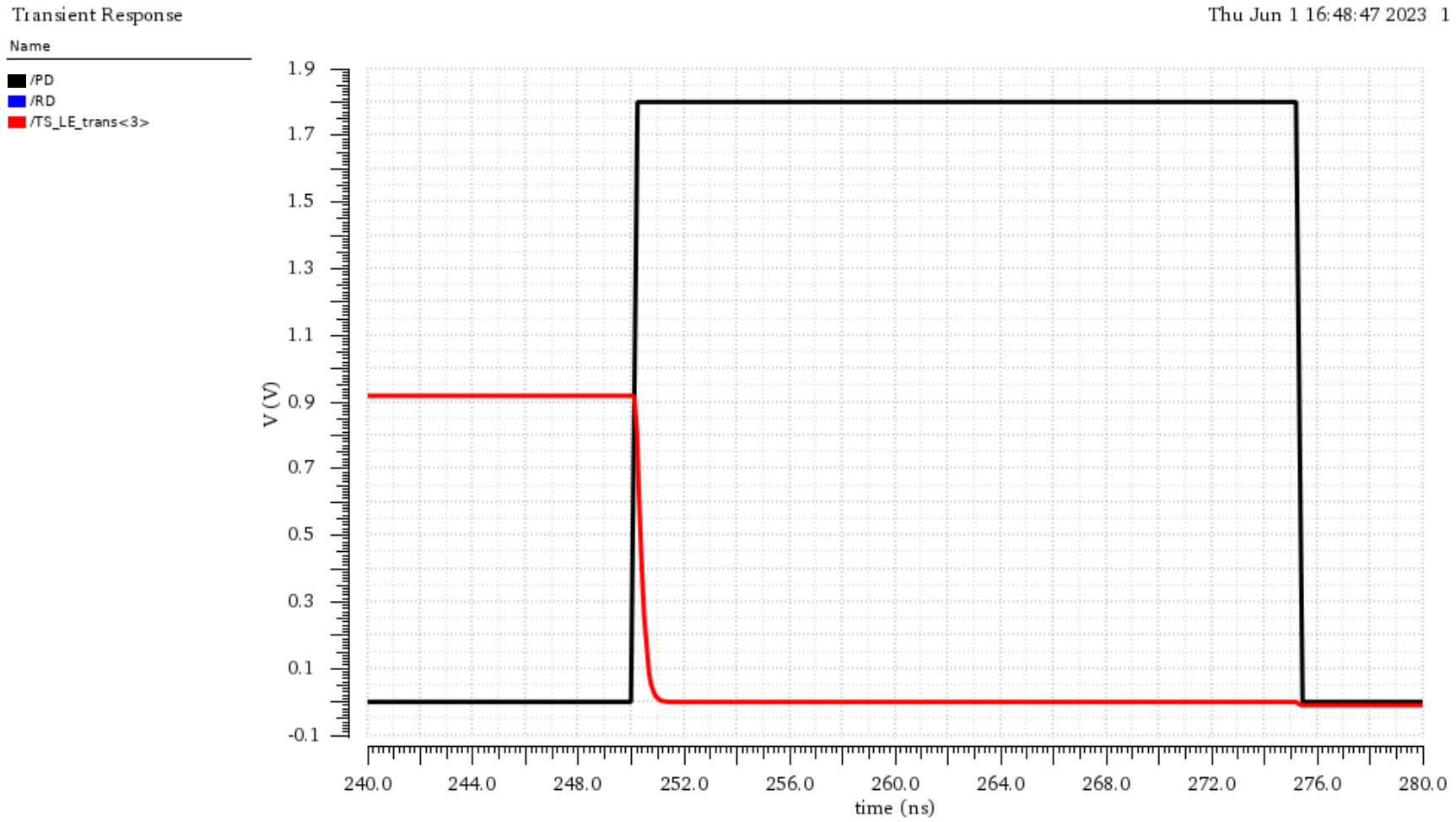
- Observed: Incorrect timestamps when running at 40MHz
  - Reported last meeting
- Model and simulate ‘full’ timestamp lines of the matrix
  - PULLDOWN signal: Discharge TS line
  - READ signal: Write (charge) TS to line



Thanks to Bernhard Pilsl for the plot

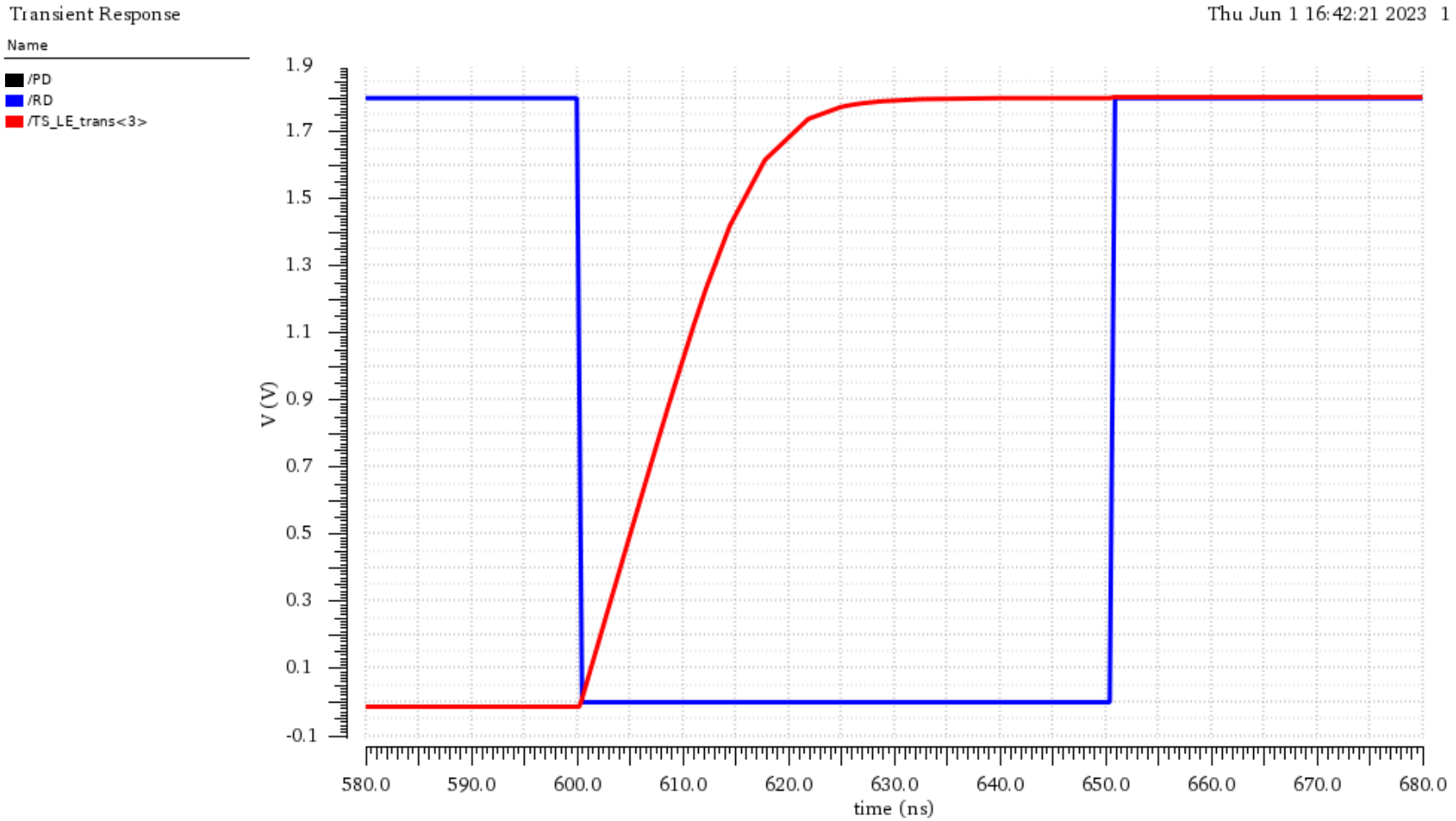
- cPara = parasitic capacitance to next line
  - Set to 0 (shielding lines)
- cGND = parasitic capacitance to ground
  - Varied (value not known)
  - 200fF
- rPara = resistance of readout line
  - Set to 5 Ohms (little influence)

Pulldown



Suspicion: Pulldown (PD) signal not properly discharging timestamp (TS) line
-> PD is long enough

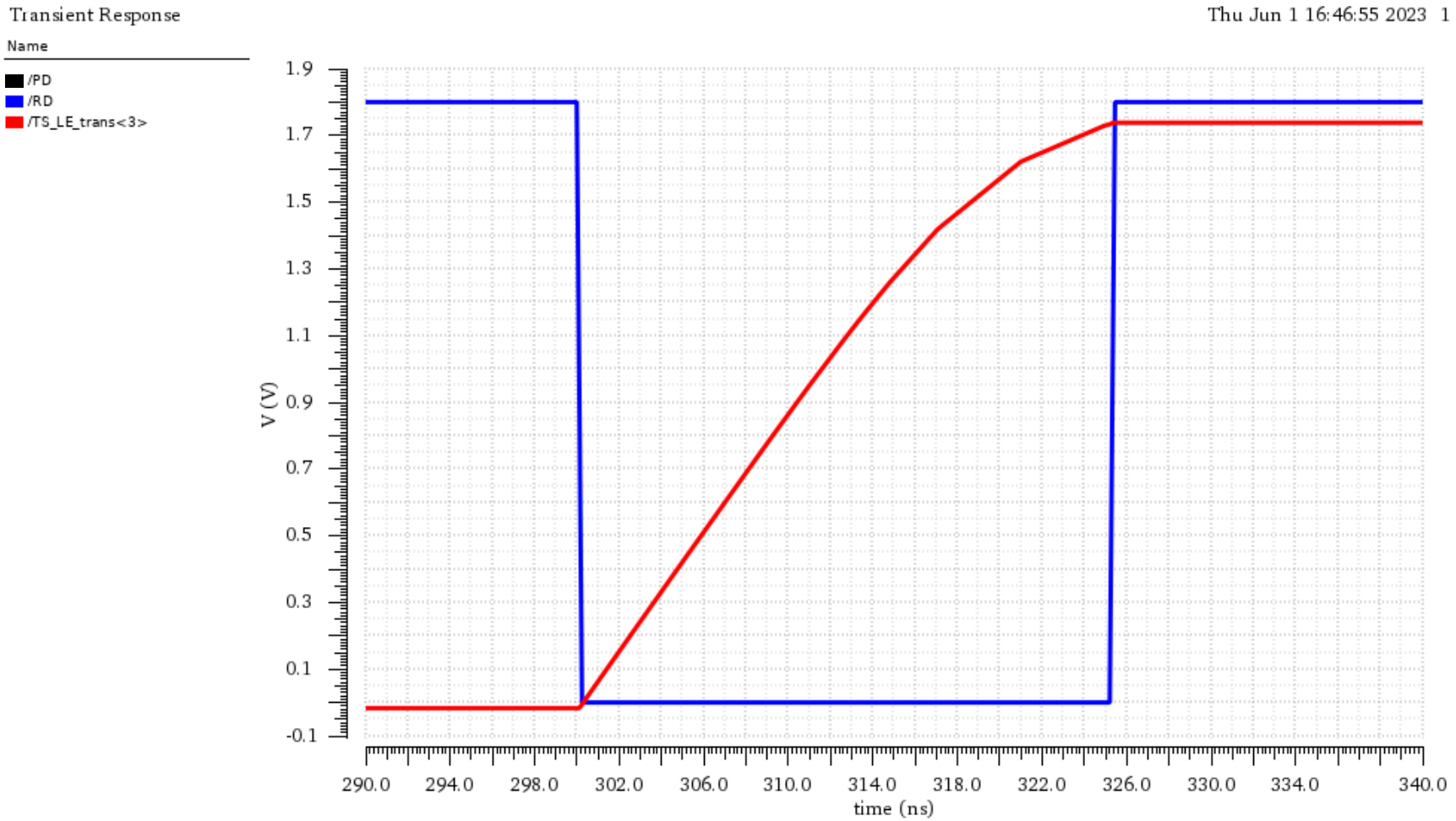
READ signal – 20MHz



Suspicion: Read (RD) signal not long enough to charge TS line

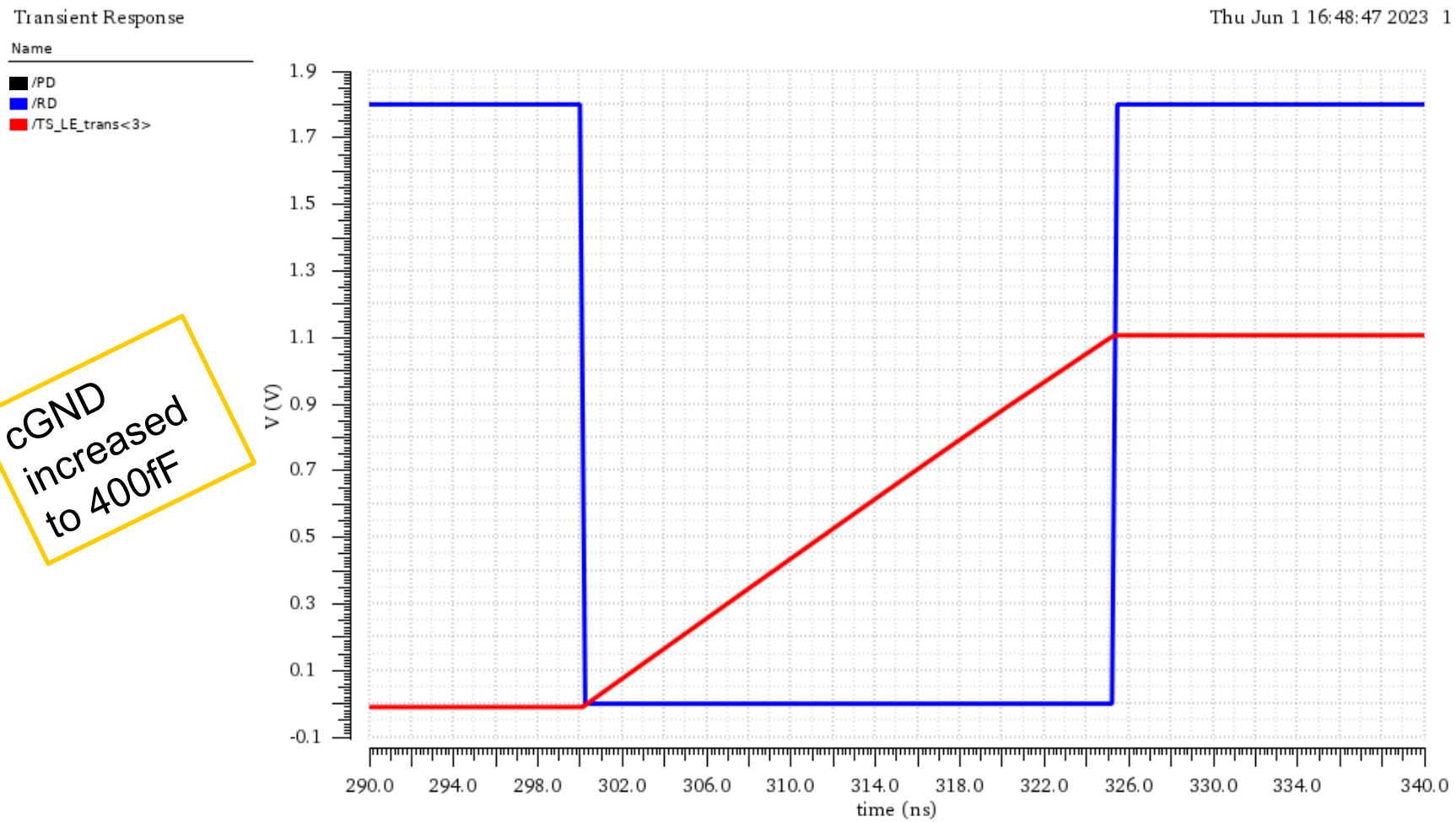
-> RD is long enough for 20MHz or 50ns

READ signal – 40MHz



Suspicion: Read (RD) signal not long enough to charge TS line
-> RD is <u>barely</u> long enough for 40MHz or 25ns

READ signal – high GND coupling



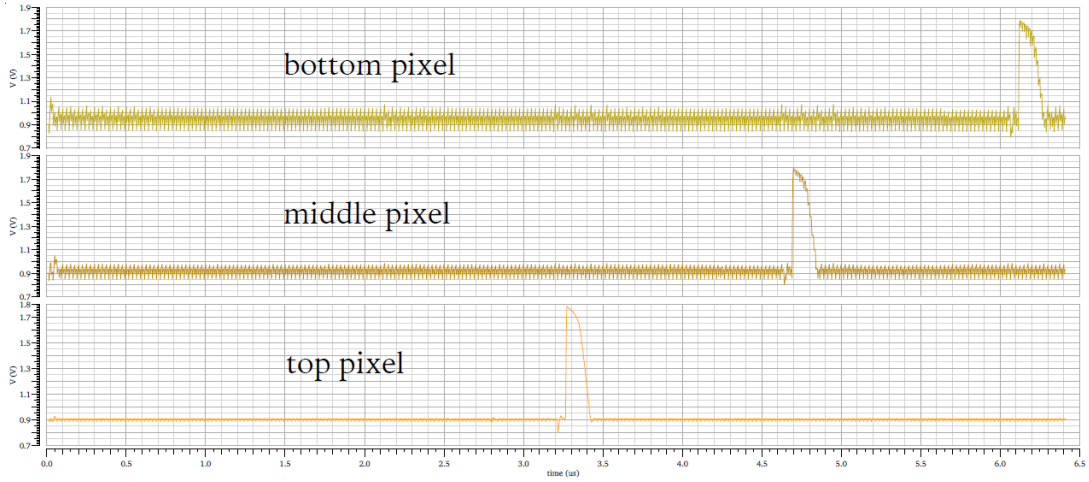
Suspicion: Higher coupling capacitance to ground increases charge time

-> RD is <u>not</u> long enough (for 25ns case)

-> **This is what seems to happen in RD50-MPW3**

Noise - coupling

- High noise observed in lower part
  - Suspicion: coupling of digital noise from the periphery
- Simulation for noise dependence on row number
  1. Connect only one pixel to analog readout line (SF_OUT) (parasitic extraction possible)
  2. Mimic digital noise on the ground
  3. Probe SF_OUT line
  4. Repeat for various row positions of the pixel on the SF_OUT line

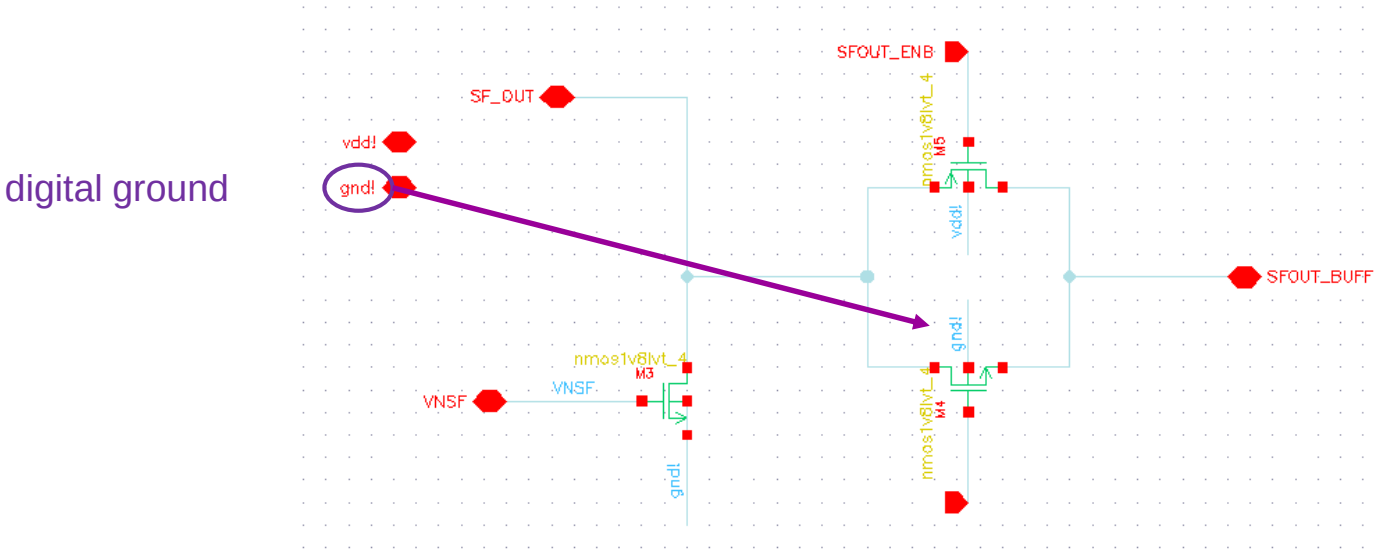


- >100 mV noise for bottom pixel possible
- Mimics what is measured

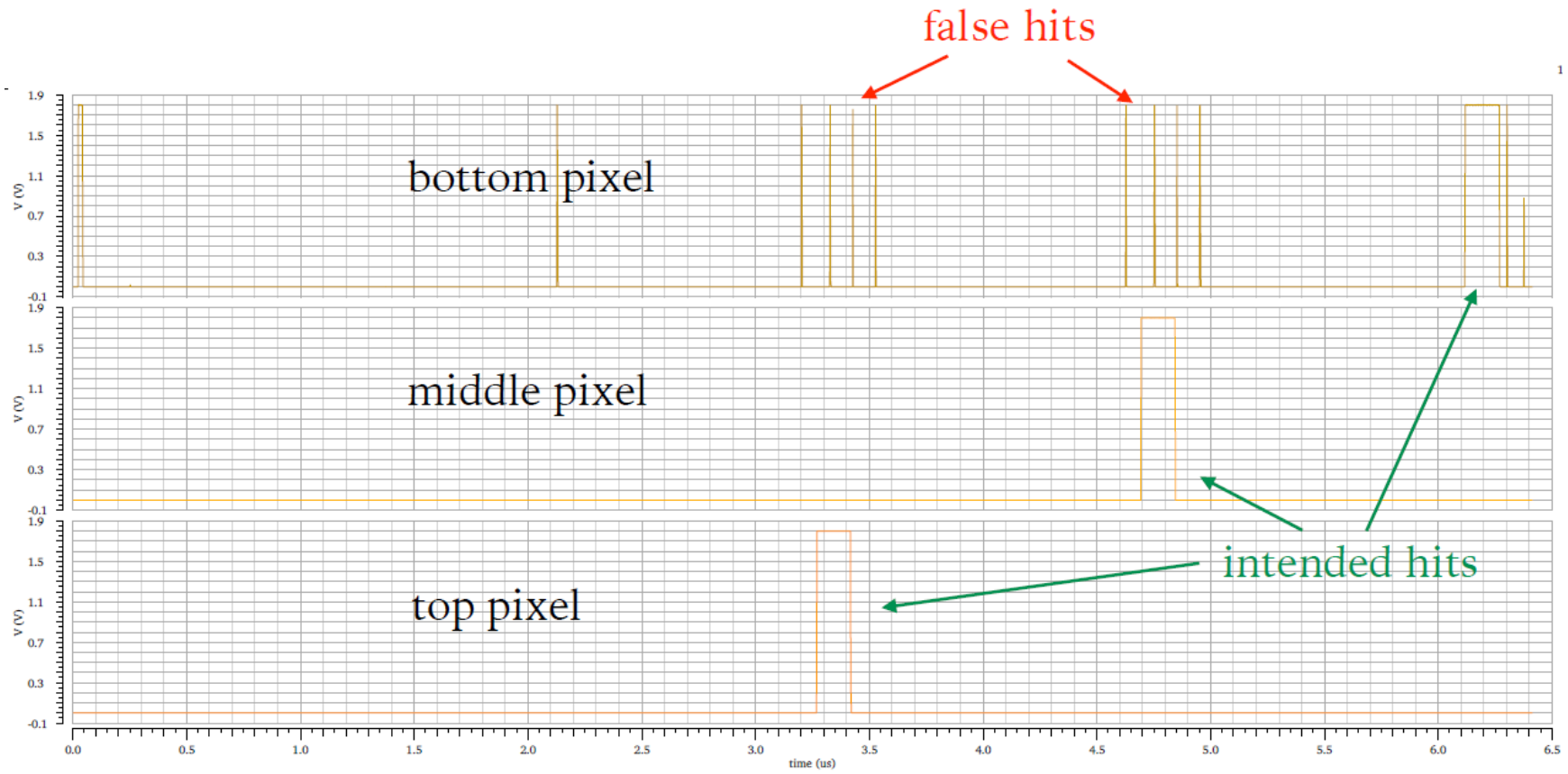
Thanks to Chenfan Zhang for the plots

Noise - coupling

- AC coupling unlikely, due to shielding lines (studied during design phase)
  - No typical crosstalk between lines
  - Detailed look at design: SFOUT buffer connected directly to digital power by mistake



COMPOUT Noise



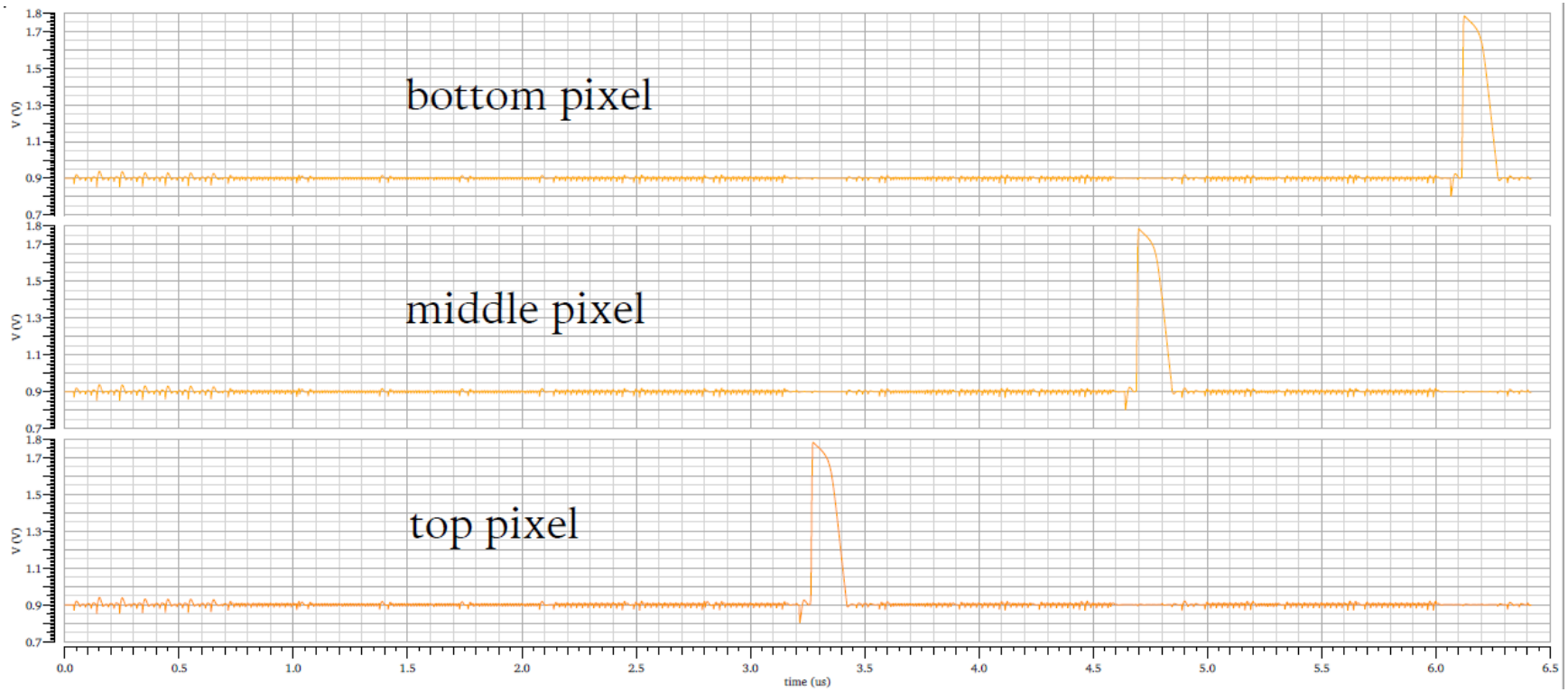
Noise causes false hits (measured after the comparator) for bottom pixels
-> **This is what seems to happen in RD50-MPW3**

DESIGN RD50-MPW4

Digital Features

- Readout of pixels configurable
  - PD and RD signals can be delayed and stretched
  - Mitigate Timestamp issue
- Debug outputs removed
  - Everything working fine in RD50-MPW3
- External control removed
  - Everything working fine in RD50-MPW3
- SERIN/SEROUT pin positions switched
  - Easier routing when connected to matrix

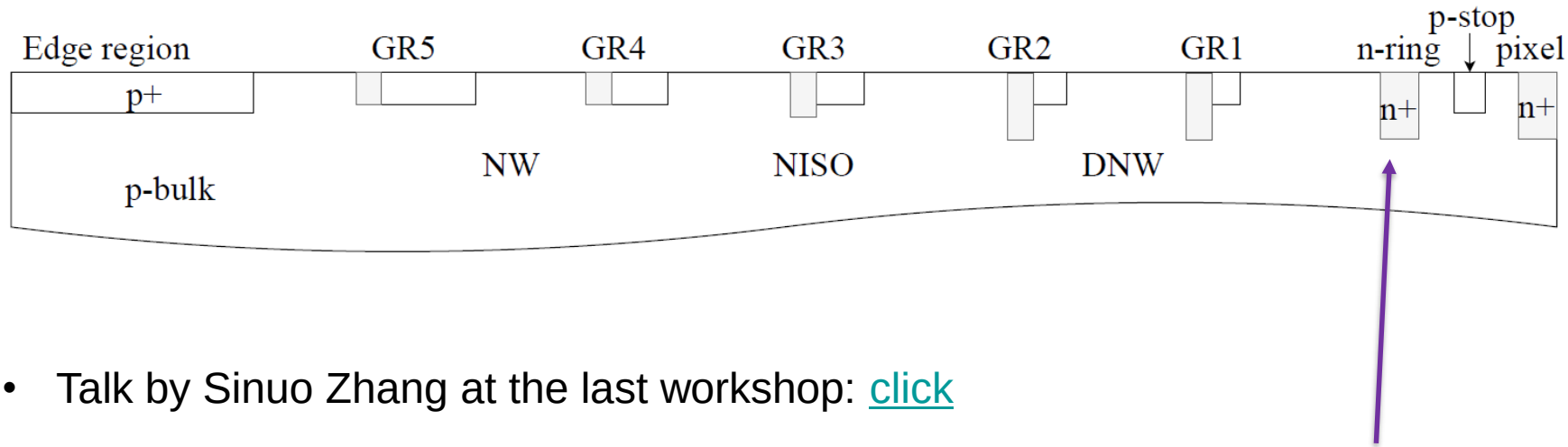
Top Level Fix – Separate Grounds



- Connect analog ground instead of digital ground to SFOUT buffer to reduce noise

-> No false hits seen in simulation anymore

Analog Features - Guard Ring



- Talk by Sinuo Zhang at the last workshop: click
- Breakdown approaching 400V or higher for the 1.9 kOhm substrate resistivity
  - Compared to ~150V now

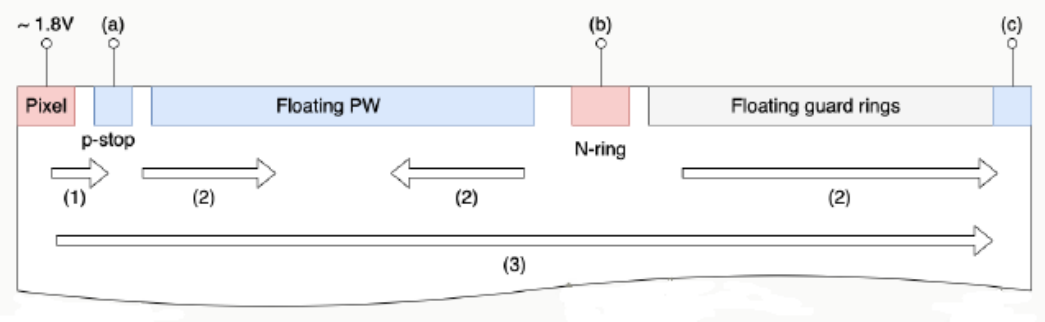
n-ring for edge biasing (next slides)

Thanks to Sinuo Zhang for the plot

Analog Features – Biasing

Moving from biasing via p-stop implant to edge or backside bias

- Optional, p-stop implants still fabricated, can be left floating



I) RD50-MPW3 biasing method: -HV at a)

- Potential drop (1), rest not relevant
- Limit = distance pixel – p-stop

p-implant
n-implant

II) Edge bias with floating p-stop: -HV at (c)

- Potential drop (3), much larger distance (across entire periphery!)
- Large Floating PW suppresses potential
- Biggest part of potential drop still (1)

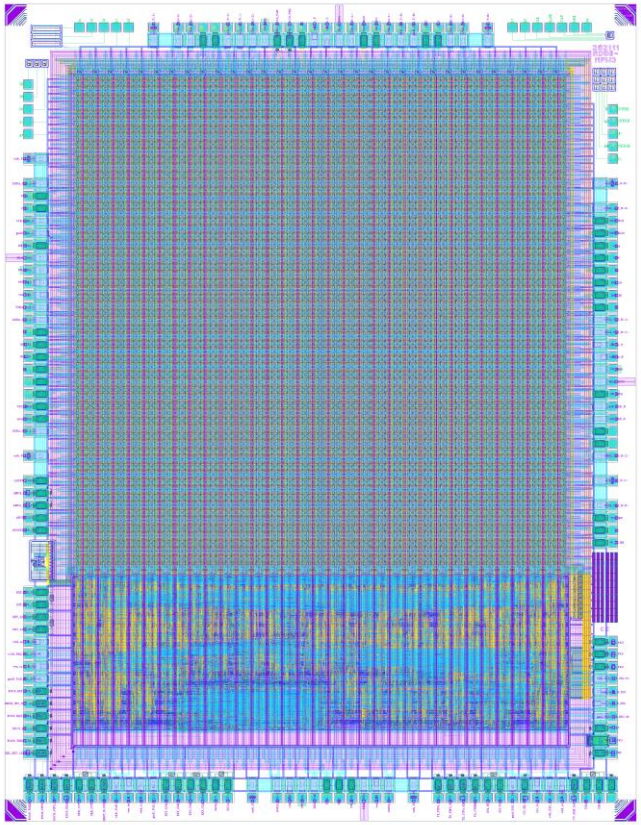
III) Edge bias with floating p-stop and biased N-ring at 0V: -HV at (c)

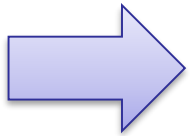
- Potential drop (2), consist of 2 parts
- Guard ring layout has huge effect
- Large Floating PW and p-stop can still cause potential drop

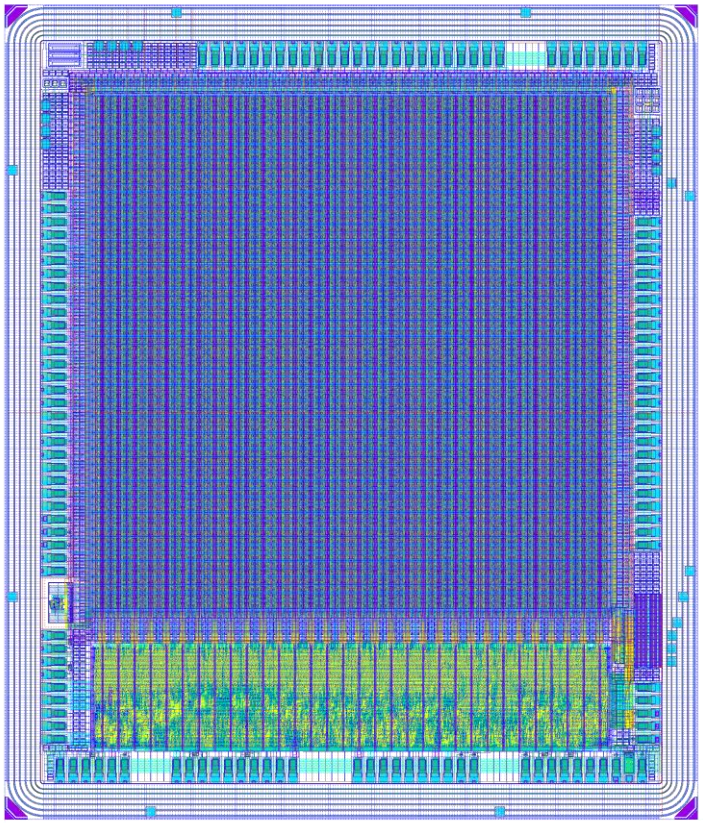
Thanks to Sinuo Zhang for the plot

Layout

RD50-MPW3







RD50-MPW4

Further Changes in RD50-MPW4:

- Large floating PW removed
- More space between matrix and edge due to new guard ring (including new pads)
- Buffer sizes in periphery decreased (less space)
  - RD50-MPW3 and RD50-MPW4 about the same area, but a bit different shape

Outlook

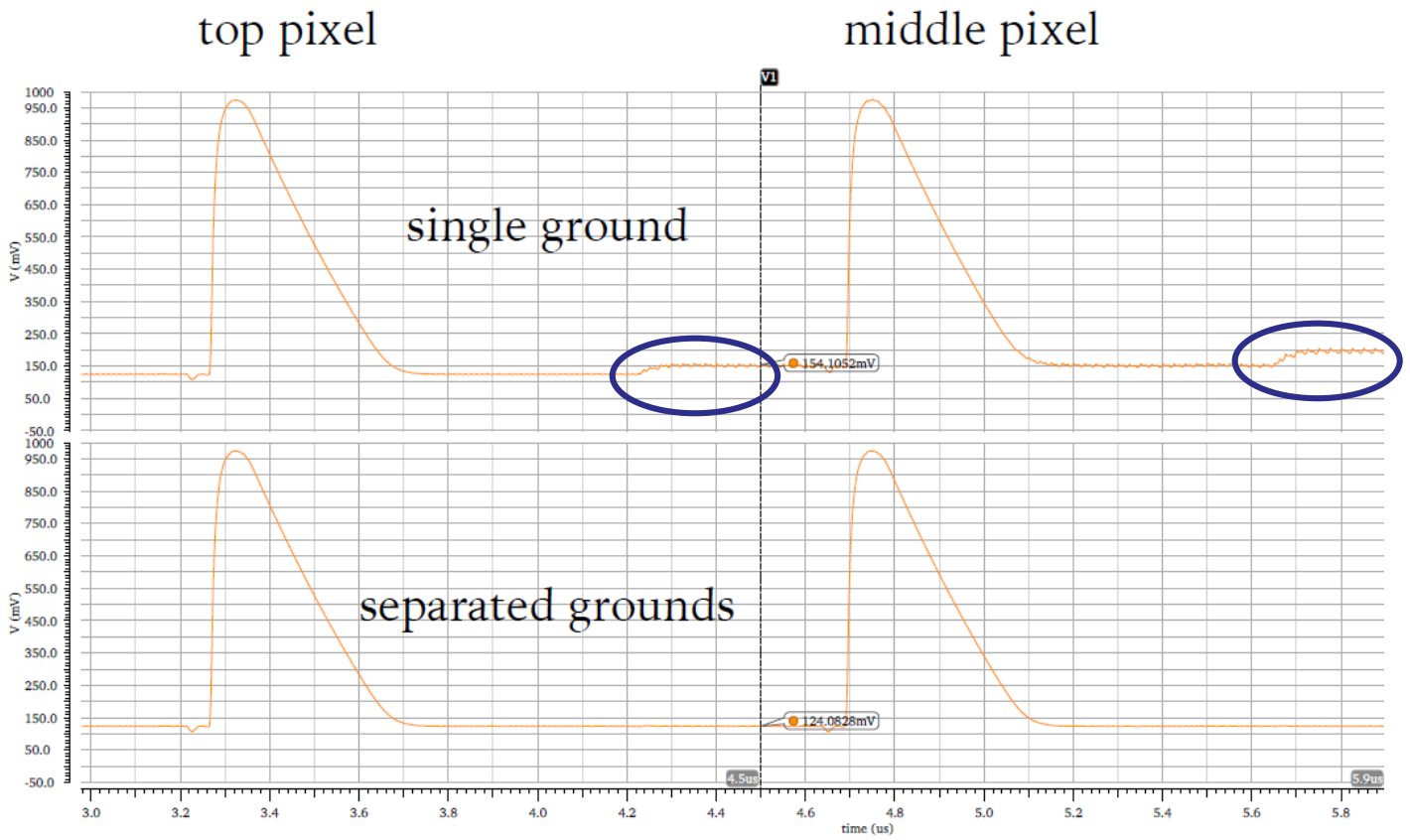
- Very first large-scale testbeam at CERN conducted by the group
  - Spatial resolution meets theory predictions
  - Noise Problem observed and fixed in next submission
    - Efficiency loss most likely originating from noise
- Design of RD50-MPW4 finished
  - Mitigating noise and timestamp bug
  - frontside and backside (new!) biased samples
  - **Submitted in May**, expected in November

- RD50-MPW3 samples irradiated, distribution ongoing
- Preparation for *next testbeam at DESY in July* ongoing

This is my last contribution to this community, as I move to chip development for photon science – It was a pleasure to work with all of you, thank you very much for the last years.

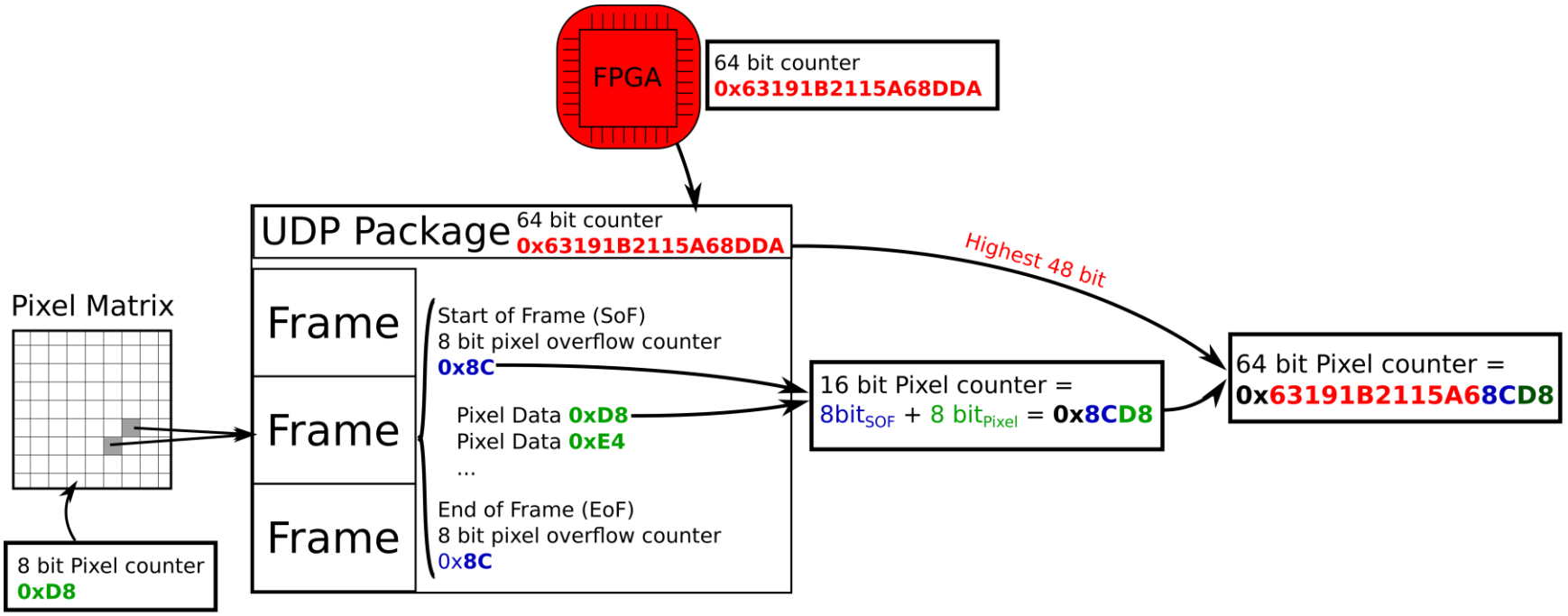
BACKUP

Baseline Shift



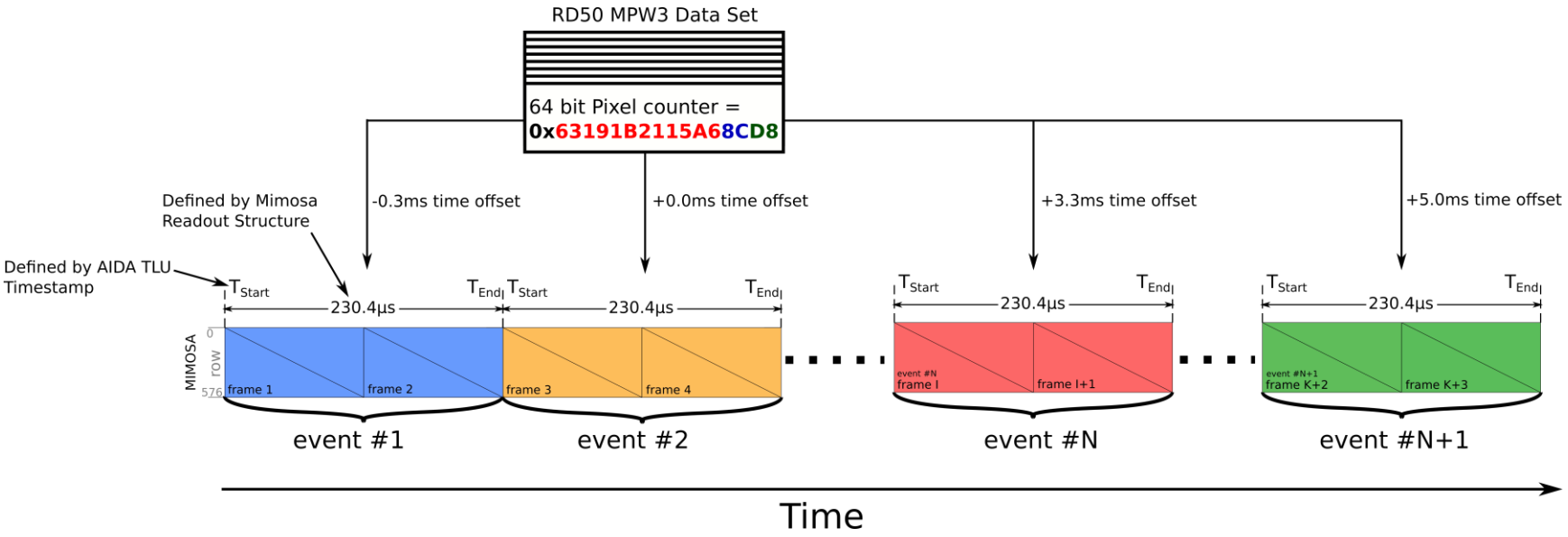
- Baseline shift measured if multiple pixels are enabled
  - Also found in simulation
  - Ignored for the measurement, as it's not severe
- Behavior gone for separated grounds

Time Synchronization



Thanks to Uwe Krämer for the plot

Event Building



Thanks to Uwe Krämer for the plot