ÖAW AUSTRIAN ACADEMY OF SCIENCES

HEPHY INSTITUTE OF HIGH ENERGY PHYSICS

SiC Wafer Layout

For SiC-LGAD RD50 common project

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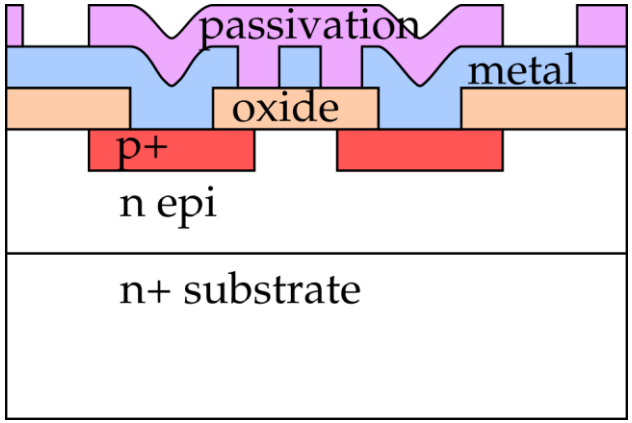
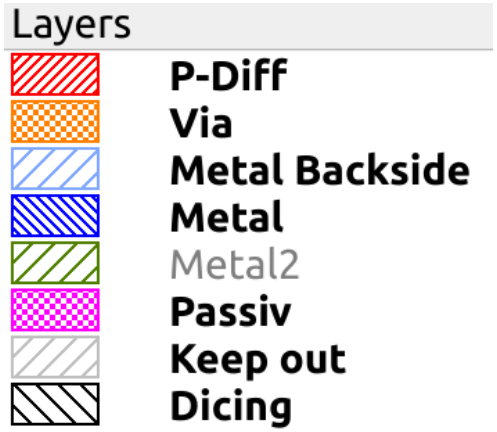
Slides prepared by Simon Waid

Process and Manufacturing

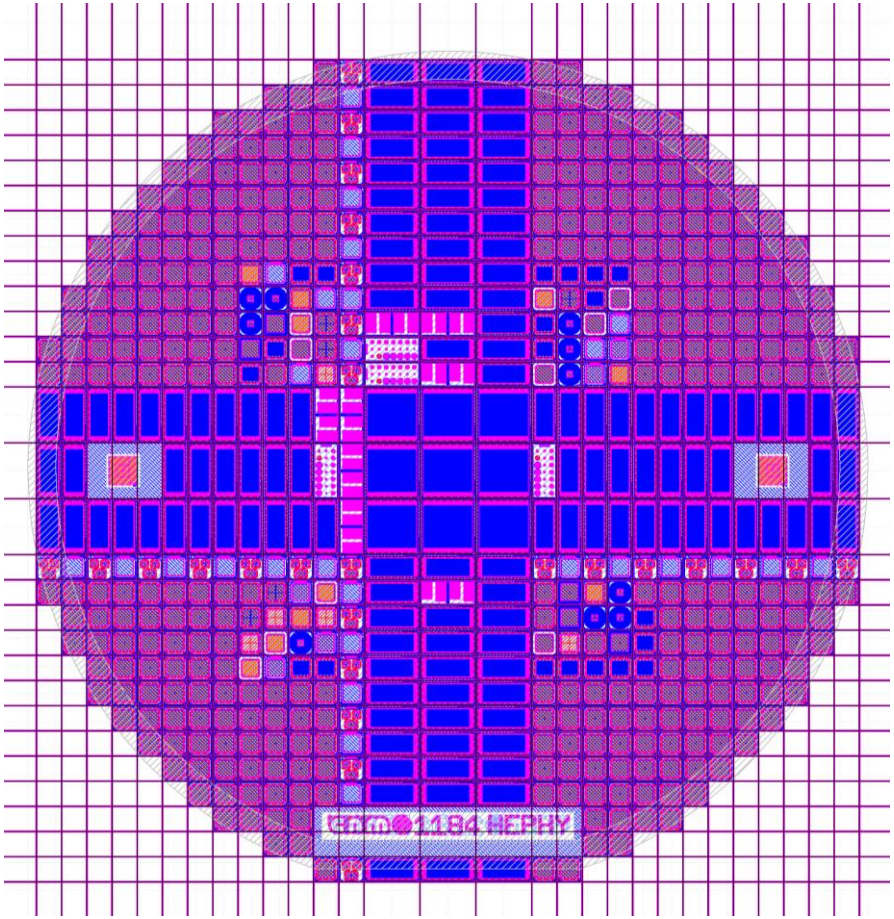
- Process details:
  - 6 inch wafer, full wafer mask
  - p+ implant on n epi layer
  - 5 masks: implant, via, metal, passivation, backside metal
- Manufacturing:
  - 3 wafers 50µm substrate
  - 2 wafers 100µm substrate
- Timeline:
  - Tape-out: End of April 2023
  - End of production: October 2023





Foreseen Structures

- 303 pcs. 4.5 x 4.5 mm² dies
- 9 pcs. 10x10 mm² dies used for strip detectors
- 126 pcs. 10x4.5 mm² dies.



Foreseen Structures

- Pad detectors
- Strip detectors
- Pad shaped MOSCaps
- Test vehicles
  - Round MOSCaps
  - MOSFET (and gate length test)
  - Diodes for Edge TCT
  - Gate controlled diodes
  - Guard ring variations
- Other structures
  - Pixel array
  - Resistive detector

Pad Detectors

ID	PAD size	Description
1M	3x3mm²	Metallized; Identic to structure 1M on CNM wafer #
1	3x3mm²	Not metallized; Identic to structure 1 on CNM wafer #
PAD	3x3mm²	Metallized with 100µm central hole for TCT. Compared to 1 and 1M then guard structure has been improved.
P-4Q	3x3mm²	4 quadrant; Not metallized
P-4QM	3x3mm²	4 quadrant; Metallized
P-MC	3x3mm²	Same as PAD but has a Schottky contact below the outer metal
P-MG	3x3mm²	Metallized with a microgrid for TCT
P-MOH	3x3mm²	Same as PAD but uses a modified guard structure
P-WSA	1x1mm²	Same as PAD, guard structure optimized for operation in air
P-WSB	1x1mm²	Same as PAD, guard structure optimized for operation in air
P-NM	3x3mm²	Not metallized, similar to 1 but uses the same guard as PAD
P-TRI	2x 1x1mm²; 1x1.9 mm²	Three Detectors with small capacitance. Includes a process test structure.

Strip Detectors

ID	Pitch	Description
S-1CM	250µm	Small-scale prototype for HDM detectors
SD	250µm	For HDM daisy chain tests
SP100	100µm	32 strips
SP50	50µm	64 strips
SV25	100µm	32 strips with a distance of 25µm
SV50	100µm	32 strips with a distance of 50µm

Pad Shaped MOSCap

ID	Size	Description
MOS-IN	3x3 mm²	Hole donor implant close to, but not overlapping the capacitor metal plate
MOS-FI	3x3 mm²	P-Implant over the full capacitor area
MOS-NO	3x3 mm²	No hole donor implant
MOS-IOH	3x3 mm²	Hole donor implant having a 6µm overlap with the capacitor metal plate

All MOSCAP dies contain process test structures

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Test Vehicles

ID	Description
MOS1	Round MOSCAPS, Hole donor implants match MOS-NO and MOS-IN
MOS2	Round MOSCAPS, Hole donor implants match MOS-FI and MOS-IOH
GCD	Gate controlled diodes
T-S	Straight transistors
T-R	Round transistors
D-R	Round diodes with varying radii
TCT	Long diodes for edge TCT
DR-GR	21 variations of guard rings for validating TCAD simulations
GLT1.5	Structures intended for measuring the real gate length on T-S and T-R
GLT3	Structures intended for measuring the real gate length on T-S and T-R

All dies contain process test structures

Other Structures

ID	Description
PIX-C	Array of pixel diodes for bump bonding. Intended to be compatible with CROC and similar chips.
PIX-M	Array of pixel diodes for bump bonding. Intended to be compatible with MPROC.
RES	Resistive detectors

General Remarks

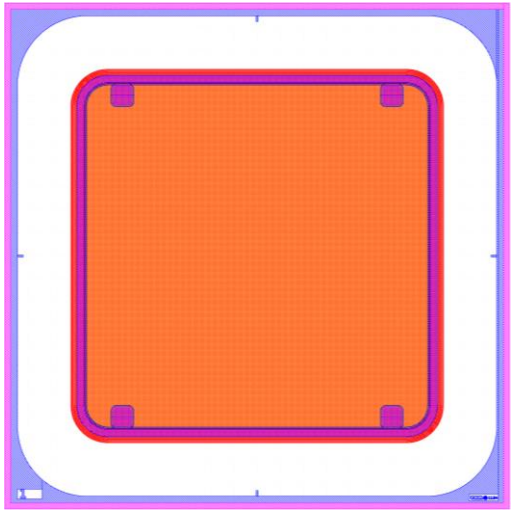
- With exception of „1“ and „1M“ all dies are equipped with unique identifiers encoded in roman letters and QR codes.
- With exception of „1“ and „1M“, alignment marks on all 4 corners enable positioning of dies.

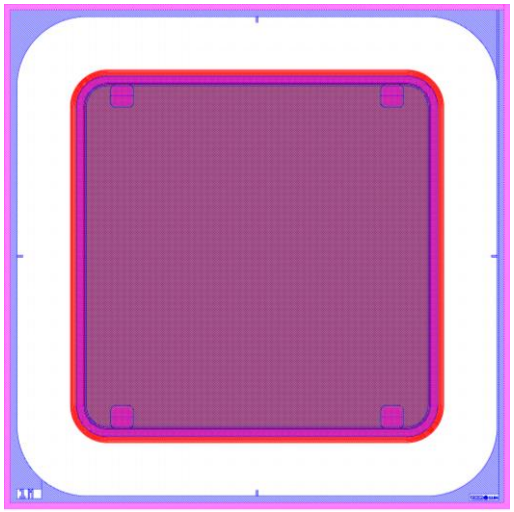
PIX 5_2, -1

Pad Detectors 1 and 1M

Taken over directly from the design of CNM wafer run no. 1011. Pads have a size of 3x3 mm²

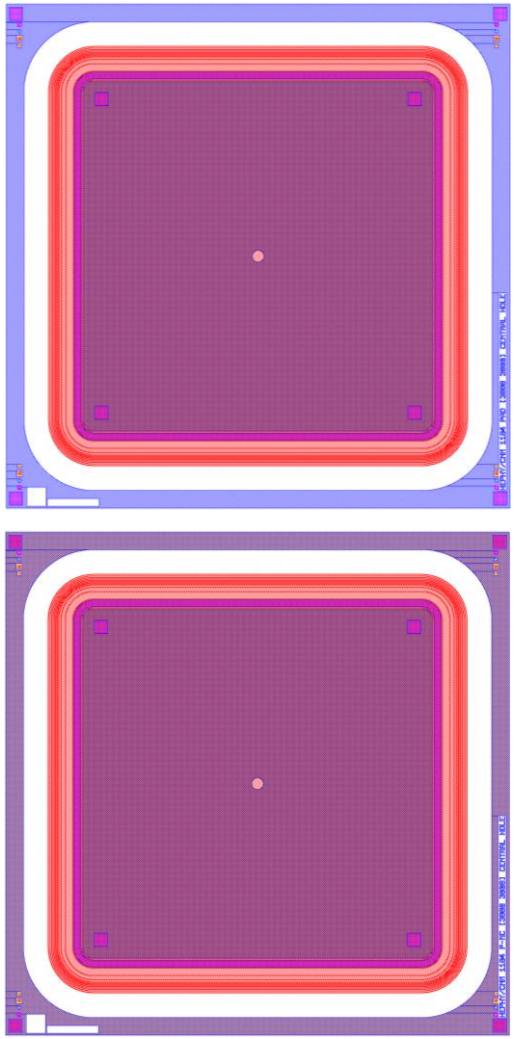
- The pad on „1“ (top) has a metal ring around the active area. The active area however is not metallized. Due to the high resistivity of the implant the pulse shapes generated by impinging particles will be deformed. The via layer is open over the active area, thus the material budget is minimized.
- The pad „1M“ (bottom) has metal over the full area. Otherwise it resembles „1“
- The guard structure consists of 5 rings with a width of 5µm and a distance of 5µm. PAD and PAD-NM are similar but have an improved guard structure.





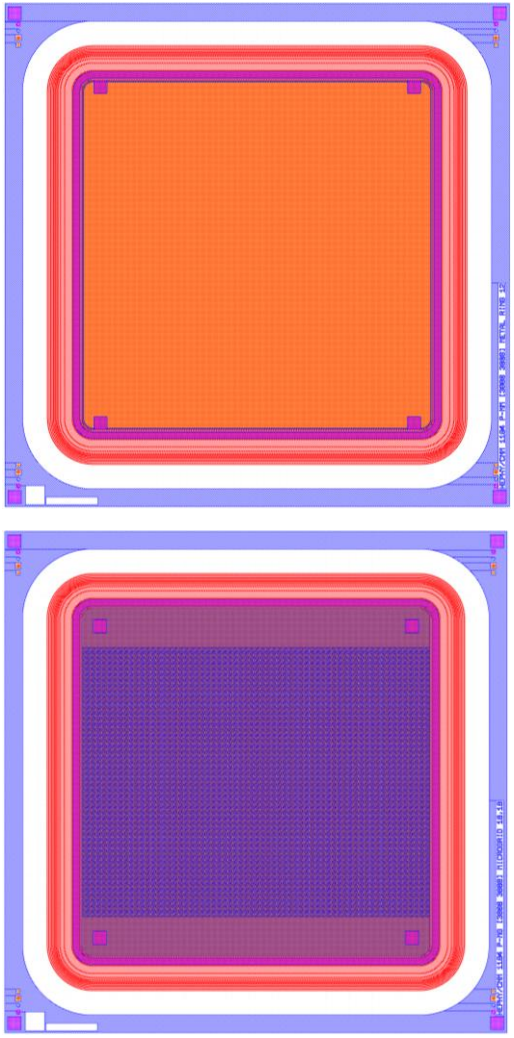
Pad Detectors PAD and P-MC

- The design of „PAD“ is similar to „1M“. Changes include:
  - The guard has been optimized towards higher operating voltages
  - A central hole in the metallization with diameter of 100 µm serves as entrance point for a laser e.g. to perform TCT measurements.
- The design P-MC equals PAD, except that the outer metal is in contact with the substrate.



Pad Detectors P-NM and P-MG

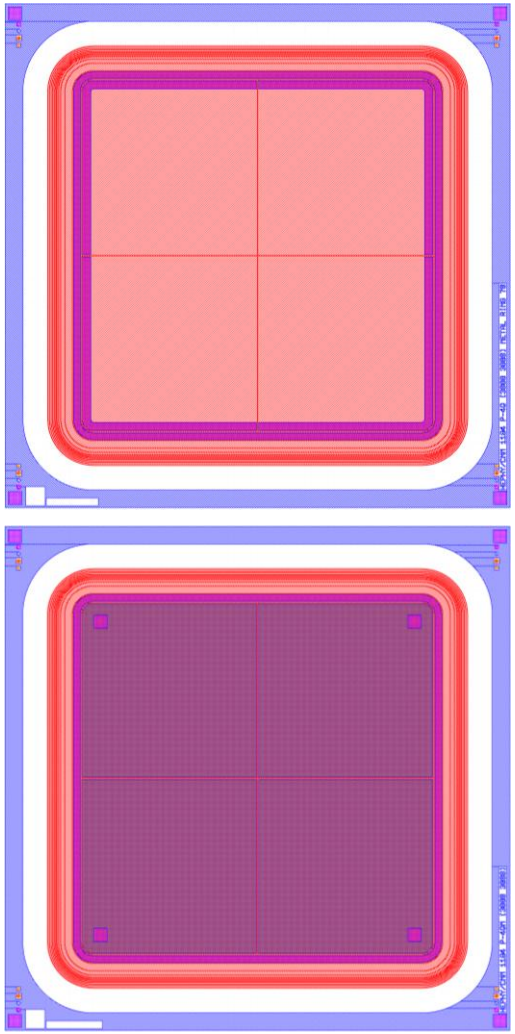
- P-NM (top) is similar to “1”. However, similar to “PAD” it uses an improved guard ring
- P-MG (bottom) is similar to „PAD“. However, instead of a central hole it uses a fine grid of holes 10µm in size and 10µm apart.



Pad Detectors
P-4Q, P-4QM

This detectors are pads split into quadrants.

- P-4Q (top) has no surface metallization
- P-4QM (bottom) has a surface metallization

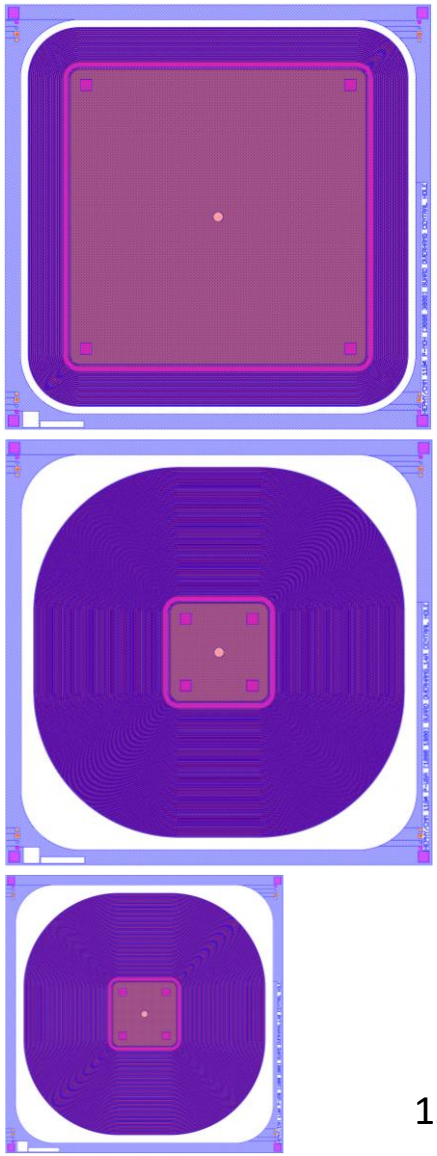


Pad Detectors P-MOH, P-WSA and P-WSB

“P-MOH”, “P-WSA” and “P-WSB” use metal overhang structures in the guard ring.

- “P-MOH” (top) is a test vehicle and not expected to work at high voltages.
- “P-WSA” (center) and “P-WSB” (bottom) are designed to minimized electric fields in air. “P-WSA” uses relaxed design rules. In the unlikely event fabrication of “P-WSA” fails, “P-WSB” is a fallback. It uses stricter design rules at the cost of worse performance.

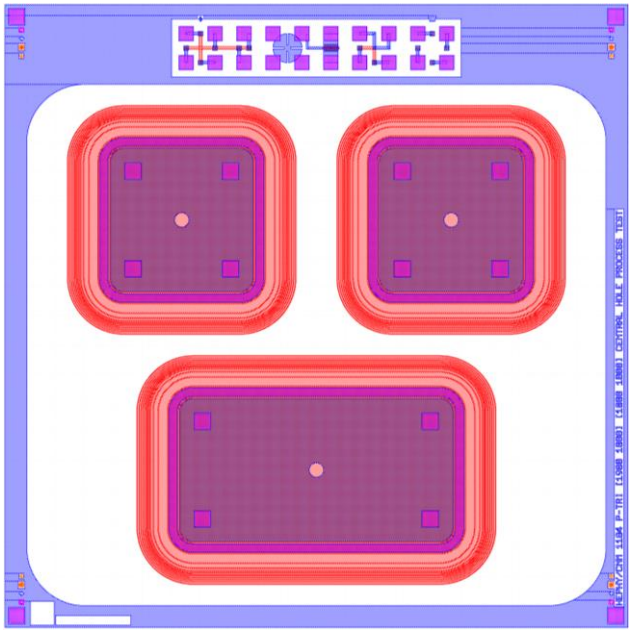
Due to the current limited capabilities of SiC TCAD models the structures have not been fully optimized. For future designs one might envision optimizing P-WSA/P-WSB. The guard rings are potential candidates for the final HDM detector.



Pad Detectors P-TRI

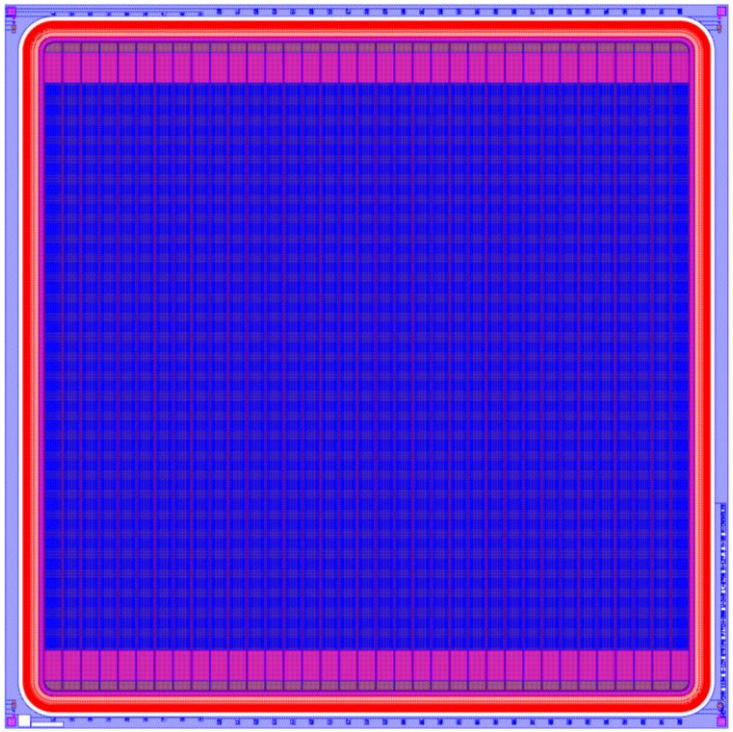
Three detector diodes enable measurements with low capacitance. A central hole in the enables TCT measurements.

The sizes are two times 1x1 mm² (top) and 1x1.9 mm² (bottom).



1x1 cm² Strip Detector S-1CM, Pitch 250µm

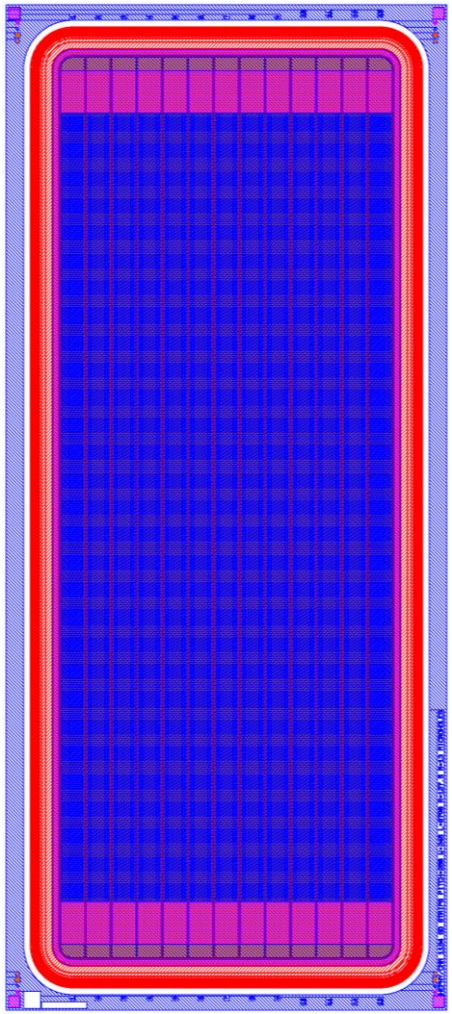
Demonstrator for the HDM system. It has 35 strips with a pitch of 250µm. The die area is 1x1cm². The guard structure has been optimized for high voltages. However, distances in air are insufficient. To prevent arching, the dies will need to be covered by a protective film.



1x0.45 cm² Strip Detector SD; Pitch 250µm

Identic to S-1CM but with a lower number of strips. Intended to be daisy chained for testing realistic detector capacitances on the HDM system.

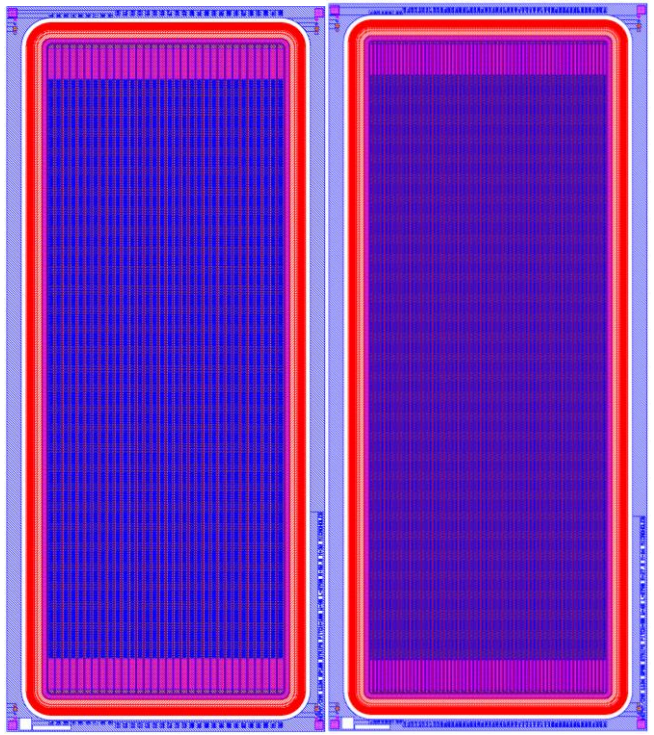
To prevent arching, the dies will need to be covered by a protective film.



Strip Detectors SP50 and SP100

- SP50 Contains 64 Strips having a pitch of 50µm.
- SP100 Contains 32 Strips having a pitch of 100µm.

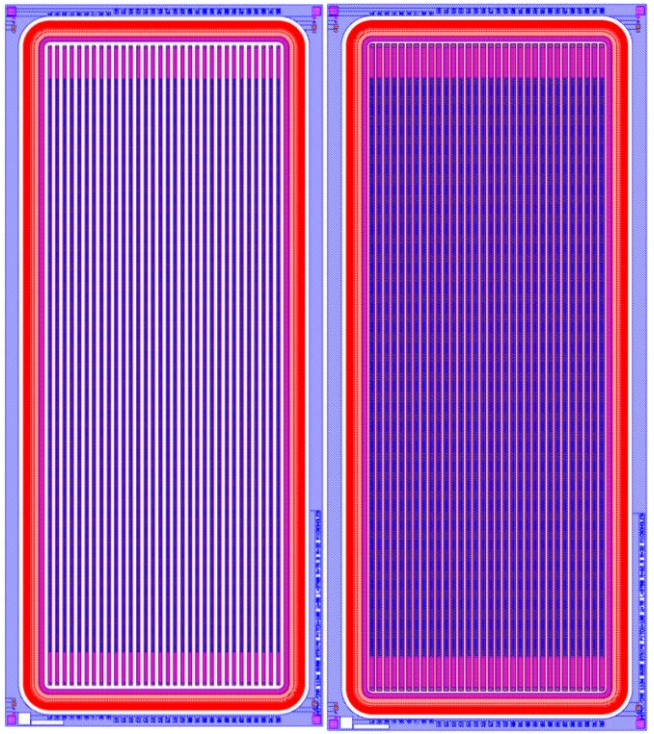
To prevent arching, the dies will need to be covered by a protective film.



Strip Detector with Narrow Implants SV25 and SV50

Both contain 32 Strips having a pitch of 100µm. The distance between the strips is 25µm for SV25 and 50µm for SV50.

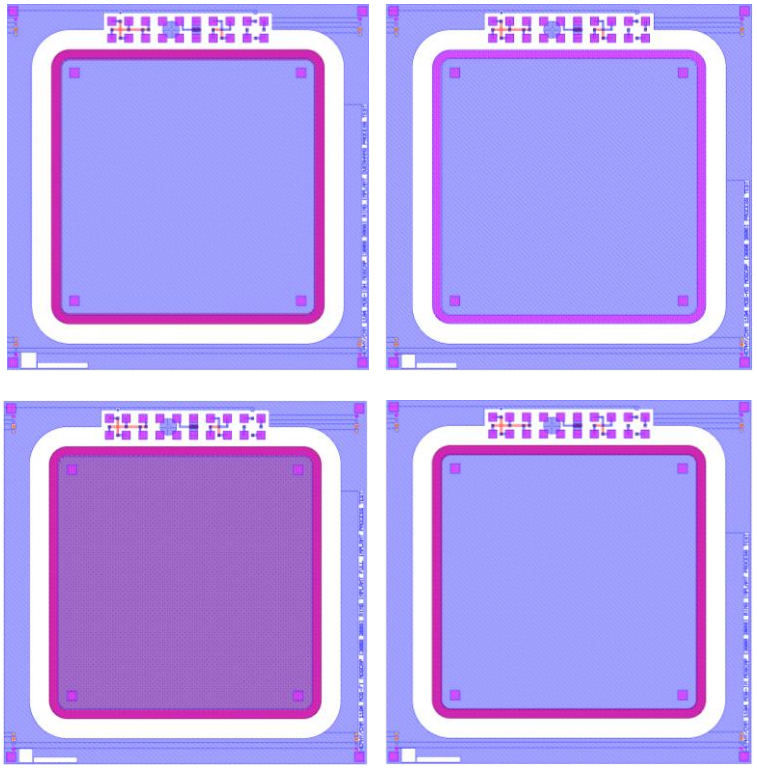
To prevent arching, the dies will need to be covered by a protective film.



MOSCAPs

4 MOSCAP design were implemented.

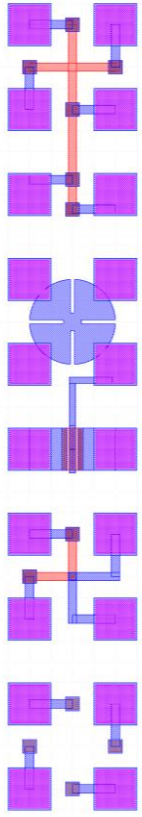
- „MOS-NO“ (top-right) has no implant. It is expected to fail in delivering minory carriers to the area below the oxide.
- „MOS-IN“ (bottom-right) has a contactable implant ring at a distance of 6 µm to the top electrode. This ring might help in providing minority carriers.
- „MOS-IOH“ (top-left) has a contactable implant ring overlapping 6 µm with the top electrode. This ring might help in providing minority carriers. This device is expected provide minority carriers in a way similar to the channel formation in a MOSFET.
- „MOS-FI“ (bottom-left) has a contactable implant covering the full area of the top metal.



Process Test Structure

This structure contains:

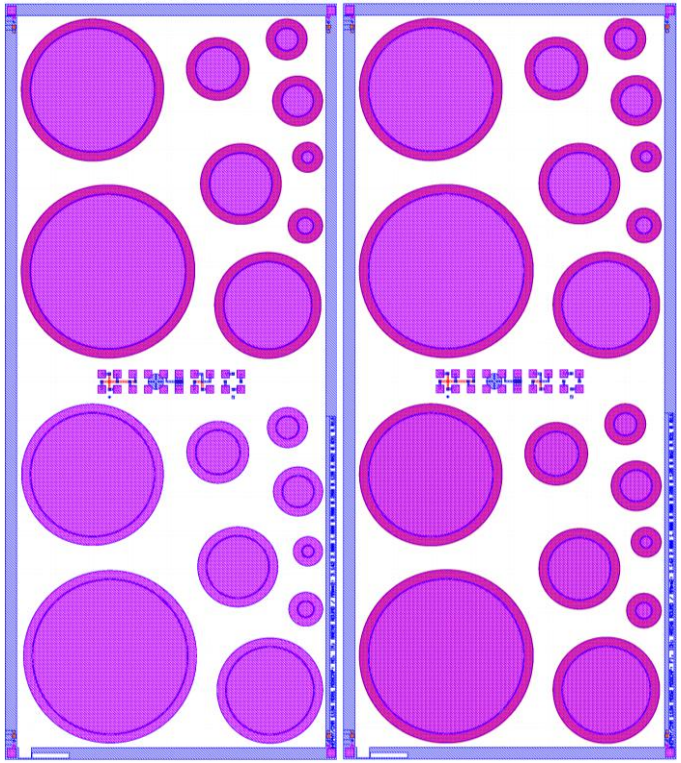
- Van-der-Pauw structures for Implant, Substrate and Metal
- An enhancement mode MOSFET
- A cross kelvin bridge for the metal-implant contact



Round MOSCaps (MOS1, MOS2)

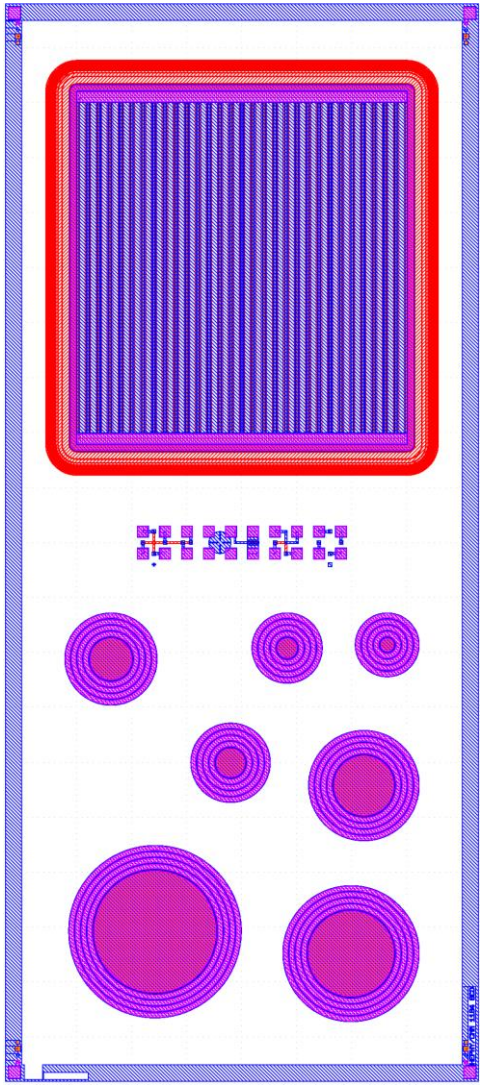
MOSCaps with varying radii, can be used to measure edge effects. The implemented hole-donor match the pads as follows:

- MOS1, left bottom: MOS-NO
- MOS1, left top: MOS-IN
- MOS2, right bottom: MOS-FI
- MOS2, right top : MOS-IOH



Gate Controlled Diodes (GCD)

A GCD in pad shape (top) and round GCDs with multiple gates (bottom) were implemented. The pad shaped GCD is equipped with a guard ring for high voltage operation.

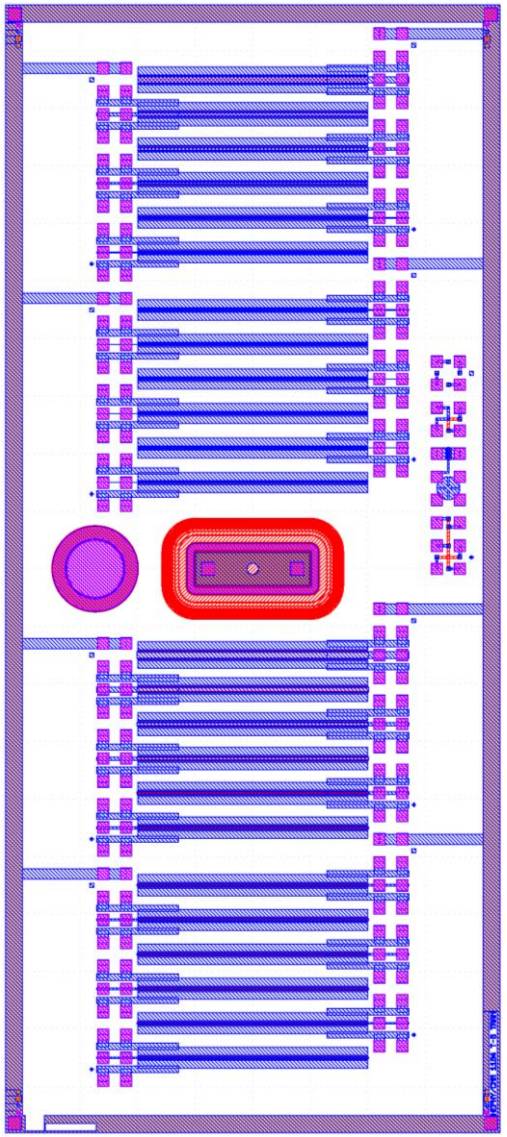


Straight Transistors (T-S)

Straight MOSFET of enhancement mode and depletion mode type. The depletion mode type is expected to never deplete.

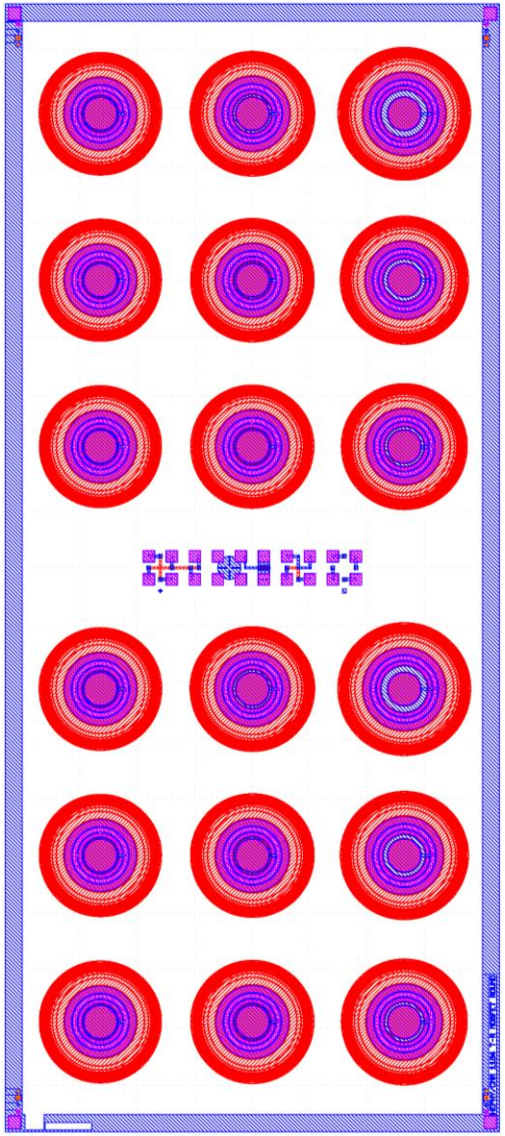
In addition to the MOSFETs a MOSCap, a diode and a process test has been accommodated on the die.

This die is intended for radiation tests and benchmarking of TCAD simulations.



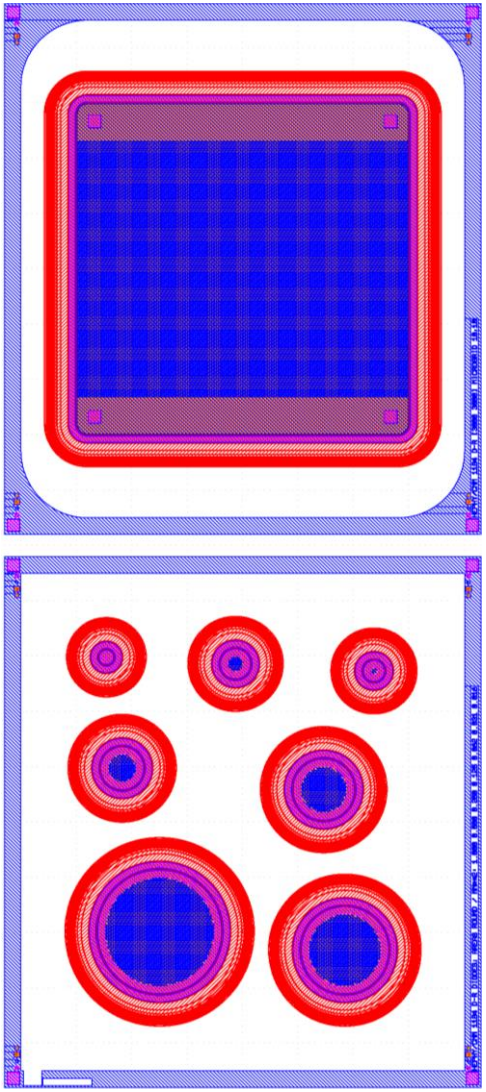
Round Transistors (T-R)

Round MOSFET of enhancement mode and depletion mode type. The depletion mode type is expected to never deplete. The gate contact ring is the outermost ring as there was not enough space for a passivation opening above the actual gate ring.



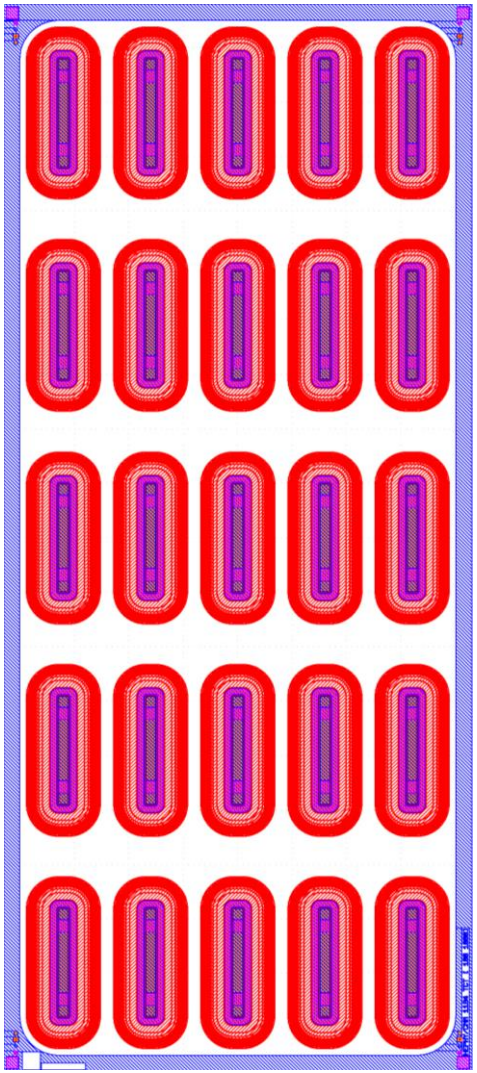
Diode Round (D-R)

Diodes with varying radii, can be used to measure edge effects. Guard rings ensure high-voltage compatibility. A microgrid enables TCT measurements. In the top part a PAD provides a large area diode.



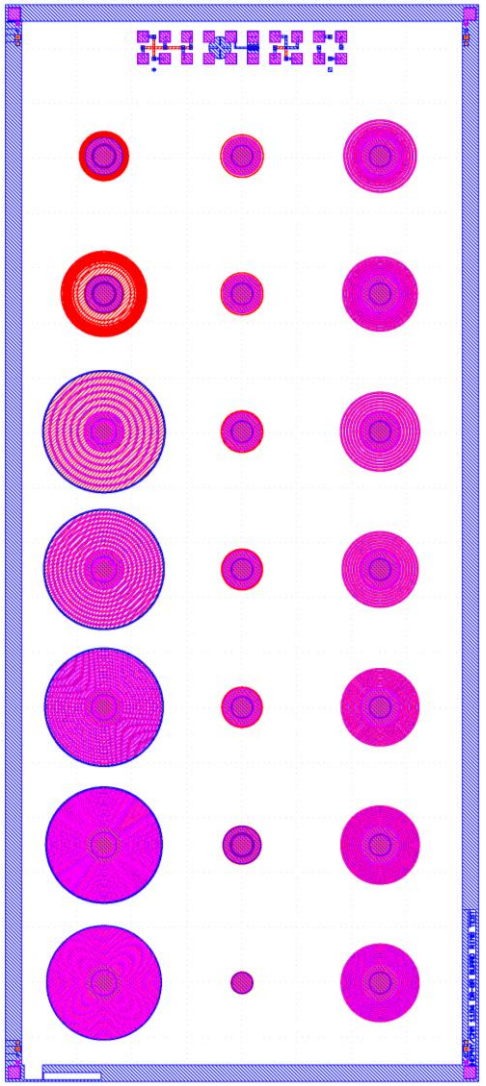
Edge TCT (TCT)

Diodes with guard rings and a small capacitance are arranged in a grid. The die can either be polished or cleaved to obtain a flat surface and a laser can be used for edge TCT.



Guard Ring Test (DR-GR)

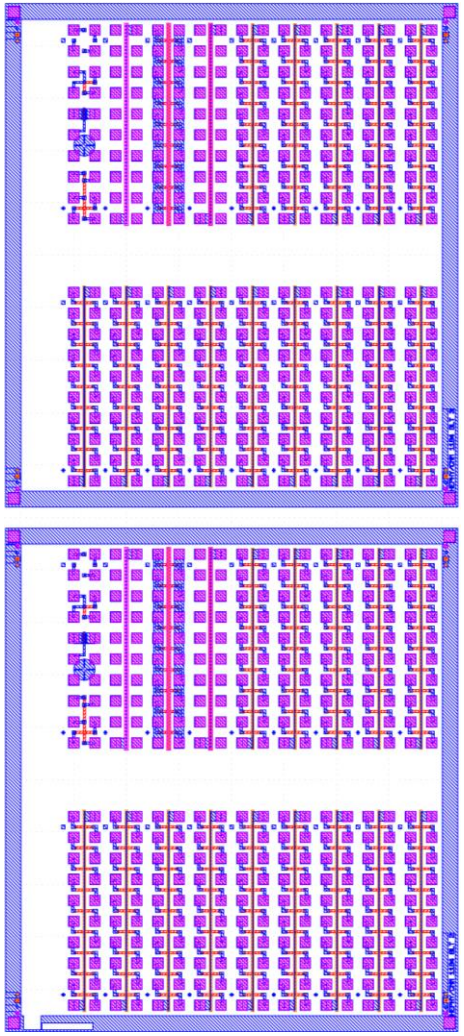
Round diodes surrounded by a variety of guard rings. This structure serves for benchmarking TCAD simulations. The breakdown voltage as well as potentials on guard rings can be measured and compared to simulations.



Gatel length test (GLT1.5, GLT3)

Should enable measurement of the actual gate length of transistors. Two methods are implemented:

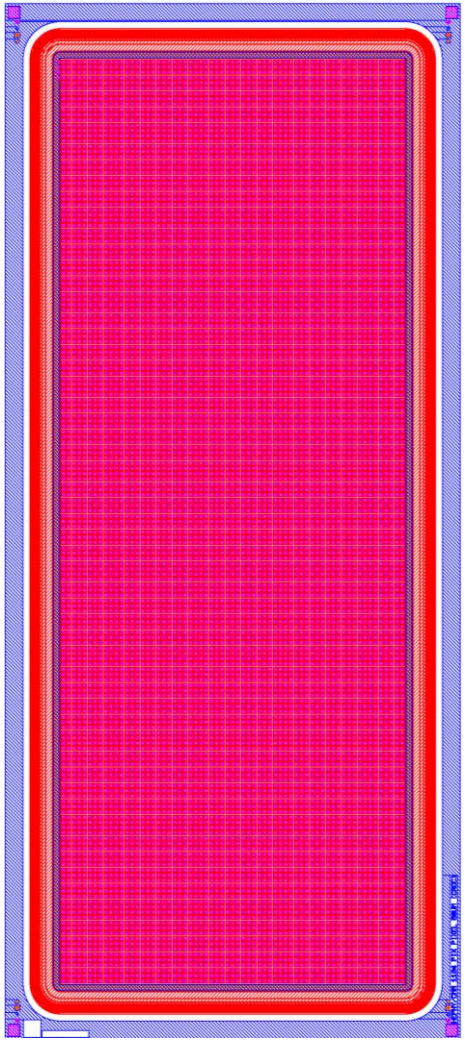
- AFM: A voltage is applied between implant and the substrate. Electric force microscopy (EFM) is used to visualize the electric field.
- P-Metal contacts: the width of a reference metal can be measured, e.g. using a profilometer. The IV curves between the reference metal and P-implants shifting position is measured. The gap between the P-implants can be assessed from the IV curves.



Pixel Array of Diodes (PIX)

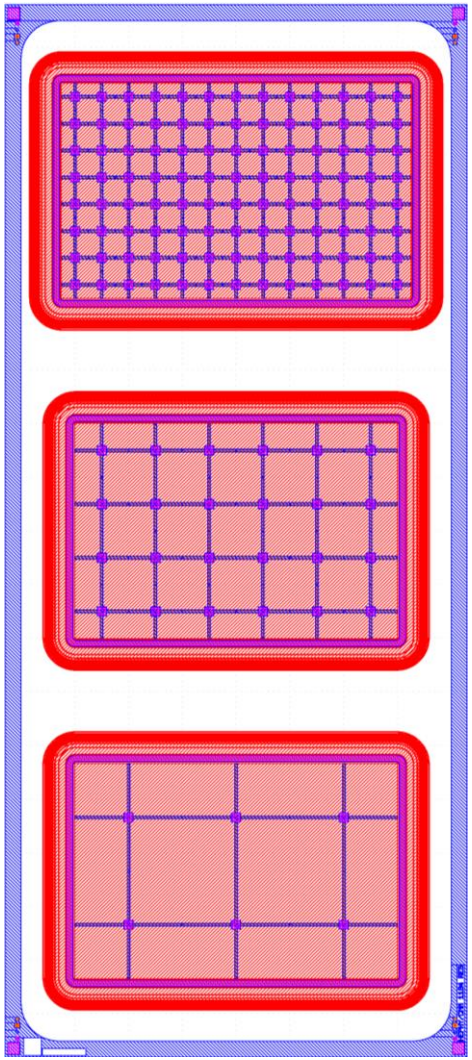
Pixel array of diodes with openings in the passivation for bump bonding.

- PIX-C: The pitch is matched to the CROC chip from CMS
- PIX-M: The pitch is matched to the MPROC chip. This is a KIT development
- Initially thought about Roc4sense, but apparently no chips are available anymore



Resistive Areas (RES)

An array of crosses can be contacted while most of the area is covered only by a P-Implant of high resistivity. From the shapes and arrival times of signals the position of an impinging particle can be deducted.



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Thank you for your attention!