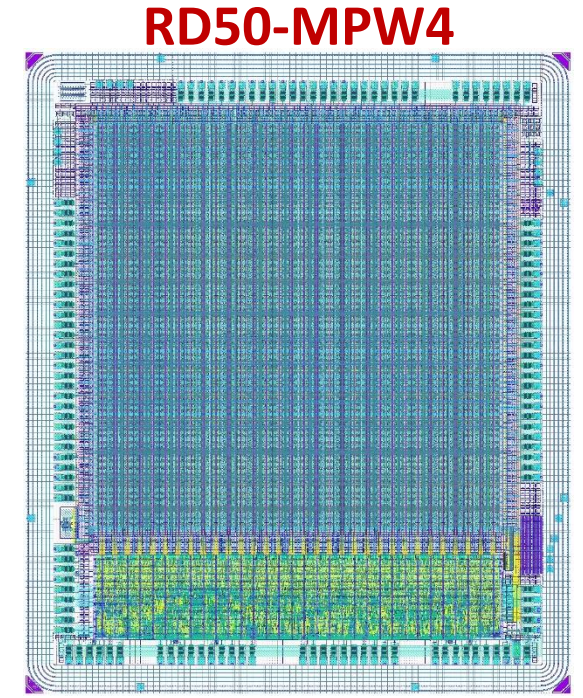
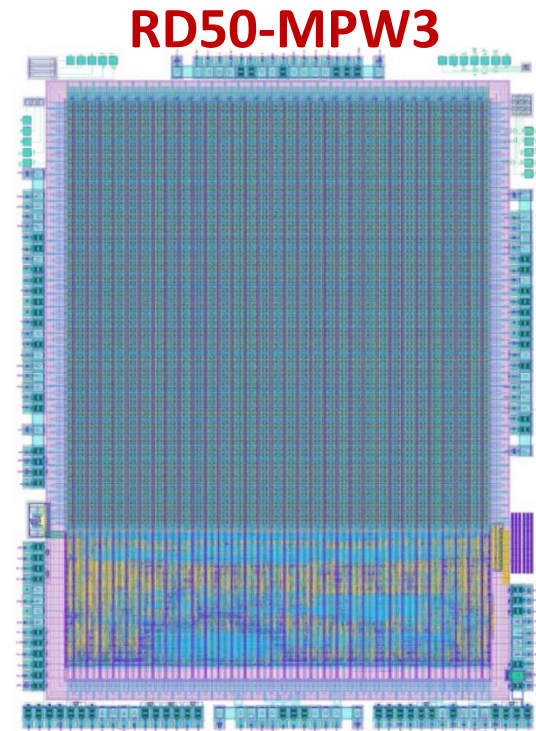
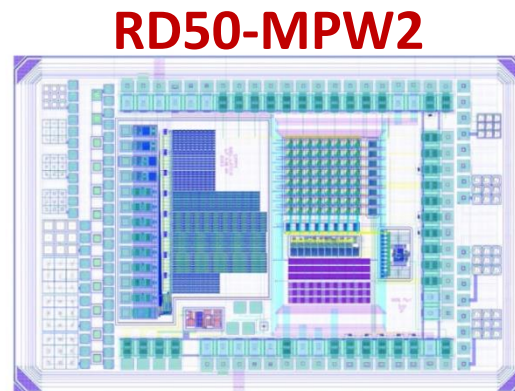
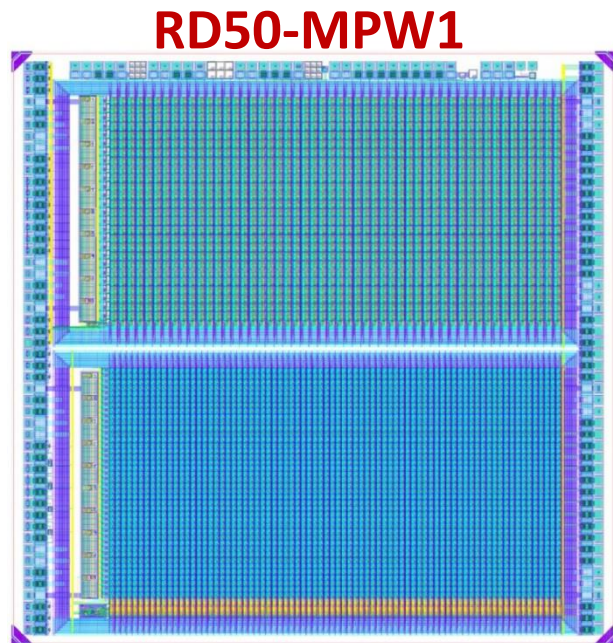


CERN-RD50 – Monolithic CMOS

- R&D programme to study and develop radiation hard High Voltage CMOS sensors for very high luminosity colliders (HL-LHC, FCC)



RD50-MPW3 (*common project 2019-01-RD50*)

■ Irradiation campaign

- 1E14, 2E14, 5E14, 1E15, 2E15 with neutrons (June 2023)
 - Goal is to test the active matrix (lab, test beam) and the test structures (eTCT, TSC)
 - We still have a few irradiated samples available for distribution, and we can irradiate more if people are interested – get in touch with Ljubljana colleagues and/or Eva
- Higher fluence with neutrons (TBD)
- Protons (TBD)

■ Test beams

- CERN (October 2022)
 - Goal was to integrate RD50-MPW3 + Caribou into Mimosa-26/EUDAQ + AIDA2020 TLU
- DESY (July 2023)
 - Goal is to confirm there are no synchronisation issues and test cooling set up, test new piggy boards (produced in 2023) and get data for non-irradiated and irradiated samples

RD50-MPW4 (*common project RD50-2023-02*)

▪ Main submission details

- Submission in May 2023
- Purchased 1 wafer in standard resistivity + 4 wafers in 3 k Ω ·cm
- Delivery of thin and top side biased samples expected in November 2023 (standard + one 3 k Ω ·cm wafers)
- Thinning and backside processing expected in November/December 2023 (two 3 k Ω ·cm wafers)
- Final delivery expected in December 2023

▪ Evaluation

- Electrical tests in the lab (first half of 2024)
- Test beams at CERN and/or DESY (summer 2024?, with non-irradiated samples)
- Irradiation campaign (second half of 2024), expectation is that we will be able to go to higher fluence (1E16?)
- If new collaborators would like to get samples for testing, please get in touch with Eva

RD50-MPW4 – Main goals

- **To fix issues observed in RD50-MPW3**
 - Interface between matrix and periphery
 - We know the solution already (longer pull-down)
 - Easy generation of global time-stamp
 - We know the solution already (64-bit counter in the chip)
 - High noise in lower half of matrix
 - Currently studying this both in simulations and lab measurements
- **To further improve V_{BD} and therefore radiation tolerance too ($V_{BD} > 400\text{ V}$ is possible)**
 - Improve rings around the chip as in test structures in RD50-MPW3
 - Improve HV distribution to the pixels (V_{BD} should not depend on the p/n pixel electrodes spacing any more)
- **To do backside biasing**
 - It is possible with MPW submissions (Liverpool experience with UKRI-MPW0 HV-CMOS chip)