RD50 funding request

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Title of project MPW4 DAQ

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Request to RD50 **24000€**

Total project cost **48000€**

Abstract: We request funding to get the hardware of the Caribou 2.0 DAQ system, the new DAQ standard appropriate for the monolithic detector saga MPWx under development by the RD50 HV-CMOS working group.

Project description

The group RD50 High Voltage CMOS (HV-CMOS) working group is developing a series of MPW chips (Multi Project Wafer) with evolving and improving designs of monolithic pixel particle detectors. The RD50 MPW saga (MPW2, MPW3, MPW4) are mixed signal chips, with increasing amount of digital circuitry. Considering the more advanced designs, see figures 1, 2 (MPW3, fully manufactured, the MPW4 in manufacturing phase), they present an in-pixel digital backend responsible of procesing the analog discriminator output, adjusting the discriminator threshold level, storing time stamps for the rising and trailing edges of discriminator output and a 8bit ROM memory to store the pixel address in its double column (see figure 3).

The digital periphery is the newest design in the MPW3/4. The MPW2 chip presented only a small digital circutry for matrix indexing. The new digital periphery implements full digital readout and configuracion. It is internally connected over a wishbone bus. As in any actual readout chip the MPW3 present a slow control mode and a fast control mode. The slow control is used to configure the ASIC as well to read information about some internal circuits through an I2C link. The fast control mode is responsible of data readout. In any mode the readout responds to digital commands generated by the DAQ system.

To get more details about MPW2 and particularly about the MPW3/4 chips, go to the annex.

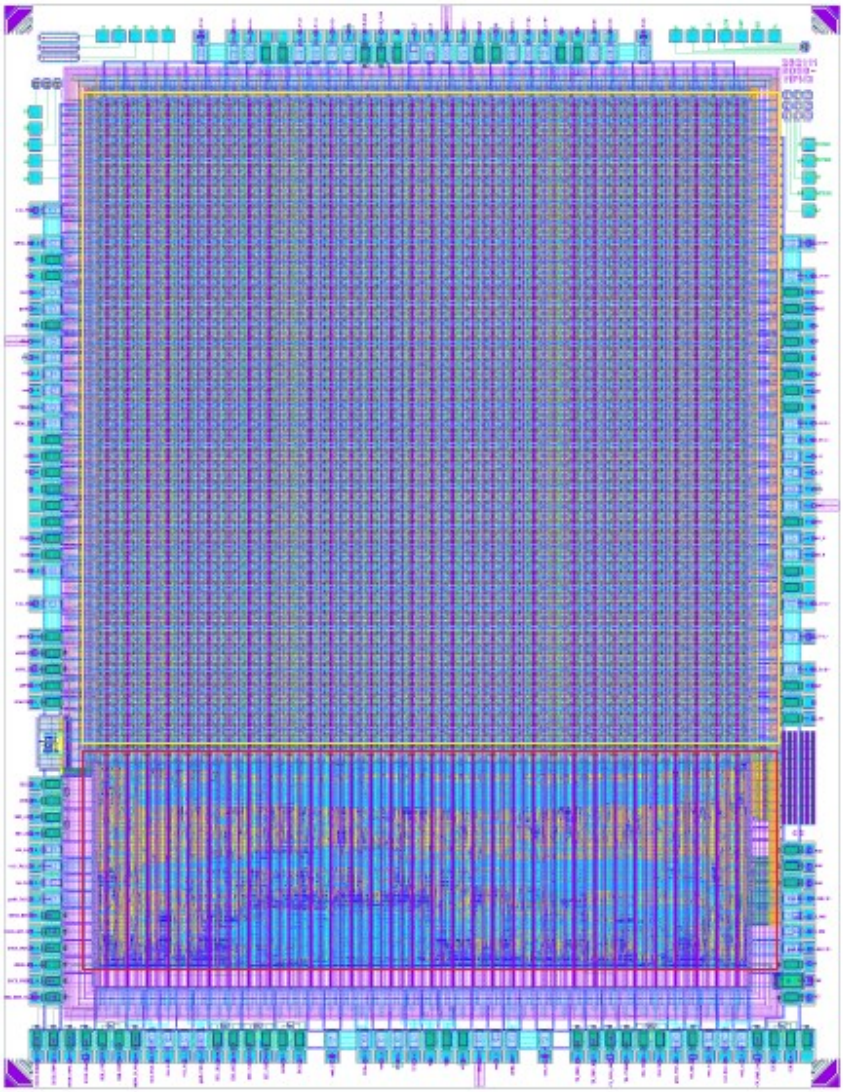

Figure 1: MPW3 mixed signal monolithic pixel detector. Yellow rectangle: pixel matrix. Red rectangle: digital periphery..

The necessity of a DAQ system was clear from the very beginning, in our first MPW2 chip. A monolithic detector is both a pixel matrix and a digital chip because only by digital circuitry, no matter how simple, is possible to address each pixel and proceed to readout. By nature the readout needs a digital configuration. The MPW2 system was comprised of the MPW2 chip, a chipset card (Caribou 1.0) to provide biasing, DAC and digital interfaces, and a full FPGA card, the ZC706. The FPGA card supports a logic design (a controller) responsible of generating commands routed to the monolithic detector, managing the data pipelines to the analyzer end computer and enabling the communication channels (parallel high speed and I2C to the monolithic detector, ethernet to the analyzer end computer).

For the MPW2 system we decided to use a mix of cards. Caribou 1.0 was available and the ZC706 is a commercial development card for the Xilinx Zynq 700 System On Chip FPGA. The full MPW2 system is depicted in figure 4. It is a design operative since 2019.

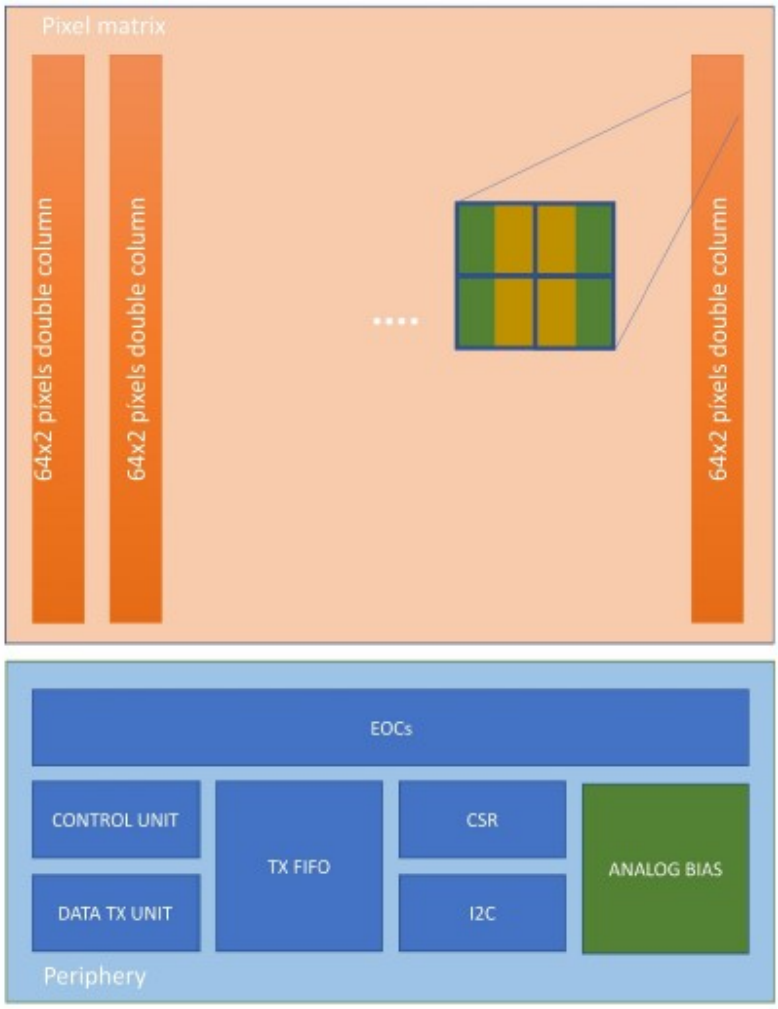

Figure 2: MPW3 Functional Structure: Double column pixel matrix(orange) and IP blocks in the digital periphery (blue)

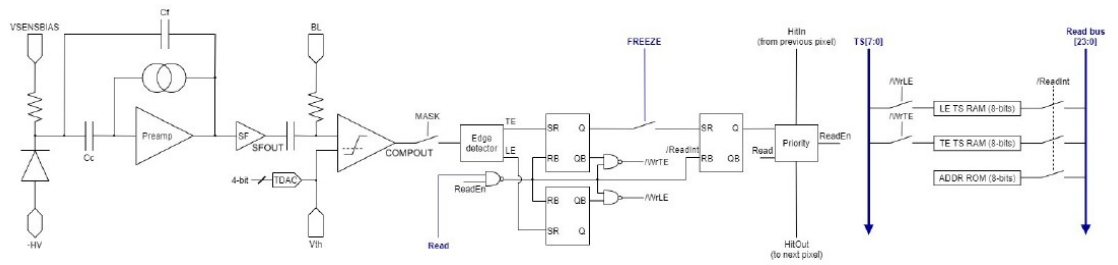

Figure 3: In-pixel electronics block diagram. Behind the comparator comes the pixel digital backend.

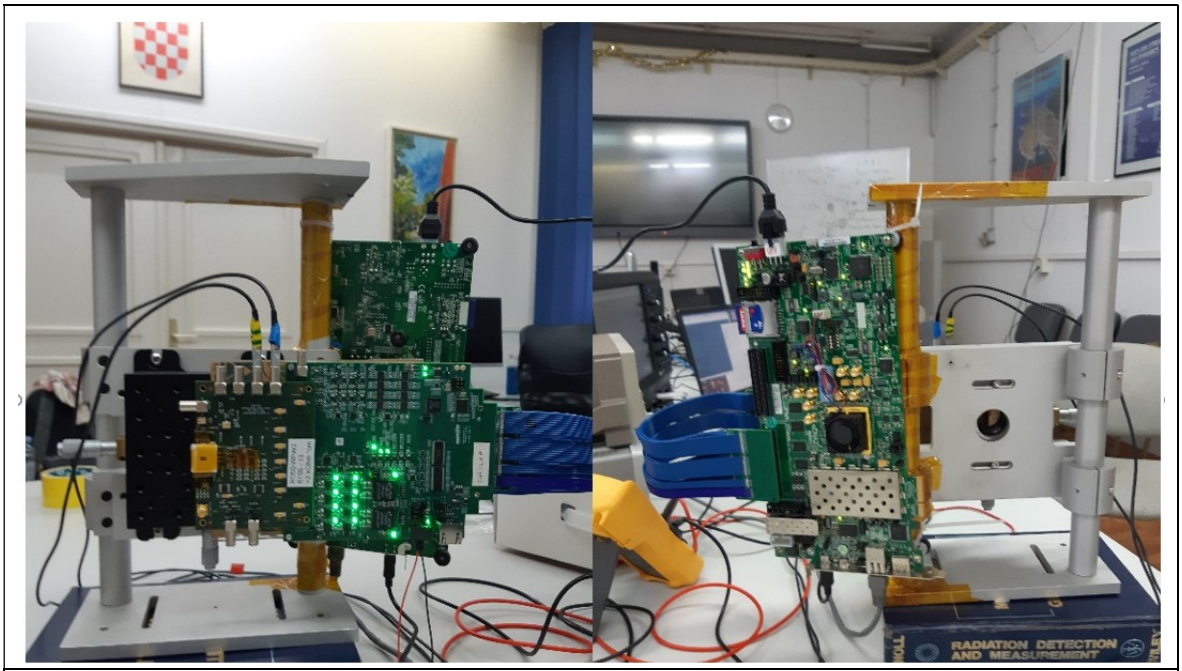

Figure 4: Left: the MPW2 mounted on its PCB is visible (under a white lid), with the Caribou 1.0 chipset card connected to the right (green leds on). Right: the ZC706 control card is shown, connected to the Caribou 1.0 by a blue ribbon cable. The Zynq7000 SoC FPGA is below the black fan.

The MPW3 monolithic pixel detector can re-use the MPW2 DAQ system (Caribou 1.0 plus ZC706 card). However the MPW2 DAQ is showing limitations. The bigger one is also clear from figure 3: it is not a compact DAQ, useful for initial testing but with no robustness for more complex testbeams. It would be a bottleneck very soon considering the evolution of MPW3/4. In the RD50 HV-CMOS working group we agree that we need a new DAQ specifically designed for the monolithic detectors, more robust and more capable. The Caribou 2.0 DAQ toolset operates on one mother card and one insertion module (Mercury XU1 SOM Module) instead of the two cards architecture from legacy Caribou 1.0 + ZC706 DAQ toolset. Simplicity and robustness is the leit motiv.

The new DAQ Caribou 2.0 is also based on the Xilinx Design ToolChain, now using the Xilinx Ultrascale, the evolution of the Xilinx Zynq 7000. The Ultrascale is a System on Module, comprising a Kyntex 7 logic fabric, 2 ARM R5 embedded microcontrollers and 1 Quad ARM A54 microprocessor. The Quad ARM A54 fully runs a Linux OS, useful to get analysis tasks locally (in chip) and to support a client-server architecture to communicate with the end computer. This is a big advantage because on chip several (or even all) analysis tasks can be made instead of in the remote control end computer, gaining speed and compacity. A client-server architecture also simplify the data transfer between the DAQ system and the end computer, up to a level that the end computer can become a simple human interface via a web browser. This also means a bigger simplicity from the point of view of the end user because through web interface tools are standard and everywhere accesible nowadays.

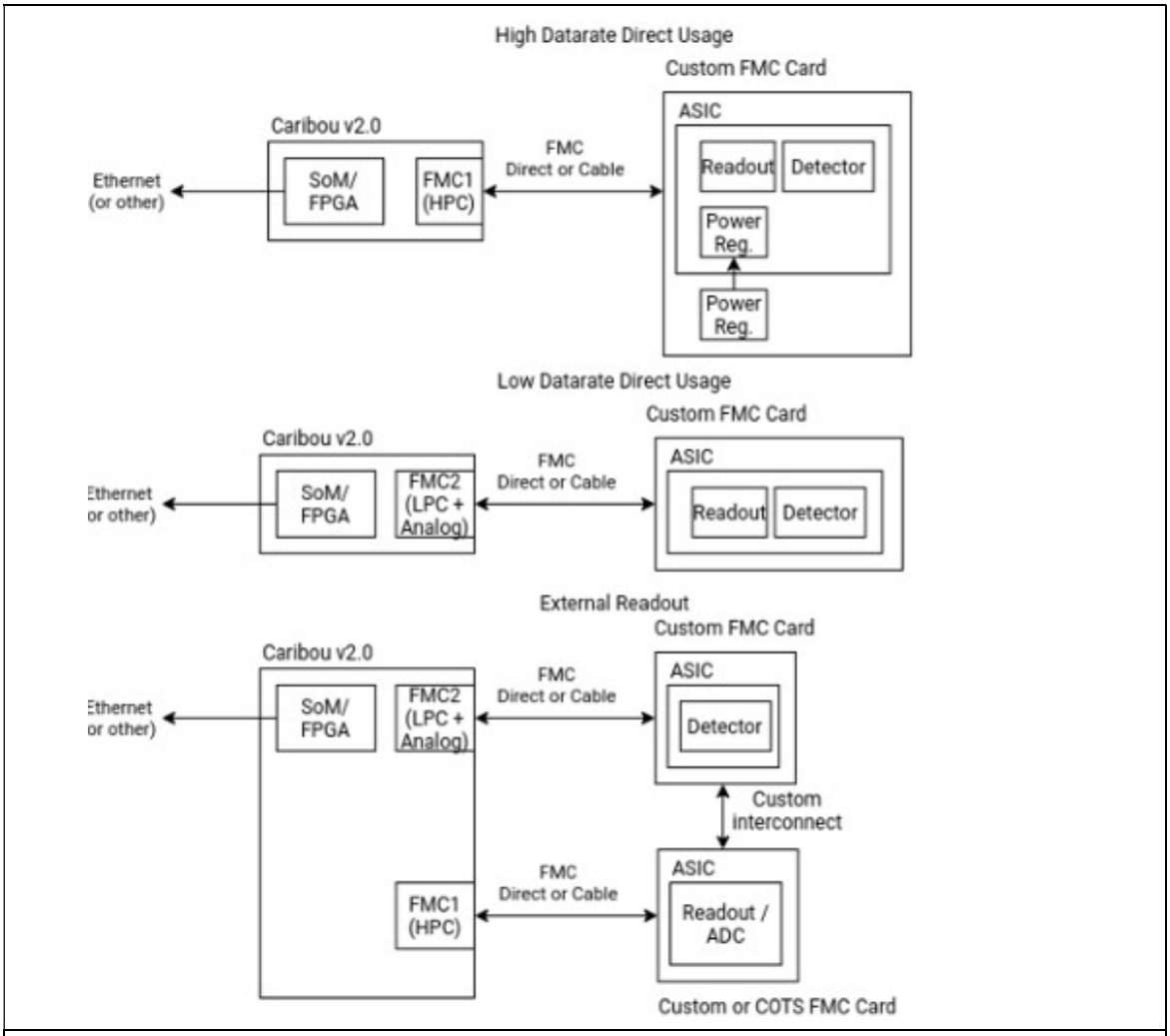

Figure 5: Caribou 2.0 Use cases. Top, high Datarate Direct Usage, Middle, Low Datarate Direct Usage, Bottom, External Readout

The Caribou 2.0 adds also versatility, up to three use cases (see fig 5). On High Datarate Direct configuration the Custom FMC Card supporting the monolithic detector (ASIC) send high throughput dataflow by a HPC (High Pin Count) FMC cable. On Low Datarate Direct usage the dataflow reduces density to use a LPC (Low Pin Count) FMC cable. Finally the External Readout mode combines both. The last configuration is not specific for the MPWx saga but a general one (typical for example in hybrid detectors where the detector pixel die is connected by a bump bonding matrix to a readout ASIC chip). The versatility of the Caribou 2.0 ensures its usability, not limited to the MPWx chips saga.

The new project is a funding request to pay the 50% of the hardware necessary to get the Caribou 2.0 DAQ, nowadays in the final phase of development by the Carleton group.

The tables below show the project costs (see Table 1) considering just one DAQ system for each of the institutes involved. The idea is to have two DAQ systems for each institute (for example as spare) so each institute will pay the full system cost (4k€) for the additional (or spare) Caribou 2.0 DAQ. The project participants are listed in Table 2.

Quantity	Description	Unit price [€]	Net price [€]
6	Caribou 2.0 mother card	1k	6k
6	Mercury ME-XU1-15EG-2I-D12E-G1 Card	2.5k	15k
6	MPW chip card	0.5k	3k
	Total DAQ (unitary) cost	**4k**	**24k**

Table 1 Project costs.

Institute	Caribou 2.0 mother card (€)	Mercury XU1 card(€)	MPW4 card(€)	Contribution [€]
Sevilla	1k	2.5k	0.5k	4k
Carleton	1k	2.5k	0.5k	4k
Liverpool	1k	2.5k	0.5k	4k
HEPHY	1k	2.5k	0.5k	4k
IFIC	1k	2.5k	0.5k	4k
Nikhef	1k	2.5k	0.5k	4k
RD50	6k	15k	3k	24k
Total	12k	30k	6k	**48k**

Table 2 Project costs distribution between the project participants and RD50.

Annex: Details of the MPW3 design.

Following the success of the RD50-MPW2 High Voltage-CMOS (HV-CMOS) pixel chip (common project 2019-01-RD50), the RD50 CMOS Working Group is developing a new prototype, aka RD50-MPW3, which integrates a larger and more advanced pixel matrix with new and optimised peripheral readout electronics to further study these sensors. RD50-MPW3 is in the 150 nm HV-CMOS technology process from LFoundry S.r.l., like its predecessors RD50-MPW1/2 [1], and incorporates all the lessons we have learnt so far.

RD50-MPW2 optimises the sensing diodes and analogue readout electronics [2–4], and includes new structures like a Single Event Upset (SEU) tolerant memory array. We have evaluated this prototype extensively in the lab and at proton and ion beam facilities. The leakage current is 10^{-10} A/pixel (10^{-6} A/pixel in RD50-MPW1), the breakdown voltage 120 V (60 V in RD50-MPW1) and the time resolution less than 10 ns. We have conducted the proton test beams at MedAustron (Austria) and the Rutherford Cancer Centre (United Kingdom) [5, 6], and the ion test beams at the Ruđer Bošković Institute (Croatia) [7]. We have irradiated several samples up to $2x10^{15}$ n_{eq}/cm^2 at TRIGA in Ljubljana, and evaluated the irradiated passive and active pixel matrices with edge Transient Current Technique (eTCT) [6, 8] and radioactive sources. The results obtained, like those for the parameters describing the effective doping concentration as a function of fluence, are compatible with the literature. We have evaluated the sensors with the Two Photon Absorption (TPA) technique. We have developed a dedicated Data Acquisition System (DAQ), for lab and

test beam measurements, which builds on the CaR board [9]. We have published this work in RD50 collaboration meetings, conferences and proceedings papers already, and have a few other publications in preparation. In recent months, several collaborators have joined the RD50 CMOS Working Group, which now involves more than 40 scientists in 15 institutes worldwide. In spite of its undeniable success RD50-MPW2 has several design limitations, such as the small number of rows and columns of the pixel matrix (8 columns x 8 rows), the lack of digital readout electronics to identify particle hits and a very simple peripheral readout that makes certain type of measurements too slow or not possible. To give a specific example of the consequences of these limitations, in RD50-MPW2 only one pixel at a time can be read out and this has seriously restricted our studies.

RD50-MPW3 overcomes the limitations of RD50-MPW2 by extending the number of pixels in the matrix (64 columns x 64 rows), incorporating in the pixel area digital readout electronics based on the well-known column drain architecture (i.e. FE-I3 style) and adding optimised peripheral readout electronics for effective pixel configuration and fast data transmission [10]. The RD50-MPW3 in-pixel digital readout is a highly improved version of that we developed for RD50-MPW1 [11]. We have incorporated logic to mask noisy pixels, replaced the priority circuit that referees the order in which hits are read out for a less area-consuming alternative, and allowed pausing the digitisation of new hits until the readout of a column is complete. To prevent the generation of crosstalk, which we observed in RD50-MPW1, we have added one metal routing line connected to ground between every two long metal routing lines that carry fast digital signals. Each pixel contains a new 8-bit SRAM shift register, which enables serial configuration and stores a per pixel-trimming to compensate for threshold voltage variations (four bits), a flag to mask noisy pixels (one bit), and values to enable or disable the calibration circuit (one bit), the amplifier output monitor (one bit) and the comparator output monitor (one bit). The analogue readout electronics reuse those we developed for RD50-MPW2, as the lab and test beam evaluations concluded their performance is satisfactory. We have separated the analogue and digital grounds of the pixel, with a trench, to avoid noise coupling between the analogue and digital domains. The pixel size in RD50-MPW3 is 62 µm x 62 µm. This represents a small increase of the pixel size in RD50-MPW2 (60 µm x 60 µm), however it is necessary to accommodate all the new features here described while maintaining the breakdown voltage we achieved in our previous prototype (8 µm spacing between the p- and n-type electrodes of the diode for a 120 V breakdown voltage).

RD50-MPW3 implements a double column scheme for the first time in the RD50-MPWx prototypes, which together with the also new 8-bit SRAM shift register for serial configuration, alleviates the routing congestion and facilitates means to minimise the crosstalk. The double column scheme almost halves the number of metal routing lines, as the pixels within a double column share most of the many metal routing lines they require. To enable that, the layout of the pixels is horizontally mirrored in every double column (i.e. analogue readout on one side and digital readout on the other side for one of the two columns, and vice versa for the other). To avoid voltage drops across the pixel matrix, we have distributed the power using a grid of wide metal lines in the highest possible metal layers. The power scheme assumes pads are located on the four edges of

the chip. Although this is not ideal for a sensor, we consider it is acceptable for R&D purposes.

The peripheral electronics, which configure the pixels and control the data readout, consist of new and optimised End Of Column (EOC) circuits and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus.

The EOCs use a First Input First Output (FIFO) memory to store, temporarily, the data generated by the pixels within a double column (i.e. leading and trailing edge time-stamps, and pixel address). This reduces the dead time, as pixels with hits are read out immediately as long as the FIFO is not full. The generated data is packed into frames, zero-suppressed and serialised at a maximum rate of 640 Mb/s over Low Voltage Differential Signal (LVDS) lines. To facilitate data transmission, we have implemented 8b/10b Aurora encoding. To assure fast and reliable synchronisation and communication with the readout FPGA, we send an idle pattern when there is no data present. RD50-MPW3 includes as well a few dedicated test structures, mostly to characterise the diode I-V, depletion region and parasitic capacitance, and a bandgap voltage reference.

References

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