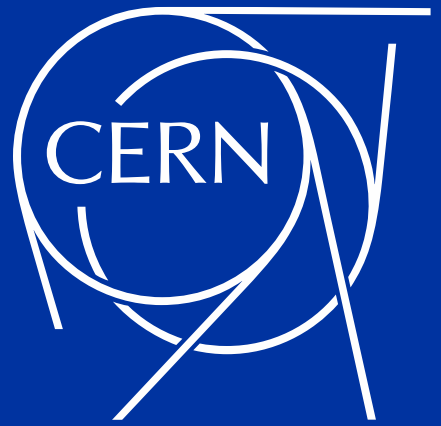


MCF Topical Meeting #51
HL-LHC Magnet Circuit Instrumentation Day 2023

Power Interlock Controller Loops, System Tests and Commissioning

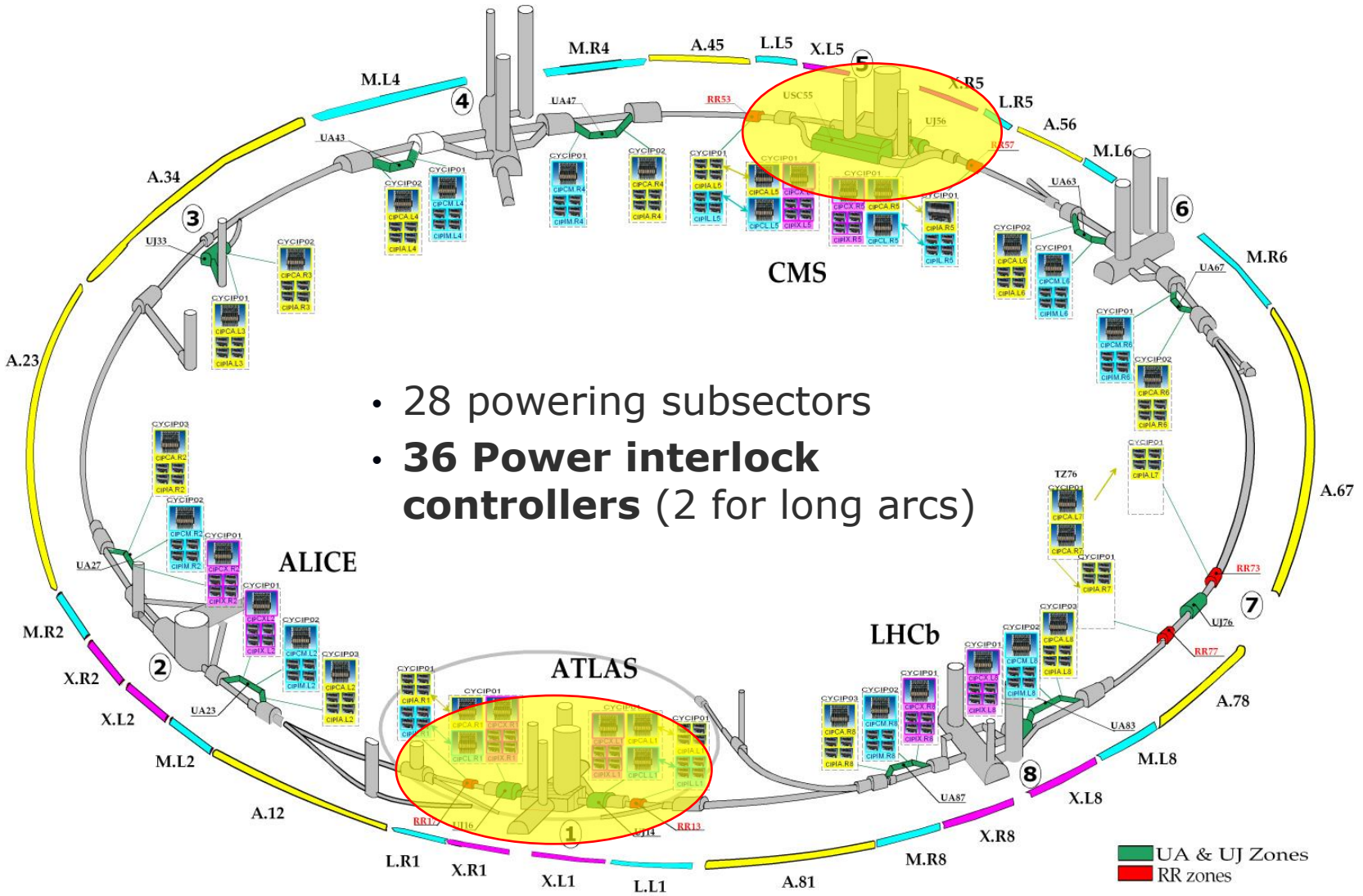
Alain Antoine (TE-MPE-MI)

20 June 2023

OUTLINE

- **INTRODUCTION TO PIC**
- **HL-LHC SPECIFICATIONS for PIC**
- **SECOND GENERATION OF PIC**
- **IST AND COMMISSIONING**
- **CONCLUSIONS**

Introduction



- 28 powering subsectors
- **36 Power interlock controllers** (2 for long arcs)

PIC is designed to:

- **Ensure the correct powering conditions for the superconducting magnet circuits of the LHC.**
- **Request a beam dump via the Beam Interlock System in case of failure of a connected circuits.**
- **A total of 12 out of 36 PICs are located at point 1 and 5.**

HL-LHC Specifications for PIC

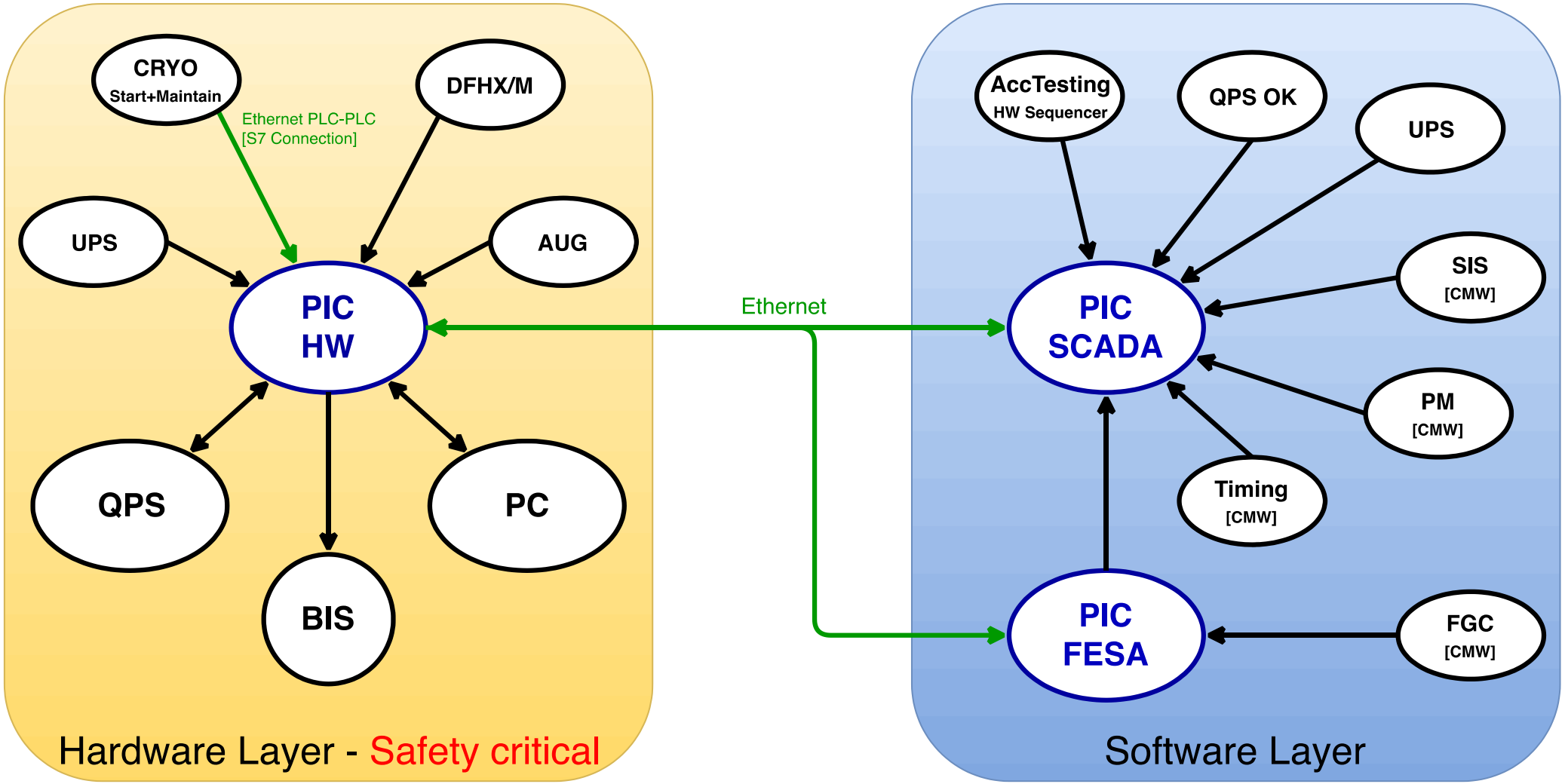
HL-LHC Specifications for PIC

- **Relocation of the 12 PICs of the sectors 1 and 5:**
  - from UL14, UL16 to UR15,
  - from USC55, UL557 to UR55.
- **Moving the electronics from the RRs to the URs to cope with the predicted increase in radiation levels induced by future HL-LHC beams.**
- **New configuration of the PICs of the inner triplet regions and matching sections in point 1 & 5.**
- **New interface at point 1 and 5 for HL-LHC circuits: DFHX/M thermal switches for the inner triplet and matching sections**
- **<u>Note:</u> PIC is ready for the 11T magnet integration**

	Circuits for HiLumi	Magnet Type	Circuit Name	Number of circuits per IP side	Total number of circuits	I_nominal (7 TeV) [kA]	I_ultimate [kA]	L per circuit at nominal current [mH]	R per circuit [mΩ]	Comments or References
Inner Triplet	Triplet Q1, Q2a, Q2b, Q3	MQXFA / MQFXB	RQX	1	4 (IR1/5)	16,23	17,5	255,4	0,15	CERN-ACC-2017-0101; EDMS 1375861
	Trim Q1	-	RTQX1	1	4 (IR1/5)	2	2	69	1,35	
	Trim Q1a	-	RTQXA1	1	4 (IR1/5)	0,035	0,035	34,5	226,16	
	Trim Q3	-	RTQX3	1	4 (IR1/5)	2	2	69	1,2	
	Orbit correctors Q1/2 - Horizontal/Inner	MCBXFB	RCBXH[1,2]	2	8 (IR1/5)	1,74	1,864	58,4	2,37	
	Orbit correctors Q1/2 - Vertical/Outer	MCBXFB	RCBXV[1,2]	2	8 (IR1/5)	1,43	1,532	124,8	2,42	
	Orbit correctors Q3 - Horizontal/Inner	MCBXFA	RCBXH3	1	4 (IR1/5)	1,593	1,709	107,1	1,99	
	Orbit correctors Q3 - Vertical/Outer	MCBXFA	RCBXV3	1	4 (IR1/5)	1,34	1,441	232,3	1,98	
	Superferric, order 2	MQSXF	RQSX3	1	4 (IR1/5)	0,174	0,197	1530	14,31	
	Superferric, order 3, normal and skew	MCSXF / MCSSXF	RCS[S]X3	2	8 (IR1/5)	0,099	0,112	213	54	
	Superferric, order 4, normal and skew	MCOXF / MCOSXF	RCO[S]X3	2	8 (IR1/5)	0,102	0,115	220	54	
	Superferric, order 5, normal and skew	MCDXF / MCDSXF	RCD[S]X3	2	8 (IR1/5)	0,092	0,106	120	54	
	Superferric, order 6	MCTXF	RCTX3	1	4 (IR1/5)	0,085	0,097	805	54	
	Superferric, order 6, skew	MCTSXF	RCTSX3	1	4 (IR1/5)	0,084	0,094	177	54	
D1	Separation dipole D1	MBXF	RD1	1	4 (IR1/5)	12,11	13,231	24,84	0,31	
D2	Recombination dipole D2	MBRD	RD2	1	4 (IR1/5)	12,33	13,343	27,46	0,13	
	Orbit correctors D2	MCBRD	RCBRD[V,H]4	4	16 (IR1/5)	0,394	0,422	920	1,36	
Q4	Individually powered quad Q4 (4.5K)	MQY	Same Circuit Paramters for Q4 in IR1/5 as in the LHC, Correction Plane Swapped by Turning and Swaping of Q4 Magnets							ECR EDMS no. 2083813
	Orbit correctors Q4 (4.5K)	MCBY								
Q5	Individually powered quad Q5 (4.5K)	MQML	Same Circuit Paramters for Q5, Q6 and Correctors in IR1/5 as in the LHC							
	Orbit correctors Q5 (4.5K)	MCBC								
Q6	Individually powered quad Q6 (4.5K)	MQML								
	Orbit correctors Q6 (4.5K)	MCBC								
Q10	Individually powered quad Q10 (1.9K)	MQML	RQ10	2	8 (IR1/5)	5,39	5,83	21	0,4	ECR EDMS no. 2796793
	Orbit correctors Q10 (1.9K)	MCB	RCB[V,H]10	2	8 (IR1/5)	0,055	0,06	6020	45,8	
	Lattice Sextupole (1.9K)	MS	RS[D,F][1,2]	2	8 (IR1/5)	0,55	0,6	432	7,5	
Q5	Individually powered quad Q5 (4.5K)	MQY	RQ5	2	4 (IR6)	3,61	3,9	74	0,4	
	Orbit correctors Q5 (4.5K)	MCBY	RCBY[V,H]5	2	4 (IR6)	0,088	0,1	5270	34,4	
11T	11T dipole, MBH	11T dipole, MBH	RB.A67-RB.A78	-	2 (IR7)	11,85	12,798	15734	1	
	Trim circuit	-	RTBH9	-	2 (IR7)	0,25	0,25	127,1	30,96	

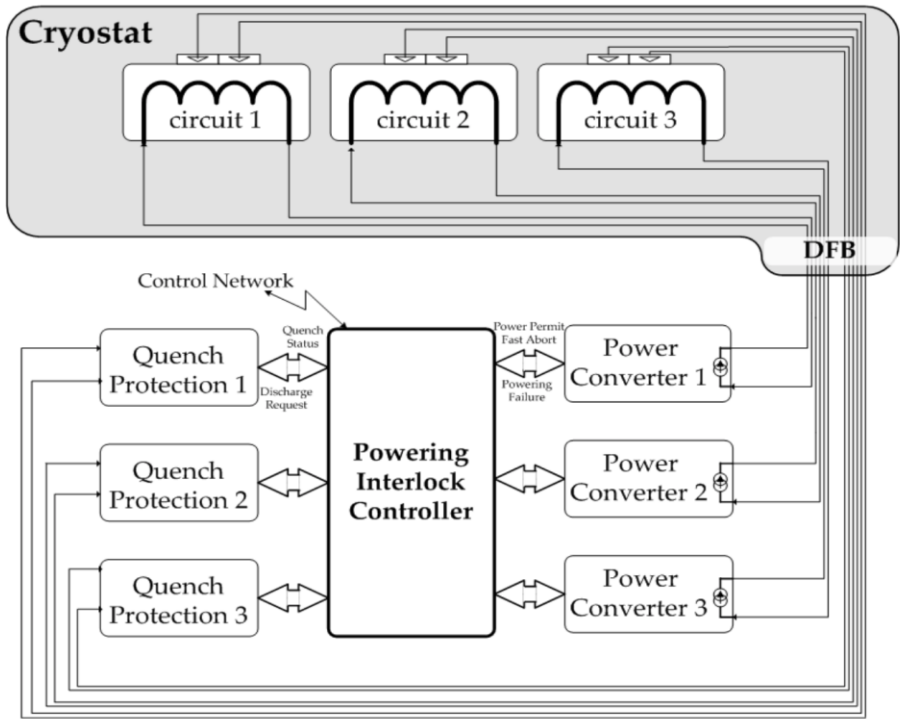
Second Generation of PIC (PICv2)

Interface overview



Circuit Interlock Types

Up to 54 circuits / PIC



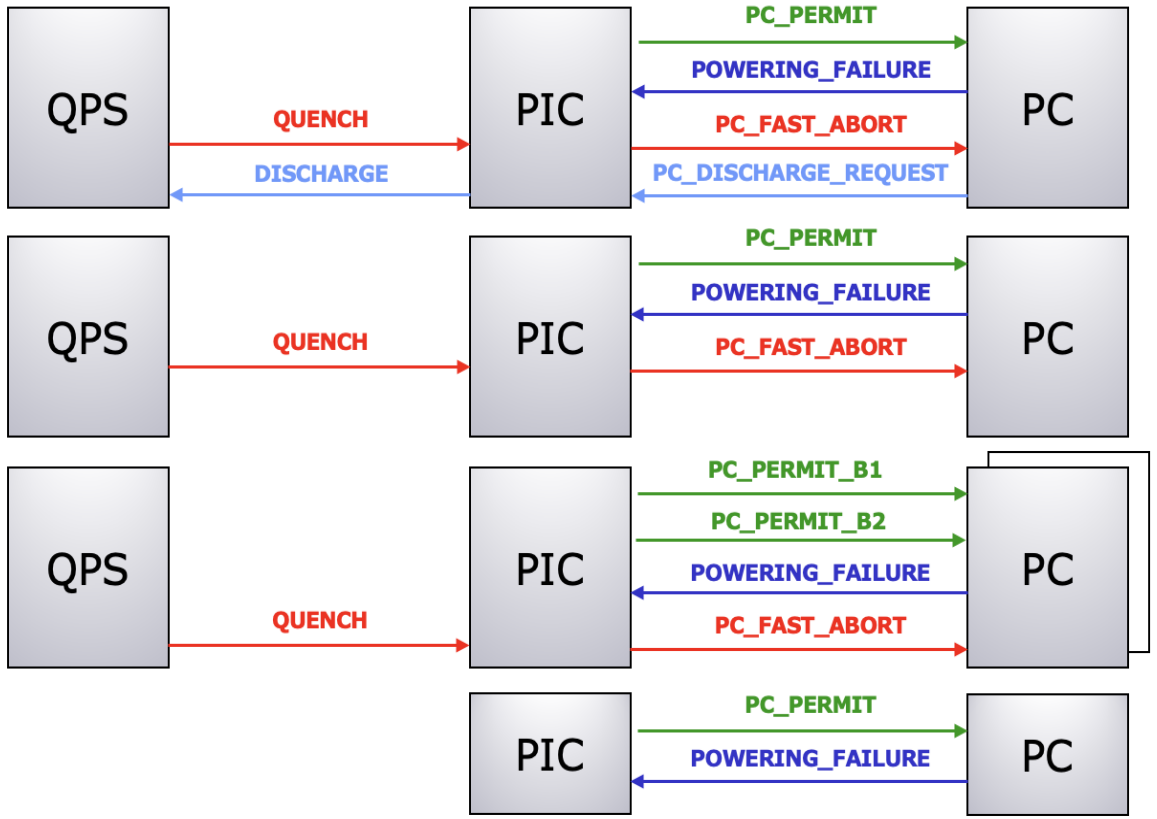
Interlock Type A
13kA main + IT

Interlock Type B1
600A EE, 600A no EE, 600A no EE crowbar + Individually powered dipoles.

Interlock Type B2
Individually powered quadrupoles (IRs)

Interlock Type C1/C2
80-120A correctors

Interlock Type D
60A dipole orbit correctors

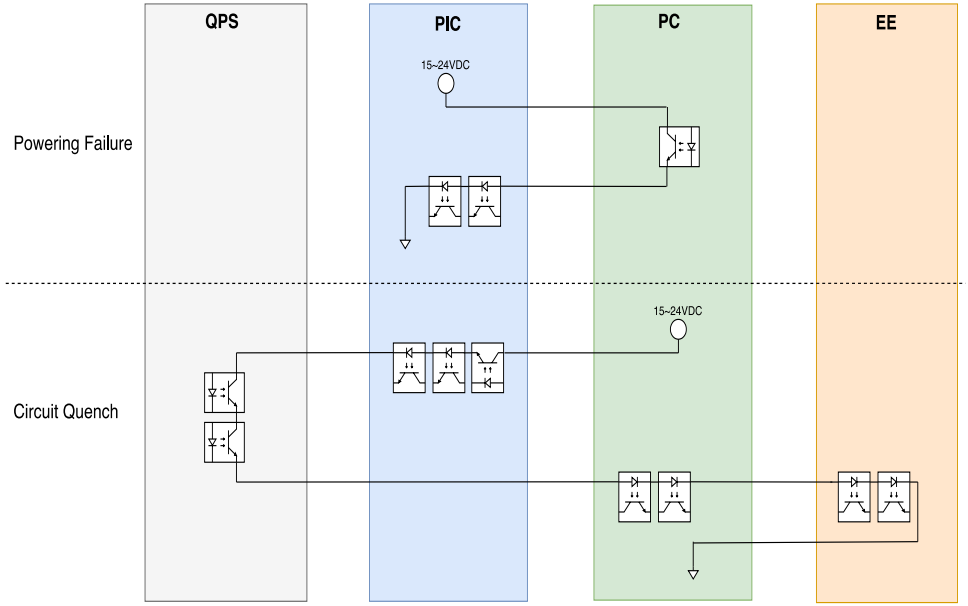


No HW interlocks, but PC PERMIT of the PC via timing system, surveillance through SIS

Second Generation of PIC

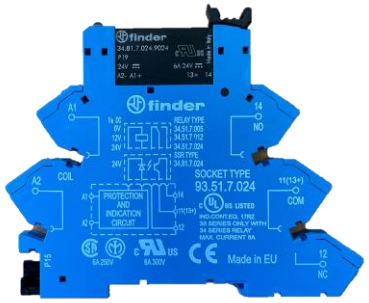
- **Why?**
  - Extend the lifespan of the PIC systems beyond HL-LHC by addressing the obsolescence of critical components in the system design.
  - Assure compatibility with HL-LHC protection requirements.
- **Design**
  - A purely industrial solution prototype based on PLC is available (HW) and will be installed at IT-STRING.
  - Redesign of the PLC, WinCC software by BE-ICS using UNICOS is in progress and should be available by end of June.

- **Reliability studies Outcome**
  - Redundant reading of the loops.
  - Beam dump request redundancy ensured by an extra CPU.
  - Study ongoing
    - Possibility of reducing the number of CPUs per LHC sector to 2, to avoid the exchange of hardware signals between the PICs.

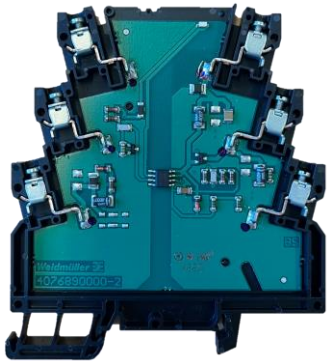


Current loops

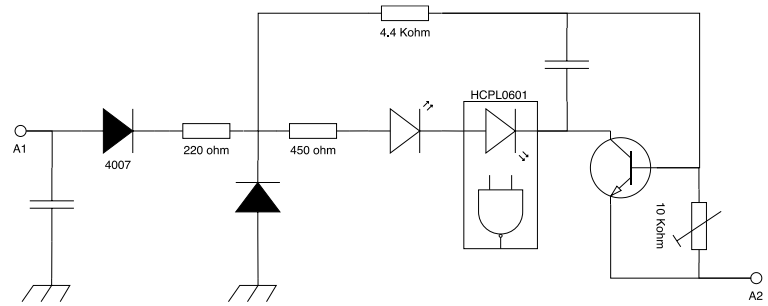
Finder



Weidmüller

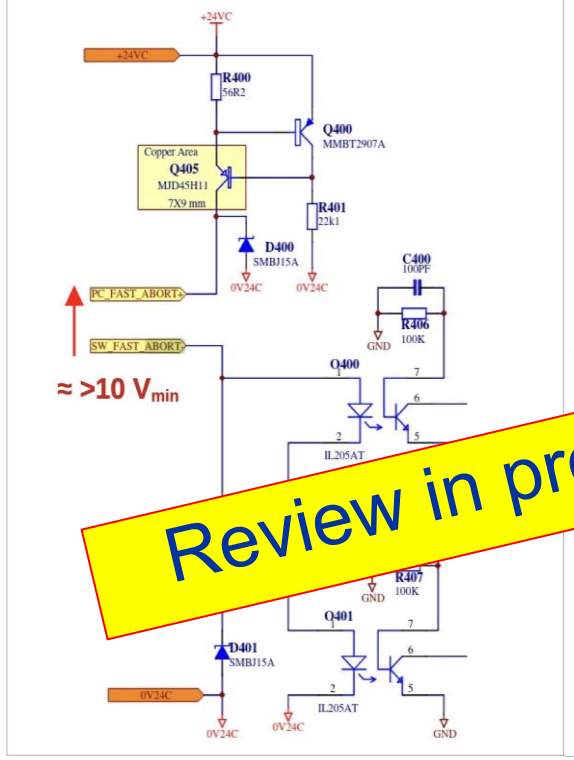


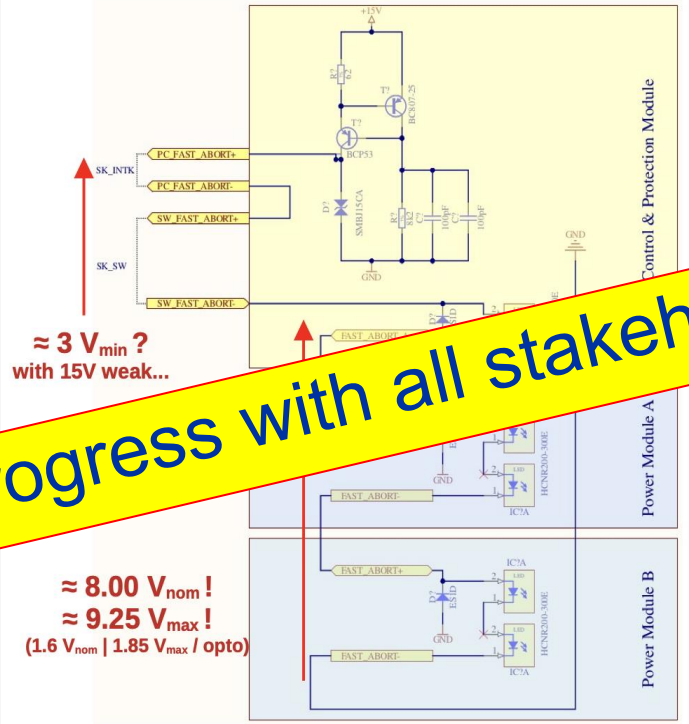
- **The new design of the PICv2 highlighted the potential risk of degradation of the integrity of the Quench loop induced by the voltage drops produced by all the systems.**
- **LHC specifications (EDMS 1001985) for current loops:**
  - 10 mA < I < 20 mA and 15 V < V < 24 V
  - Maximum allowed **voltage drop of each system is 2.5 V.**
- **PICv2 Prototype**
  - Preliminary studies to select the components have focused on the reaction time (<75us for CLIQ integration) :
    - Opto-coupler to write on the loops: Finder 24 VDC.
    - Opto-coupler to read on the loops: Weidmüller MOS 12-28 VDC.
    - ***2x 4.2 VDC optocoupler voltage drop*** is caused by internal protection against reverse current, over voltage and short circuit.
    - CLIQ is out of the picture: reaction time restrained to 10 ms -> wider opto-coupler choice.
  - ***HW validated in MPE testbed 272*** and in the PIC testbed:
    - Power Permit loop with FGC ☑
    - Powering Failure loop with FGC ☑
    - Quench loop with FGC and CLIQ (No EE) ☑

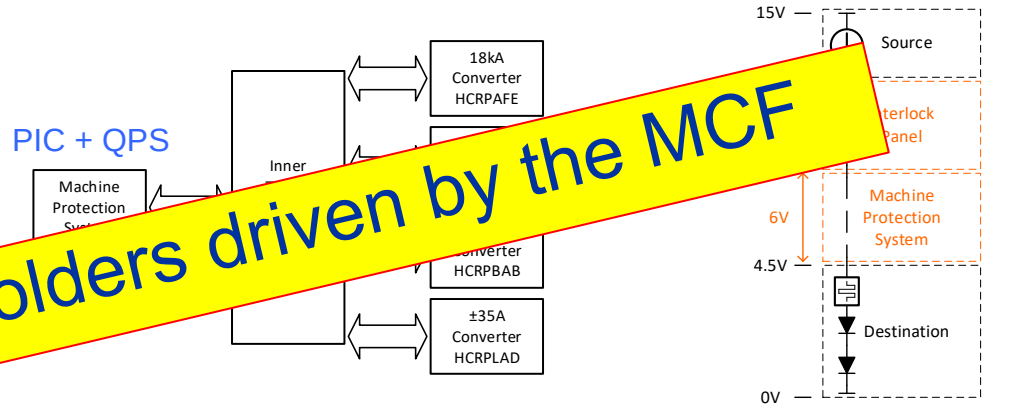


Quench Loop: different cases…

LHC600A-10V	R2E-LHC600A-10V	Inner Triplet
EDMS 970040 - page 99	EDMS 2350138 - doc	EDMS XXXX - page X







Between source and destination:

- Each **optocoupler** has a forward voltage
- Each **fuse** has a forward voltage

The loop powering is 15V, with a current regulator which needs 2.5V
The loop readout can be redundant, with a fuse, which needs 4.5V

So there is around 8V for interface panel + MPS

2V for the interlock panel, and 6V for the machine protection system.

Review in progress with all stakeholders driven by the MCF

Courtesy of Y. Thurel and B. Todd

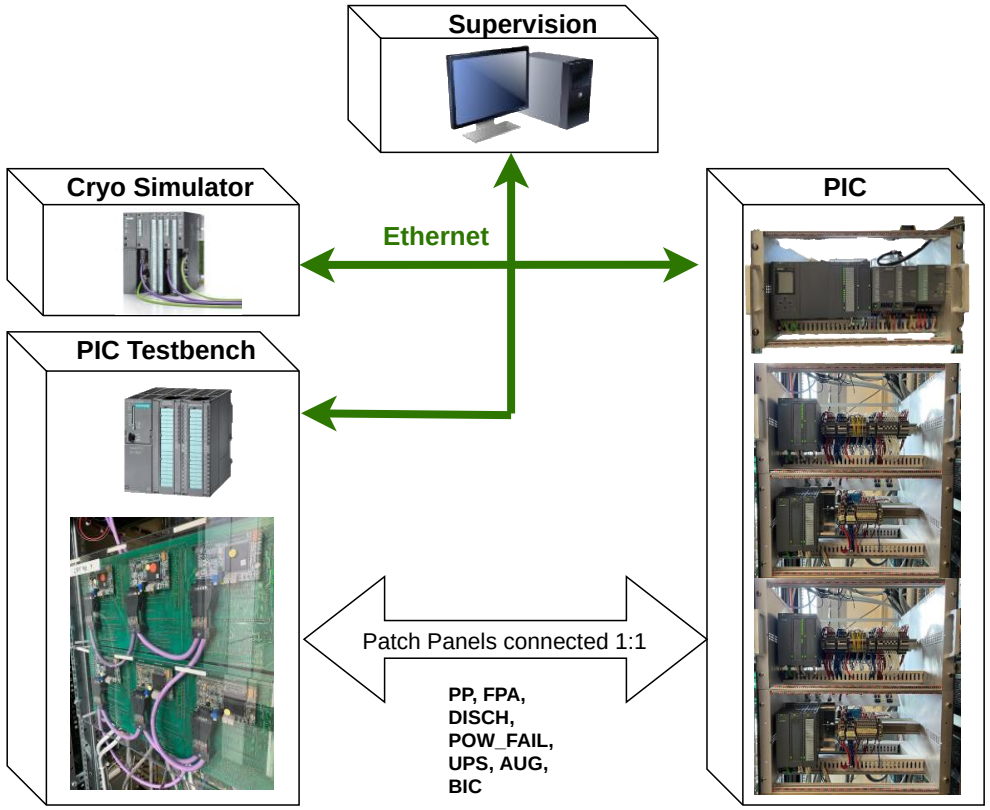
IST & HWC

Reference Documents

- **General Procedure for the Commissioning of the Electrical Circuits of a sector (Eng. Spec.)**
  - EDMS 477145: LHC-D-HCP-0001
- **Individual System Tests of the Powering Interlock Controller**
  - EDMS 531823: LHC-CI-TP-0001
- **MPS Aspects of the Power Interlock System Commissioning**
  - EDMS 896390: LHC-OP-MPS-0005
- **Interlock Tests of Powering Subsector Prior & After Connection of the Power Cables to DFB Leads**
  - EDMS 519704: LHC-D-HCP-0002

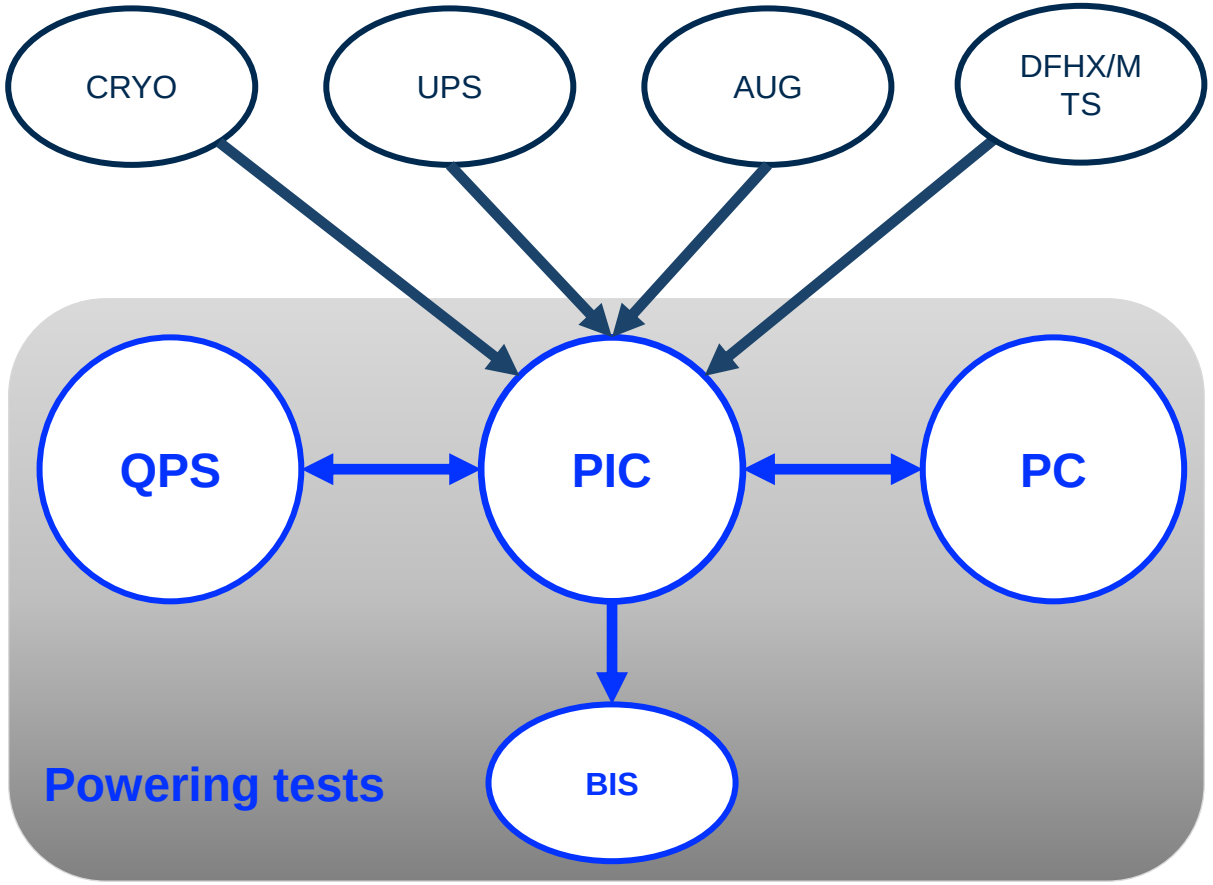
Individual System Tests

- **To validate the correct functioning of the PIC, including the supervision application in stand-alone mode.**
- **2 steps:**
  - Prior to the installation of a PIC in the LHC:
    - A **dedicated test system** is used to interface any existing PIC hardware configuration and to simulate all protection signals.
    - An **automated procedure** verifies the correct response of the powering interlock controller for all possible failure scenarios simulated with the test system (validation of PLC HW + SW).
  - In-situ (proposal to be tested at IT-STRING):
    - The PIC is entirely cabled but all systems are disconnected and replaced by dedicated “bouchon”.



Hardware Commissioning

- **12 out of 36 PIC are to be tested for HL-LHC.**
- **Tests entirely carried out manually (with the concerned teams).**
  - CRYO
    - Tests and validation from the CCC.
  - UPS
    - Validation in collaboration with EN/EL team which acts on the UPS in the tunnel.
  - AUG
    - Analysis of all events in the PIC history buffer.
  - DFHX/M Thermal switches.
    - Interface and configuration.
- **Automated tests via AccTesting.**
  - Powering tests.

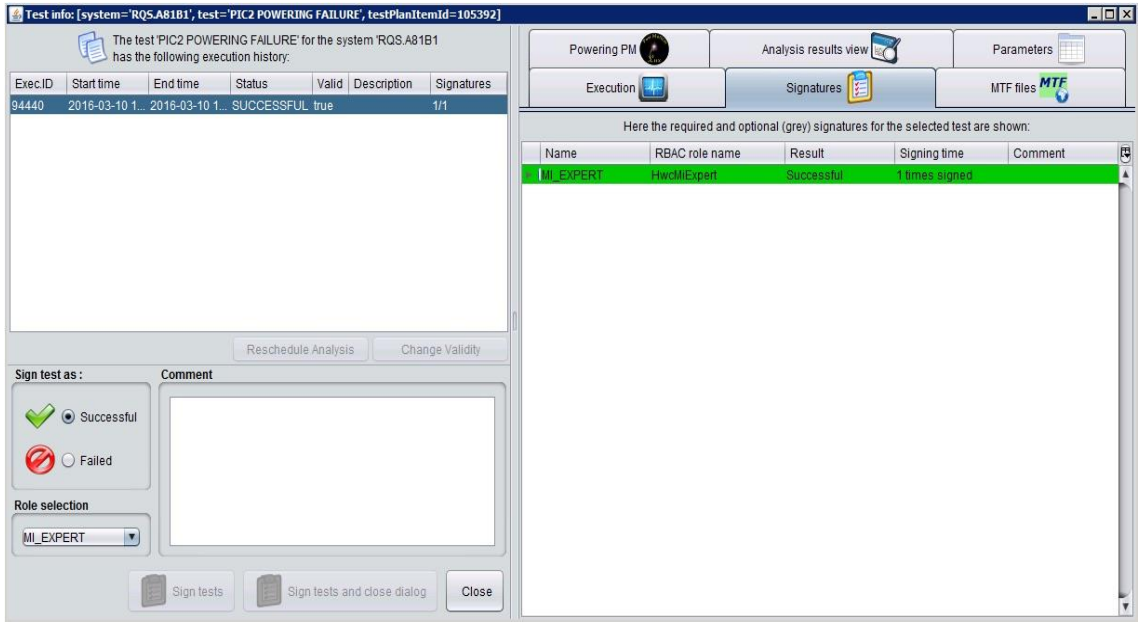


Powering Tests

Test Procedure in [EDMS 519704.]

The aim is the commissioning of hardwired protection signals, transmitted via current loops in between the involved systems (PC_PERMIT, POW_FAIL, QUENCH, DISCHARGE_REQ, BIS).

Test management with AccTesting (MPE-CB).



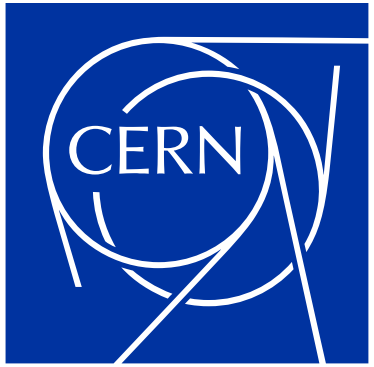
Powering Tests (2)

Test	Interlock Type	Circuit Type	PIC Signature
PC_PERMIT	A, B1, B2, C	All	Not required
POWER FAILURE	A(1)	RB	PIC Expert
	A(2), B1, B2, C	Others	Automatic (eDSL)
CIRCUIT QUENCH VIA QPS	A, B1	RB, RQD, RQF, RQX, IPD	PIC Expert
	B1, B2	600A EE/noEE	Automatic (eDSL)
FAST ABORT VIA PIC	A, B1	RB, RQD, RQF, RQX, IPD	PIC Expert
	B1, B2	600A EE/noEE	Automatic (eDSL)
DISCHARGE REQ VIA PIC	A	RB, RQD, RQF	PIC Expert
PIC TO BIC	All	All	PIC Expert

HL-LHC: 88 PIC tests / IP Side (+31 PIC to BIC tests).

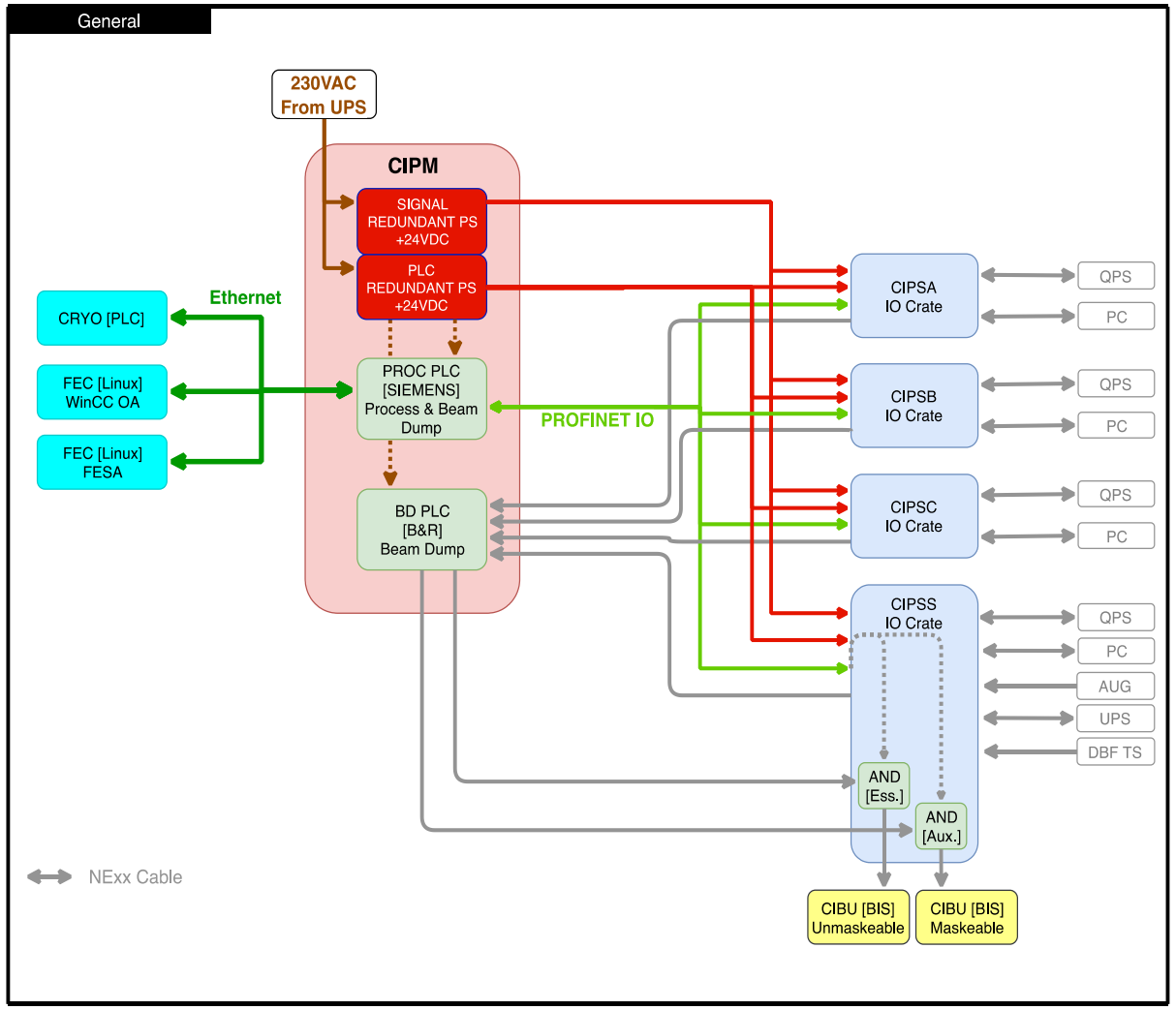
Conclusions

- **The PICv2 prototype is a full industrial solution that has been successfully tested in the MPE testbed and the Hardware is ready for IT-STRING.**
- **PLC configuration for LHC still to be defined.**
- **Review of the current loops specifications and voltage drop study with all stakeholder ongoing.**
- **The Second generation of PIC Software is currently under development by BE-ICS.**
- **PICv2 still to be integrated in AccTesting (ongoing).**
- **Very good understanding of the IST and HWC.**

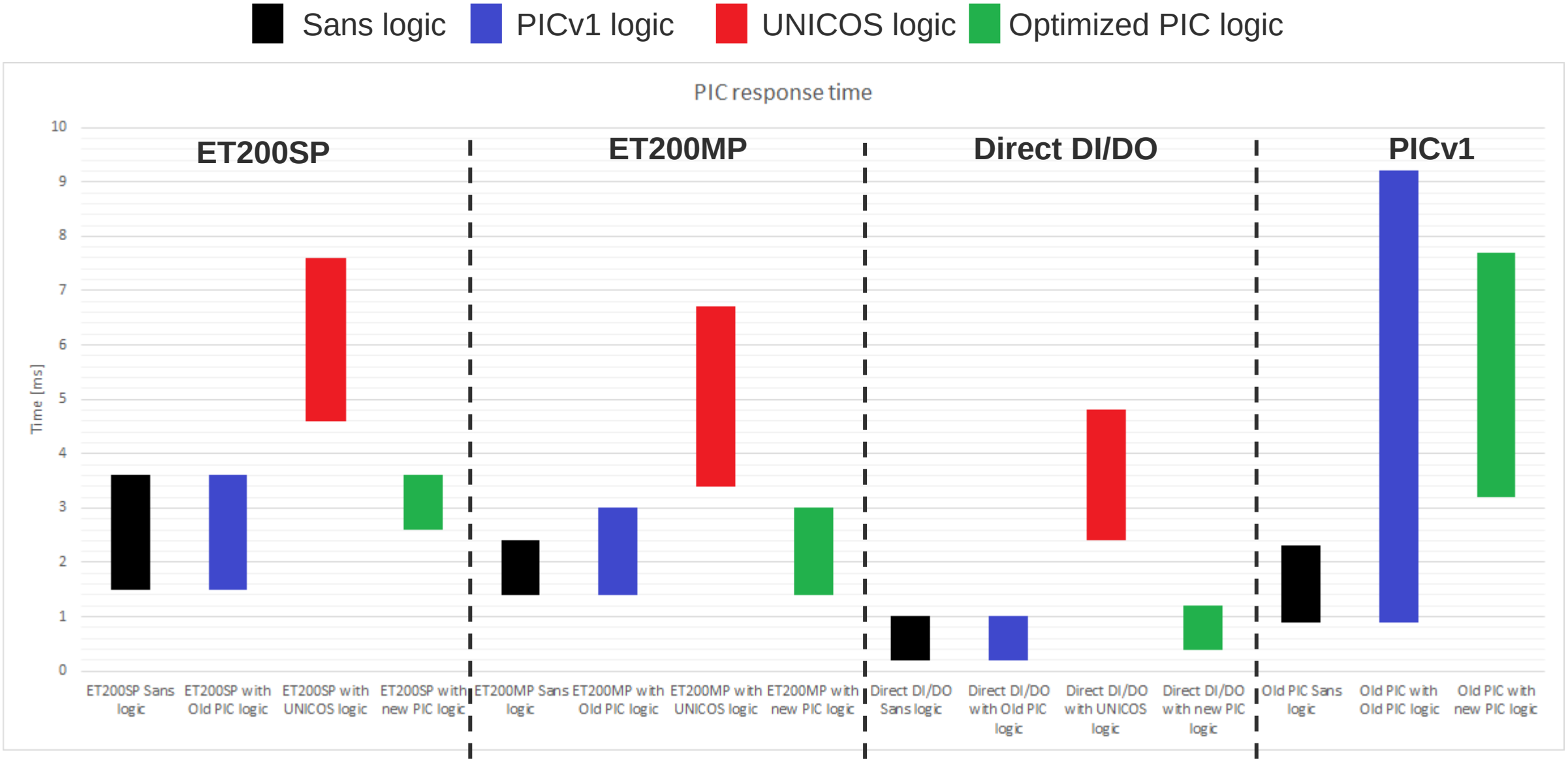


home.cern

Second Generation of PIC



PICv2 Industrial Solution – Response Time Results



PIC Software: Towards a Second Generation

- **Original PLC software**
  - Tailor-made, written in STL language.
  - Based on UNICOS TSPP protocol to communicate with WinCC OA (SCADA).
  - Not compatible with the current Siemens S7-1500 series PLC (UNICOS communication protocol).
- **A second generation of software is mandatory, keeping each system software generic throughout all instances.**

Two possible solutions

Development and maintenance of dedicated generic software and supervision (WinCC) for PIC

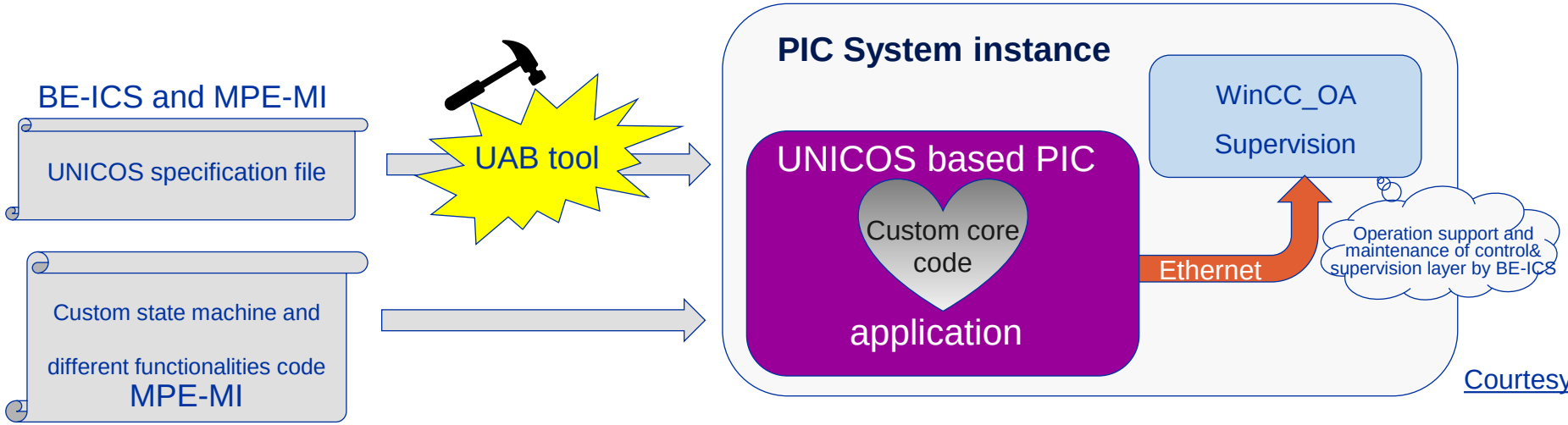
Future development and maintenance – fully under the responsibility of **MPE-MI**

Full integration of PIC into the UNICOS framework designed byBE-ICS.

Future development and maintenance – fully under the responsibility of **BE-ICS**

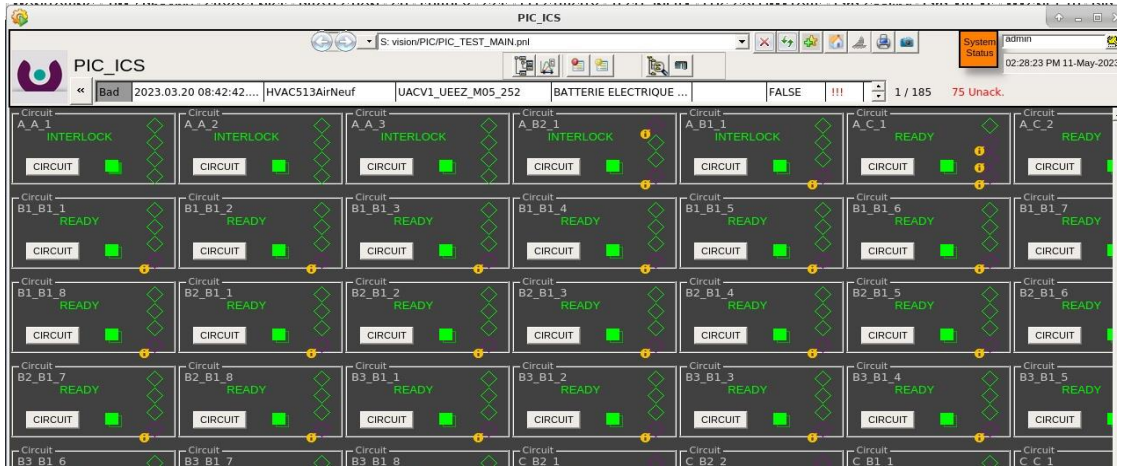
PIC v2 – UNICOS software Prototype

- **Fully UNICOS integrated PIC v2 software, is currently being developed by BE-ICS as a solution for IT STRING.**

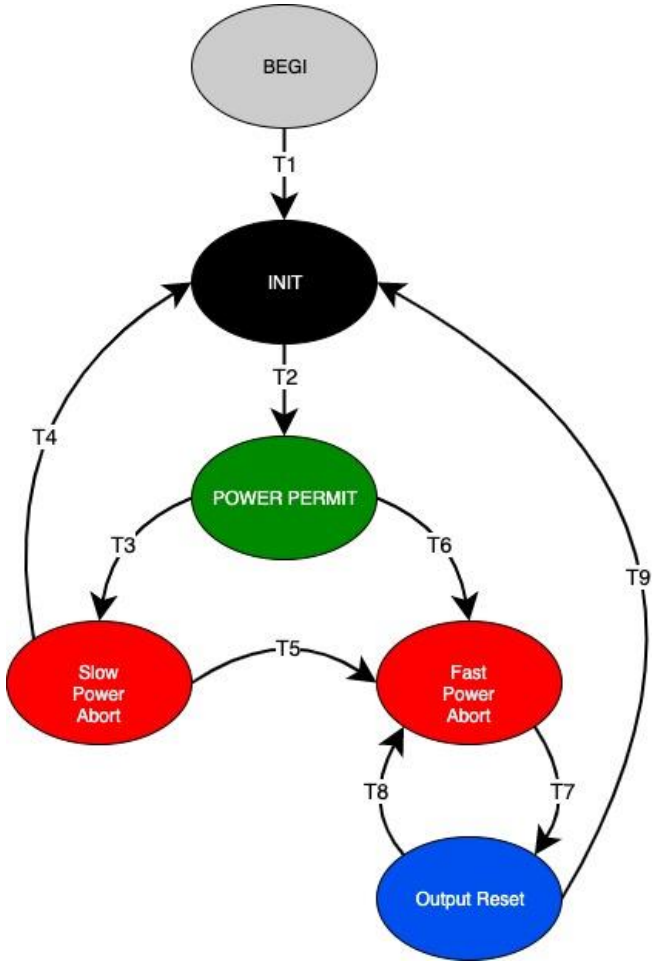


Courtesy of M. Kalinowski

- Study ongoing:
  - Merging several PICs in a powering Subsector maintaining a reaction time < 10 ms (PLC cycle time + Interface).
  - AccTesting integration.



Interlocking Strategy



Failure Type	PIC Action
Powering Failure	Slow Power Abort
Quench	Fast Power Abort
Discharge	Fast Power Abort
Cryo	Slow Power Abort
UPS	Slow Power Abort
AUG	Slow Power Abort
GPM	Fast Power Abort
Operator	Slow Power Abort Fast Power Abort

- The Global Protection Mechanism (GPM) is designed to trigger a preventive discharge of magnet circuits in the vicinity of a main magnet that quenched, in order to reduce the likelihood of secondary quenches due to heat propagation.
- Each circuit is configured to activate or not the global protection mechanism (GPM).