# System Test and Commissioning of QDS Instrumentation and Monitoring

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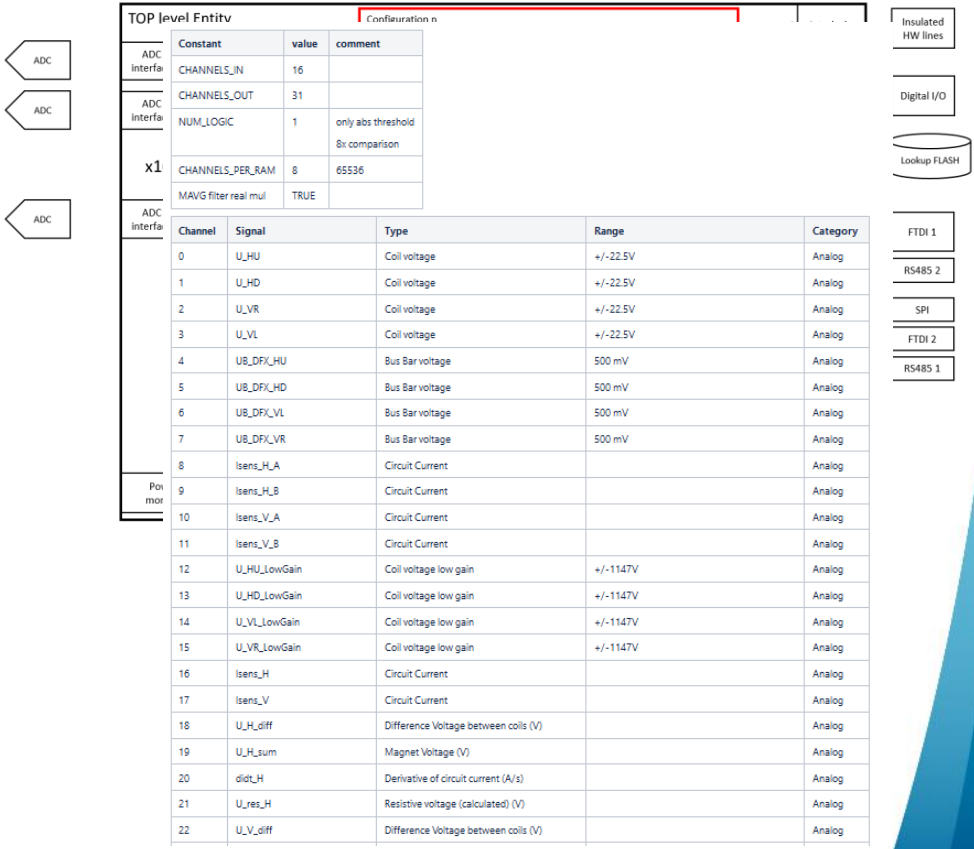
# Outline

1. Overview of QDS systems and their supervision
2. Individual system tests
3. Powering tests
4. Instrumentation and test methodology
5. Conclusions

# Universal Quench Detection System (UQDS)

- Baseline for HL-LHC protection
  - Details in the talk of Jens
- Common hardware
- **Behaviour configuration dependent**
- **Detailed testing is mandatory**
- SCADA integration
  - Common control interface
  - Unified data acquisition interface

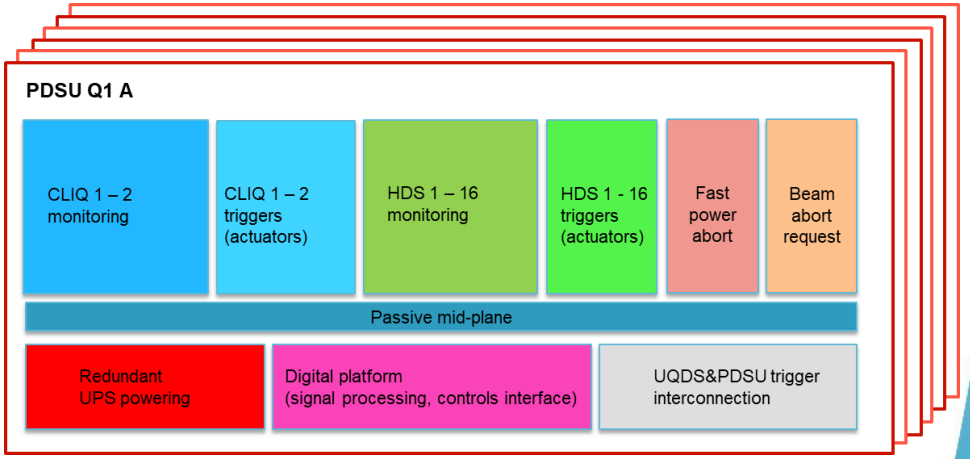



| Constant | value | comment |
|---|---|---|
| CHANNELS_IN | 16 | |
| CHANNELS_OUT | 31 | |
| NUM_LOGIC | 1 | only abs threshold 8x comparison |
| CHANNELS_PER_RAM | 8 | 65536 |
| MAVG filter real mul | TRUE | |

| Channel | Signal | Type | Range | Category |
|---|---|---|---|---|
| 0 | U_HU | Coil voltage | +/-22.5V | Analog |
| 1 | U_HD | Coil voltage | +/-22.5V | Analog |
| 2 | U_VR | Coil voltage | +/-22.5V | Analog |
| 3 | U_VL | Coil voltage | +/-22.5V | Analog |
| 4 | UB_DFX_HU | Bus Bar voltage | 500 mV | Analog |
| 5 | UB_DFX_HD | Bus Bar voltage | 500 mV | Analog |
| 6 | UB_DFX_VL | Bus Bar voltage | 500 mV | Analog |
| 7 | UB_DFX_VR | Bus Bar voltage | 500 mV | Analog |
| 8 | Isens_H_A | Circuit Current | | Analog |
| 9 | Isens_H_B | Circuit Current | | Analog |
| 10 | Isens_V_A | Circuit Current | | Analog |
| 11 | Isens_V_B | Circuit Current | | Analog |
| 12 | U_HU_LowGain | Coil voltage low gain | +/-1147V | Analog |
| 13 | U_HD_LowGain | Coil voltage low gain | +/-1147V | Analog |
| 14 | U_VL_LowGain | Coil voltage low gain | +/-1147V | Analog |
| 15 | U_VR_LowGain | Coil voltage low gain | +/-1147V | Analog |
| 16 | Isens_H | Circuit Current | | Analog |
| 17 | Isens_V | Circuit Current | | Analog |
| 18 | U_H_diff | Difference Voltage between coils (V) | | Analog |
| 19 | U_H_sum | Magnet Voltage (V) | | Analog |
| 20 | didt_H | Derivative of circuit current (A/s) | | Analog |
| 21 | U_res_H | Resistive voltage (calculated) (V) | | Analog |
| 22 | U_V_diff | Difference Voltage between coils (V) | | Analog |

# Protection Devices Supervision Unit (PDSU)

- System supervising protection devices:
  - Trigger links from 2x4 UQDS
  - Fans out to 96 Quench Heater Discharge Supply Power (HDS) trigger lines
  - Fans out to 12 Coupling-Loss-Induced Quench (CLIQ) trigger lines
  - Monitors 636 signals
- A trip of QDS:
  - Activates all HDS/CLIQ
  - Trips the Interlock loop
- A spurious trip of any HDS/CLIQ:
  - Trips the Interlock loop
  - Requests beam abort
  - Activates remaining HDS/CLIQ

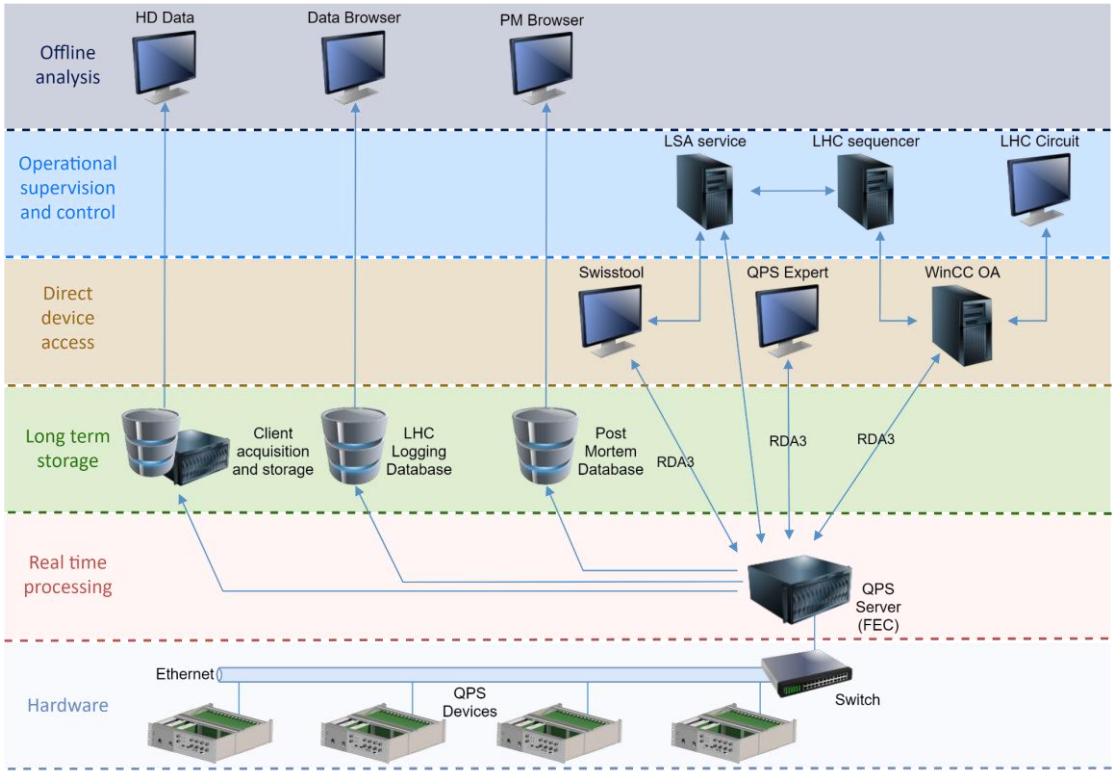


# PDSU

- **Complex system**
  - Multitude of inputs translate into interlocks
- Common hardware
- Common firmware and configuration
- **Detailed testing is mandatory**
- SCADA integration
  - Common control interface
  - Common data acquisition interface

- PDSU exposes following signals:
  - 16 DQHDS voltages (analog)
  - 16 DQHDS currents (analog)
  - 16 DQHDS trigger voltages (analog)
  - 16 DQHDS supply voltages (analog)
  - 16 DQHDS connection (digital)
  - 2 CLIQ voltages (analog)
  - 8 CLIQ currents (analog)
  - 2 CLIQ trigger voltages (analog)
  - 4 trigger supply voltages (analog)
  - 8 UQDS triggers (digital)
  - 2 PDSU triggers (digital)
- Available commands:
  - Reset
  - Buffer read
  - Buffer trigger
  - Logging
  - Test mode trigger
  - Read parameters
  - Write parameters

# QPS Supervision and Control



# System tests and commissioning

1. Integrity of the QDS cabling
2. Installation of QDS units
3. Supervision and configuration
4. QDS system verification – phase 1
5. QDS system verification – phase 2
6. Low current powering
7. QDS system tests completed

# Integrity of the QDS cabling

- Objective
  - Verification of the presence and instrumentation cabling integrity
- Requirements:
  - Field access required
  - Instrumentation VTAPs starting from Instrumentation Feedthrough System (IFS) box and ending on the QDS equipment verified by the ELQA team.
- Procedure
  - Verification of the routing between QDS patch panels and UQDS units
  - Verification of the integrity of interlock and trigger cables of UQDS
  - Verification of the instrumentation between PDSU and HDS/CLIQ
  - Verification of the integrity of interlock and trigger cables of PDSU
  - Verification of Ethernet cables

# Installation of QDS units

- Objective
  - UQDS and PDSU systems installed and powered
- Requirements
  - Field access required
- Procedure
  - Verification of the position of UQDS crates
  - Verification of the position of PDSU crates
  - Verification of the redundant powering of the systems

# Supervision and configuration

- Objective
  - Systems available in the SCADA and properly configured
- Requirements:
  - Remote access required
  - UQDS instrumentation is either connected to superconducting circuits or shorted in order to avoid continuous tripping of the protection
- Procedure
  - Verification of the QPS SCADA stack
  - Verification of availability and responsivity of all devices
  - Verification of the configuration of UQDS and PDSU systems
  - Verification of data integrity in NXCALS and PM services

# QDS system verification – phase 1

- Objective
  - Basic verification of the instrumentation
- Requirements:
  - Field and remote accesses required
  - Superconducting circuits are in the non-powered state
  - HDS and CLIQ units connected and not energized
- Procedure
  - Verification of all analogue signals
    - All signals are present, live and within specified ranges
  - Basic interlock and trigger lines tests
    - All detectors are tested
    - Aims on verifying that all connections are present

# QDS system verification – phase 2

- Objective
  - Integrity of interlocks and trigger lines
- Requirements:
  - Remote access required
  - Superconducting magnets cooled to the nominal temperature
  - HDS and CLIQ units energized to low energy and latched
    - Units will be discharged several times during tests
  - Interlocks of Energy Extraction (EE) systems installed
- Procedure
  - Verification of analogue signals of PDSU units
  - Verification of all interlock and trigger lines of UQDS units
  - Verification of all interlock and trigger lines of PDSU units
  - Verification of activation of EE systems

# Low current powering

- Objective
  - Exhaustive verification of the instrumentation
- Requirements:
  - Remote access required
  - Superconducting circuits powered with low and safe currents as defined by MCF/MP3
- Procedure
  - Reassurance that powering conditions are met
  - Verification of analogue signals of UQDS units
    - Magnet instrumentation and current sensors are subject of tests
    - Signals tested for expected patterns in given powering conditions

# QDS system tests completed

- QDS equipment released for further powering tests
  - Quench detection systems tested completely
  - Quench detection infrastructure conforms the specification
- Subsequent steps
  - Monitoring of the health of the system during powering tests
  - Following up the protection events

# Instrumentation and test methodology

- Archiving operational and protection event data sets
  - NXCALS service
  - PM service
- QDS tests tracking will rely on AccTesting
  - Reinforcement of the order and execution of all required steps
  - The individual steps are to be defined in collaboration with MCF/MP3
  - The actual implementation to be requested from TE-MPE-CB
- Tests will be executed and supervised by the QDS expert team
  - Dedicated scripts shall facilitate this process
  - Expert tools and checks will rely on direct subscriptions

# Conclusions

- QDS validation comprises of multiple stages
  - Targets different aspects of system installation and operation
  - All stages are equally important
- QDS tests are crucial to ensure the protection
  - Meticulous execution with right amount of assigned time is a key
  - Processes tracking and data archiving are paramount
- Existing procedures and tools enable successful execution
  - Adaptations are required for IT-String infrastructure


***Thank you for your attention.***