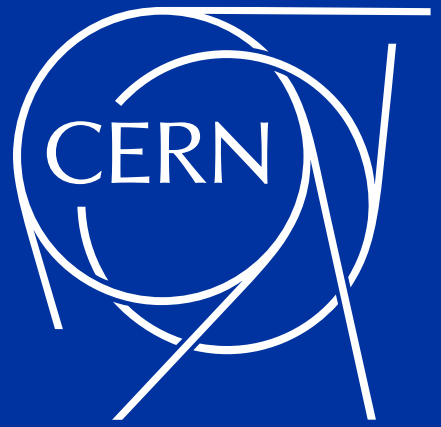


Quench Detection and Monitoring Baseline

Jens Steckert, Reiner Denz, Tomasz Podzorny, Jelena Spasic & MPE-EP Colleagues

Thanks to: Samer Yammine, Alvaro Santiago Ferrer, Giorgio D’Angelo, Emmanuele Ravaioli and SM18 crew

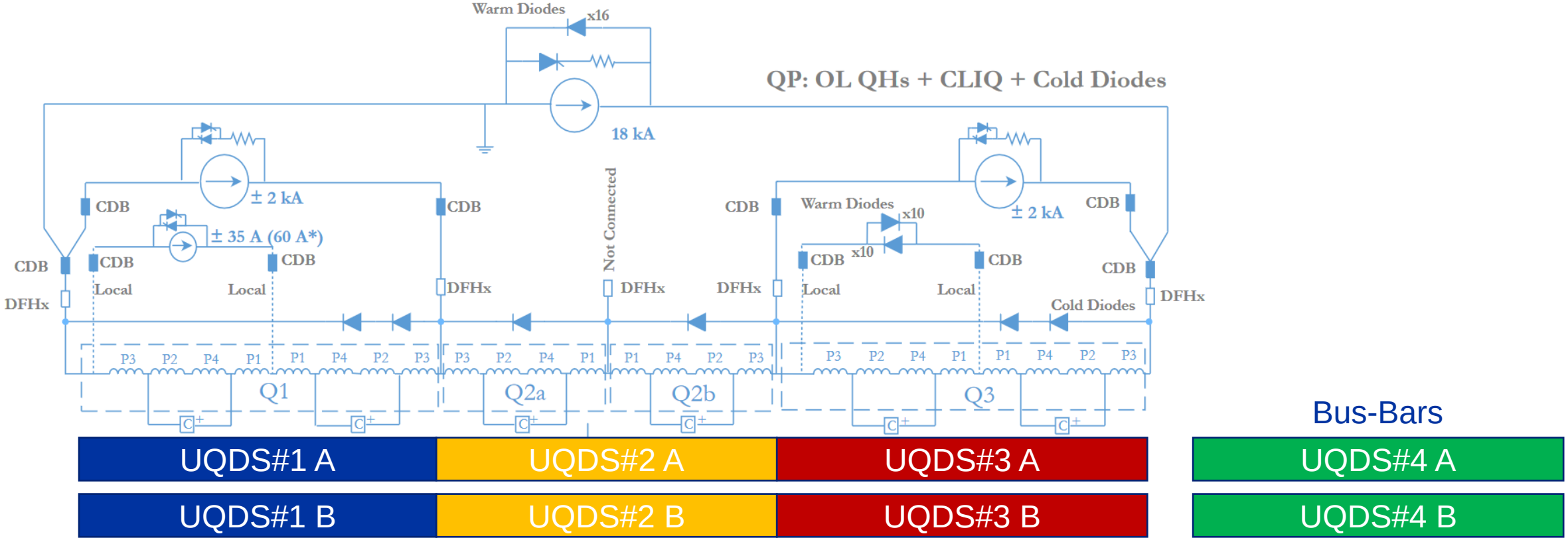
Outline

- **Baseline scheme for quench detection**
  - Inner Triplet main circuit
    - Coil-Coil, flat vs hierarchical, abs bus-bar voltage
    - System partition
  - 2kA correctors
    - Coil-Coil, L*di/dt, abs bus-bar voltage
  - D1, D2 + corrector
    - D1 symmetric and asymmetric detection scheme, D2 QD scheme, D2 corrector QD scheme
  - Bus-bars and Superconducting Link
- **QDS threshold definition and management**
  - Management of QD thresholds (Repo and x-checking tools, checksum)
- **Monitoring baseline**
  - Elements and signals (SC Link monitoring, Current monitoring, Diode monitoring)

General quench detection principles for HiLumi

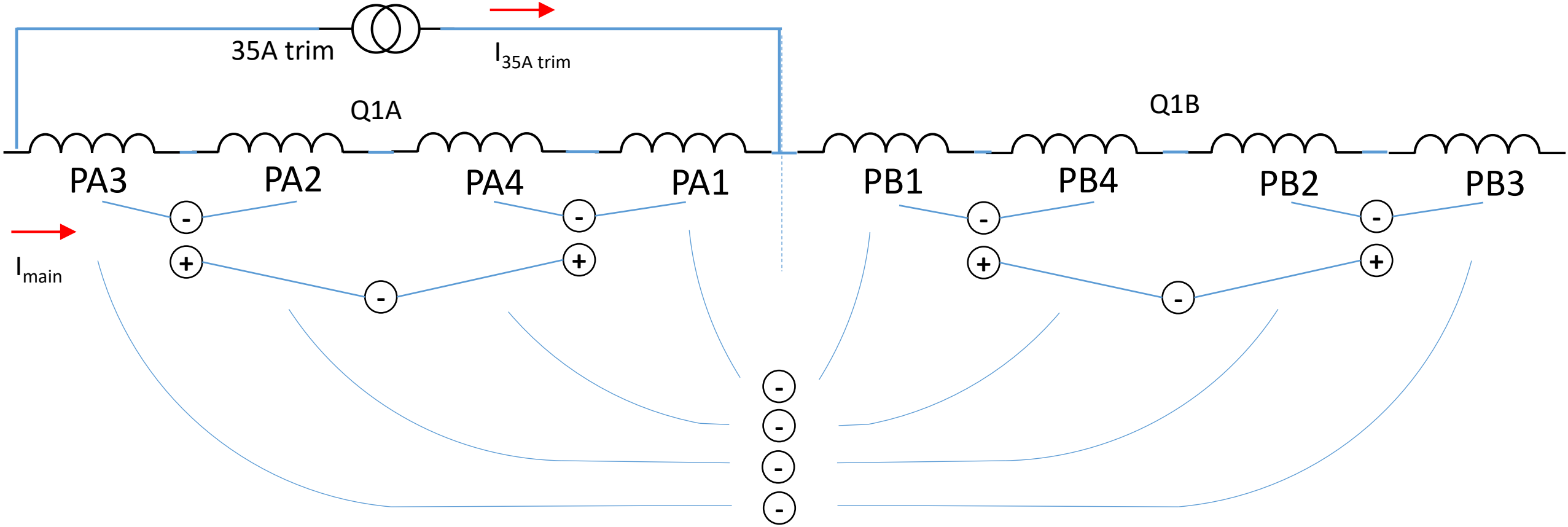
- All superconducting circuit elements are monitored and interlocked
- Whenever possible, bus-bar protection is separated from magnet protection
- Inner triplet has all poles instrumented in a fully redundant and exclusive way (forming differential pairs)
- Robust coil-coil comparison algorithms are preferred
- L*di/dt compensation algorithms are used for symmetric quench detection on correctors and used with lowest noise current sensors (DCCT)
- Dedicated current measurement for most of the circuits allow current dependent settings

Inner triple circuit, QDS overview



- **Each UQDS observes all magnet poles with identical current (except Q1)**
- **Comparison among poles detect asymmetric and symmetric quenches**
- **Bus-Bars between magnets and magnet and link are protected by separate UQDS**

IT QD algorithm example: Q1



Asymmetric detection: Coil-coil comparison of neighboring coils (PA3 - PA2, PA4 – PA1, PB1 – PB4, PB2 – PB3)

Magnet symmetric detection: Comparison of magnet halves: (PA3 + PA4) – (PA4 + PA1), (PB1 + PB4) – (PB2 + PB3)

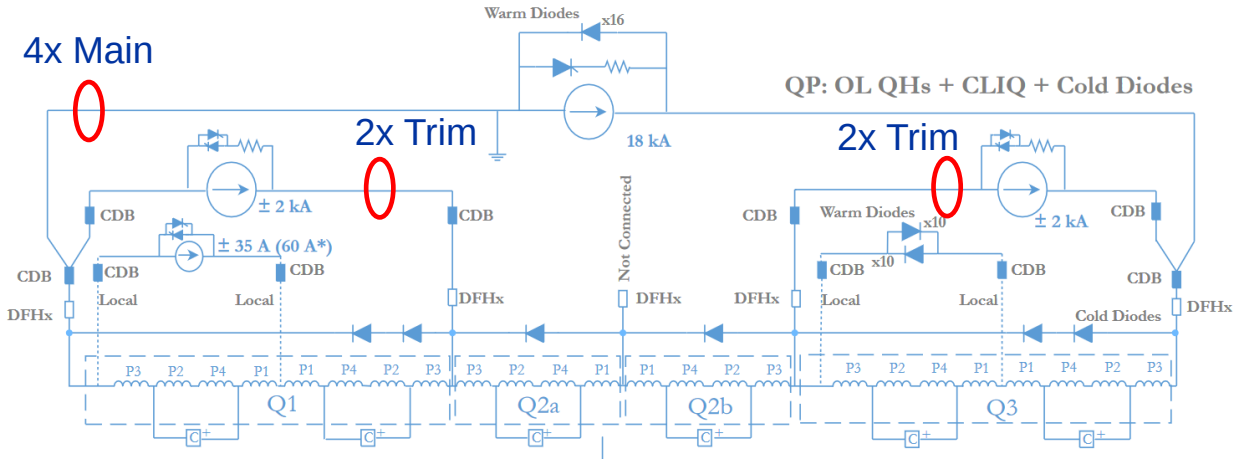
Full symmetric detection: Comparison of Coil voltages between Q1A and Q1B

IT QD, additional aspects

- **Due to trim in Q1A, inductive voltage per pole can differ up to +/-28.64mV between Q1A and Q1B (Based on max di/dt of 3.32A/s and 8.625mH pole inductivity)**
- **Voltage is still compatible with high current threshold of 100mV**
- **If the trip of the 35A converter causes out-of-spec di/dt, symmetric QD could trigger**

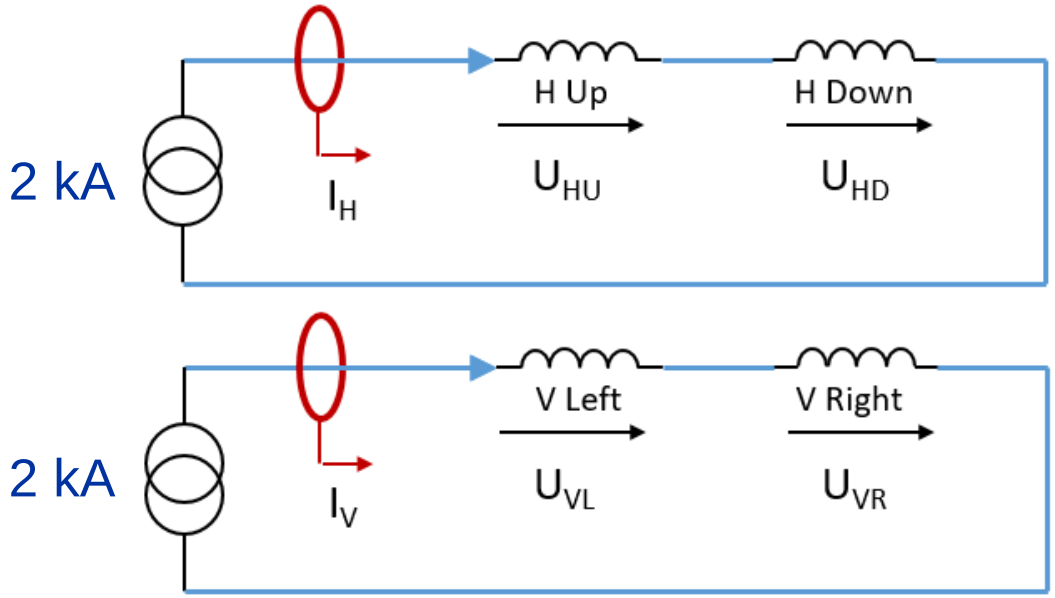
Inner triplet circuit QD, current dependent settings

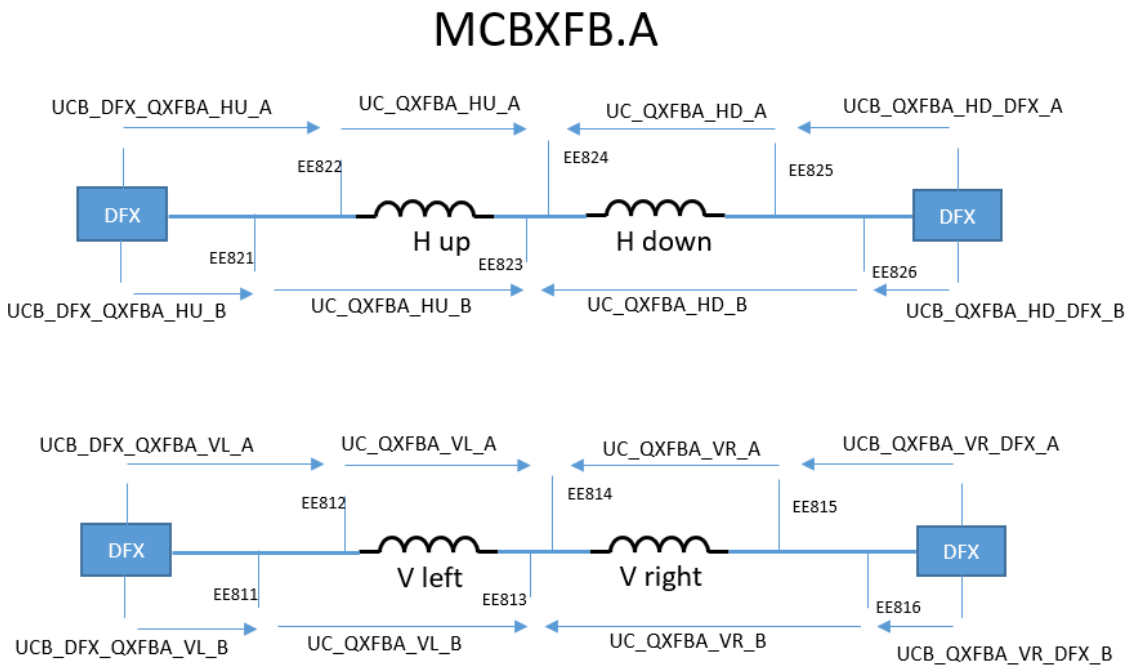
- **Current measurement of main and trim power converters**
  - Main circuit: 4 current sensors
    (2 parallel water-cooled cables + redundancy)
  - Trim circuit: 2 current sensors



- **“Real” current through each circuit to be calculated from current readings**
- **Each system is reading both redundant sensors and compares them**
- **Current identical for each element of Q1, Q2, Q3**
- **Current dependent settings are vital for compensation of flux jumps, allowing relaxed thresholds and discrimination times at lower currents where flux jumps are dominant**

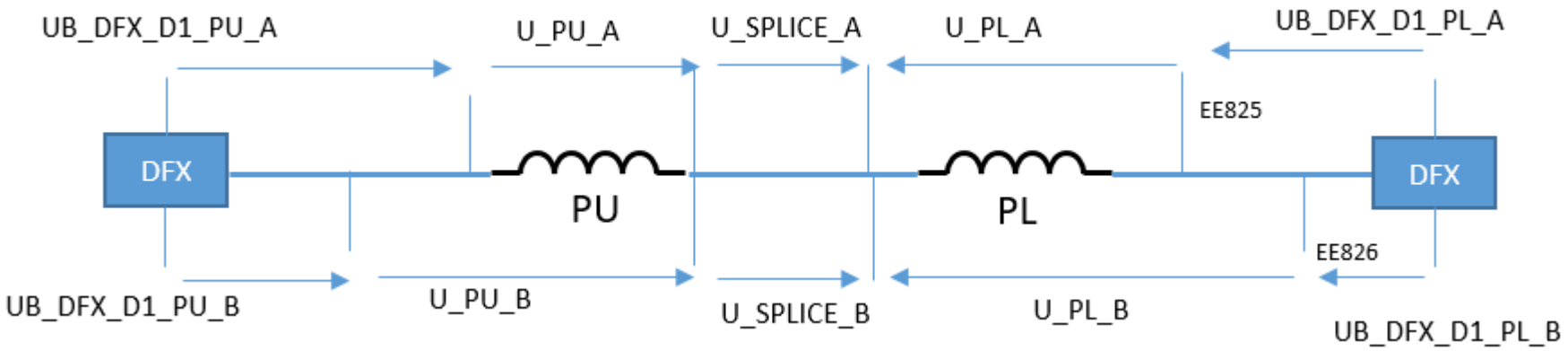
IT correctors MCBXF(A/B)





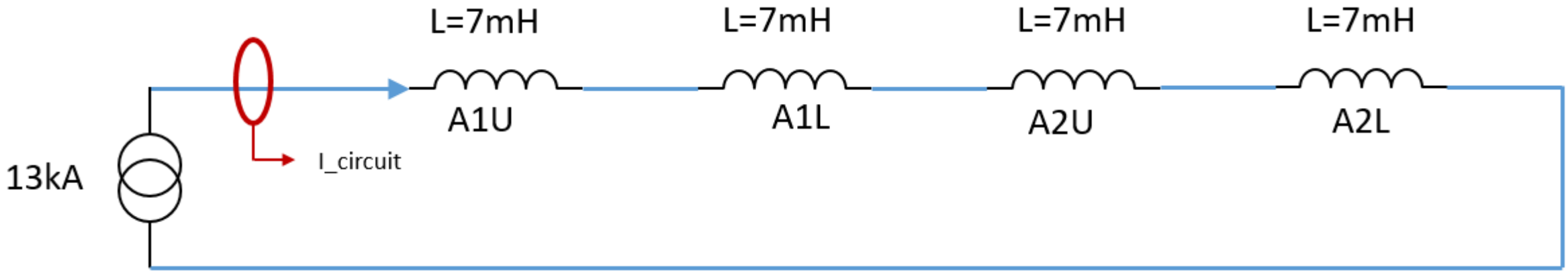
- **Asymmetric QD: Coil – Coil comparison, Bus-bars protected separately**
- **Symmetric QD: L*di/dt based algorithm** Ures = (U_{HU} + U_{HD}) – (L* di/dt)
- **Current measurement by DCCT on ¼ of current, digitally upscaled**

D1 circuit



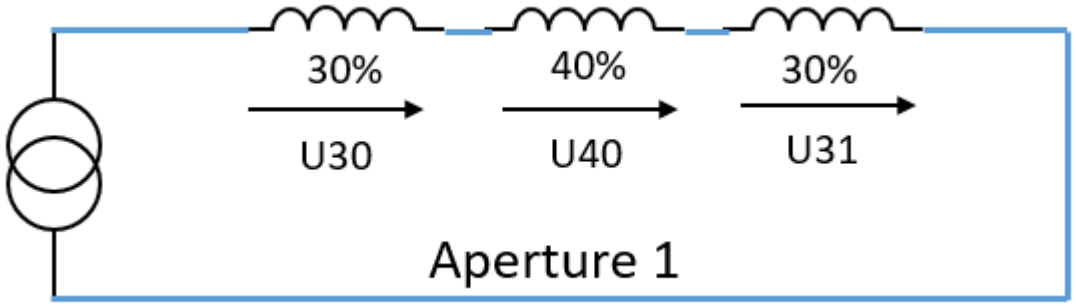
- **Asymmetric QD: Coil-Coil comparison**
- **Symmetric QD:**
  - Bus-bar between coils monitored with absolute bipolar threshold +/-50mV
  - Absolute positive threshold for coil voltage +200mV
    (active for currents > 1kA to avoid trips during PC start up)
  - QH of D1 will be fired if IT heaters are fired (so no heat propagation induced quenches from IT trips)

D2 circuit



- **Asymmetric QD: Coil comparisons (U_A1U – U_A1L), (U_A2U – U_A2L)**
- **Symmetric QD: Magnet half comparisons (U_A1U + U_A1L) – (U_A2U + U_A2L)**
- **Symmetric quench of all 4 coils is considered to be very unlikely**
- **Bus-bars between link and magnet monitored separately**

D2 corrector, MCBRD

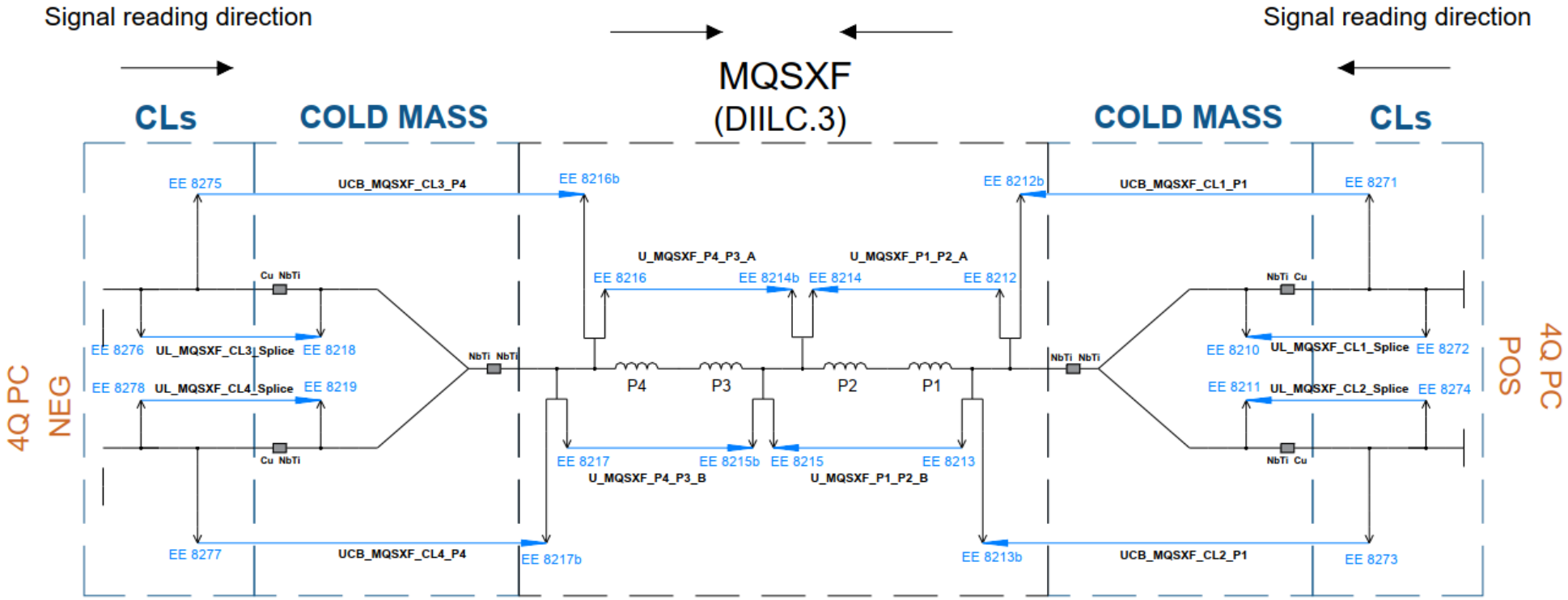


Ures = 3/2 * U40 – (U30 + U31)

Quenching element voltage	Effective threshold	Effective threshold (T= 50mV)
U30, U31	T	50 mV
U40	T / 1.5	33 mV
U30 & U31	T / 2	25 mV
U30 & U40	T * 2	100 mV
U31 & U40	T * 2	100 mV
U31 & U40 & U31	T * 2	100 mV

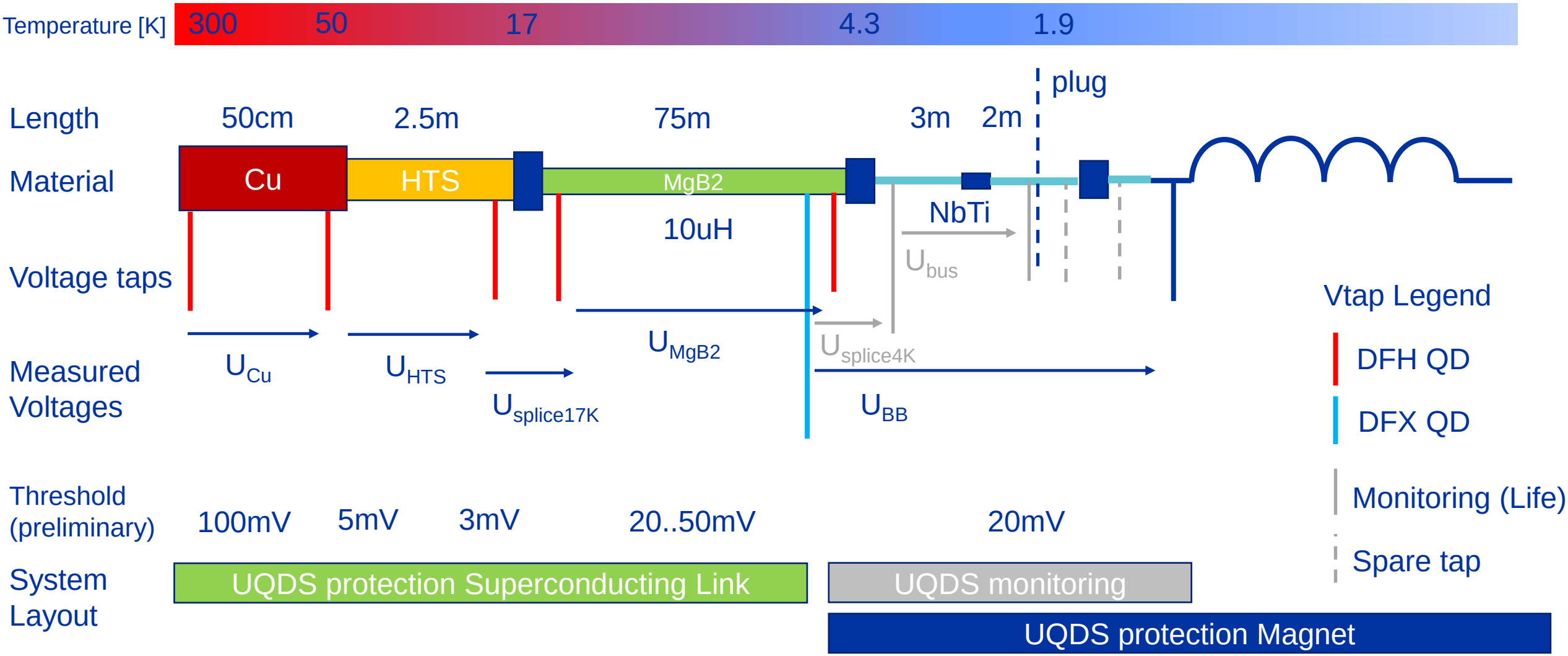
- **Hybrid algorithm for asymmetric and symmetric quenches**
- **Comparison algorithm with scaling allows to detect symmetric quenches as resistive voltage doesn’t scale the same way as inductive voltage**
- **Effective thresholds depend on number and location of quenching elements**
- **Scheme tested in SM18**

MQSXF



- **Asymmetric QD: magnet half comparison**
- **Symmetric QD: L*di/dt inductive compensation**
- **Current leads (NC): One current sensor per lead (comparison interlock)**
  Verification of current sharing

Quench detection of SC Link



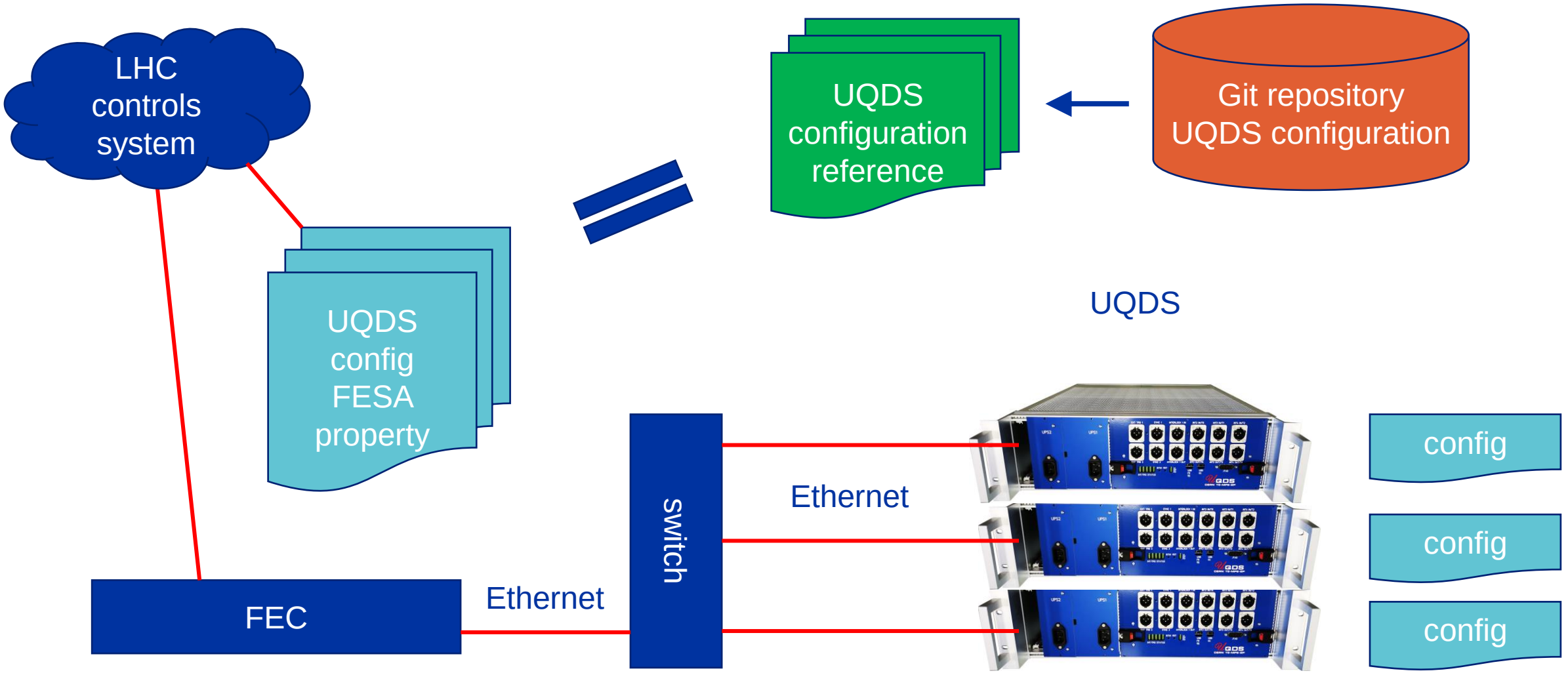
Quench detection summary

Circuit	Current	QD algorithm asymmetric	QD algorithm symmetric
Q1, Q2, Q3	18 kA	Coil comparison Current dependent thresholds	Coil comparisons across magnet Current dependent thresholds
MCBXFA/B	2 kA	Coil comparison	L*di/*dt inductive compensation Current dependent thresholds
MQSXF	120 A	Coil comparison	L*di/dt inductive compensation Current dependent thresholds
D1	13 kA	Coil comparison	Absolute unipolar coil voltage threshold Active for > I_MIN_OP Absolute, bipolar threshold on Bus-Bar
D2	13 kA	Coil comparison	Magnet half comparison
MCBRD	2 kA	Coil comparison with scaling	
Bus-Bars	Misc.	Absolute threshold	
SC-Linc	Misc.	Absolute thresholds over 4 parts of the Link	

Configuration management

- **Digital quench detectors can be remotely configured (in limits)**
- **Remotely changeable thresholds and filters have been very useful in the past**
- **Critical protection parameters are defined by magnet owners (MP3 in the end)**
- **Configurable parameters require supervision to prevent erroneous settings**
- **HL-LHC QD controls system is designed with configuration management in mind**
- **Configuration management allows:**
  - Continuous supervision of critical parameters
  - Re-configuration of hardware after intervention
  - Controlled modification of parameters due to protected repository
  - Tracking of changes via Git history

Configuration management – Architecture



Configuration management – layered approach

- **Checksum inside UQDS register file (column parity) ensures integrity on low level (wrong values open interlock)**
- **Periodic transmission of register file through controls system and exposure as FESA property**
- **Periodic comparison of FESA property with reference from repository**
- **FESA property can also be pushed down to UQDS crate in case of new configuration or hardware exchange**
- **Changes to configuration initiated on repository level only → full traceability and safety**
- **Configuration tables are stored as human-readable text files for full traceability**

Monitoring Baseline

- **Monitored circuit elements are instrumented and connected to UQDS**
- **UQDS on monitored elements is not redundant and not interlocking**
- **Monitored signals might send post mortems dependent on the supervised element**
- **All monitored signals are recorded in logging database**
- **All monitored signals are time synchronous to the other signals <1ms**

Monitored (not used for QD) signals overview

Circuit	Element(s)	# per IP side	Description	PM trigger condition
IT, 35A trim	6kA current sensor	2	Additional current sensor for MP3	Sync with Main IT QDS
IT, cold diodes	Cold diode voltages	28	Diode voltage supervision	Sync with Main IT QDS
IT, warm diode	Warm diode voltages	8	Diode voltage supervision	Sync with Main IT QDS
IT, CLIQ leads	CLIQ lead voltage	12	Monitor voltage across NC CLIQ leads	Sync with Main IT QDS
IT k mod leads	Kmod leads voltage	4	Monitor voltage across Kmod leads	
All with SC link	U_SPLICE4K, U_BUS	2x16	Additional voltages for SC link diagnosis	Sync with associated Circuit QDS
Total		86		

Some open Points

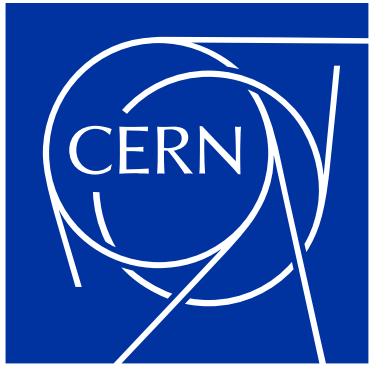
- **Signal naming needs to be polished, not fully consistent throughout the circuits**

  → We need to work out a scheme in the coming weeks, should not be an issue

- **CLIQ & Kmod lead monitoring Vtaps violate the exclusive pole Vtap scheme of IT circuit**
  - The effect on signal integrity needs to be studied
  - This configuration can be tested in STRING

Summary

- Quench detection algorithms defined for all circuits
- Key QD algorithms are tested in SM18
- Current monitoring established (for protection and analysis)
- System layout and voltage allocation finished
- Configuration management defined, first experience to be collected in SM18
- Monitoring baseline established



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