UNIVERSITY OF LIVERPOOL

Solid State Tracking Detectors for Experiments at Future Circular Colliders

Corfu Workshop on Future Accelerators, 24th to 28th of April 2023

Abstract:

Modern detector science and technology has originated from High Energy Physics experiment needs in the ‘80’s of the past century, based on the achievement and knowledge of the silicon industry of the time. In particular, the first segmented array of silicon diodes (a microstrip sensor) was developed to track vertices at the NA11 experiment at the SPS accelerator at CERN (Geneva, CH). During the following years, detector technology developed into a special branch of the huge silicon research and development enterprise that has strongly contributed to the evolution of science and society. For the sensor technology, this development has been driven by the ever more demanding needs of particle physics experiments at colliders. Now, future colliders hunting for BSM physics set again incredibly difficult challenges for particle tracking sensors. A discussion of the R&D achievements and trends is here presented.

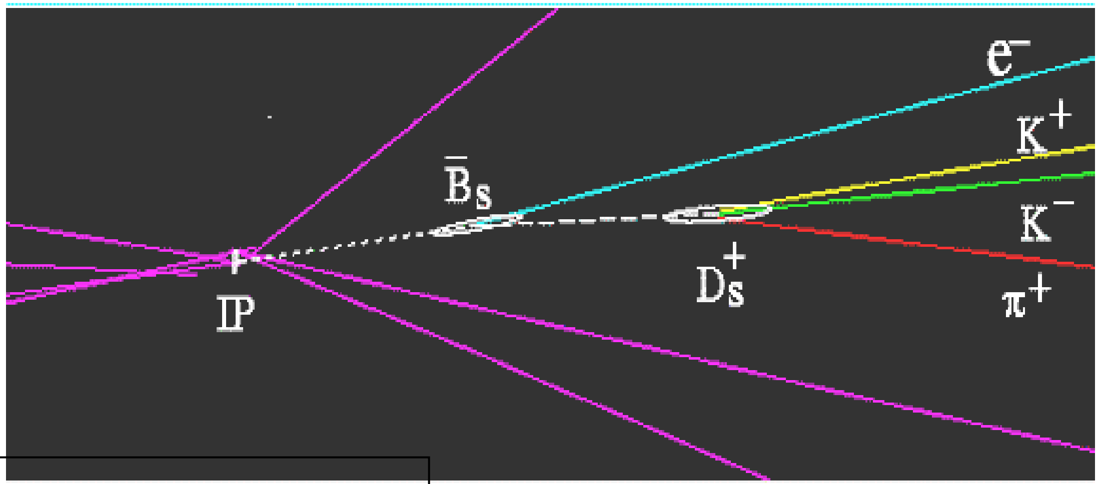
OUTLINE:

- Physics requirements and silicon sensors: fulfilling ever more stringent requests. The revolutionary impact of silicon detectors in HEP
- The technology drivers to sensor evolution:
  - Improvements on the sensing elements (niche foundries)
  - Evolution of microelectronics (CMOS)
- State-of-the-art: is silicon sensor development slowing ?
- The Future Circular Collider needs: huge challenge for detector technology

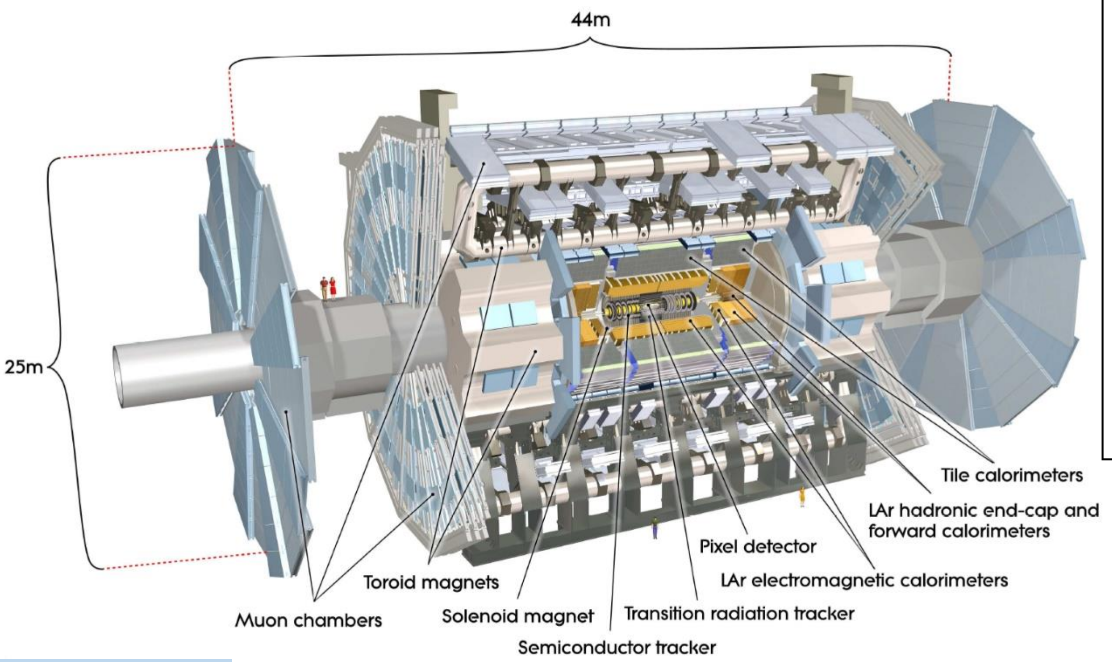
Collider physics detectors

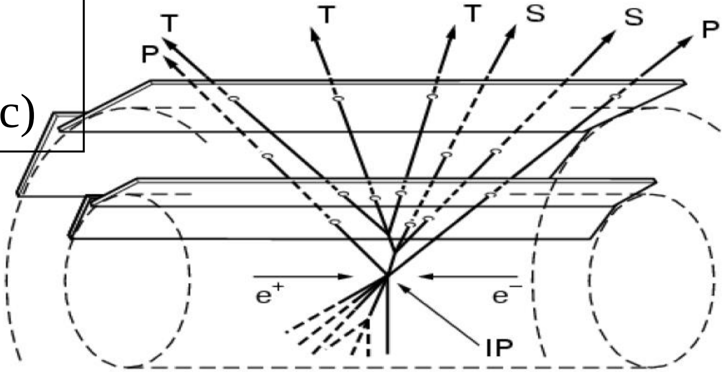
Required performance for general purpose particle physics detectors:

- full solid angle coverage
- accurate momentum and/or energy measurement
- identification of all particles
- no dead time
- Vertices identification



Example:
Mean decay length B_s ($\tau \approx 1.5$ ps):
in B_s-frame: $c_\tau \approx 450\ \mu m$
in lab frame $\beta\gamma c_\tau$ = few mm!
D_s ($\tau \sim 0.5$ ps):
in D_s-frame: $c_\tau \approx 150\ \mu m$
in lab frame $\beta\gamma c_\tau$ = few mm!
(lower mass $\Rightarrow$ more relativistic)

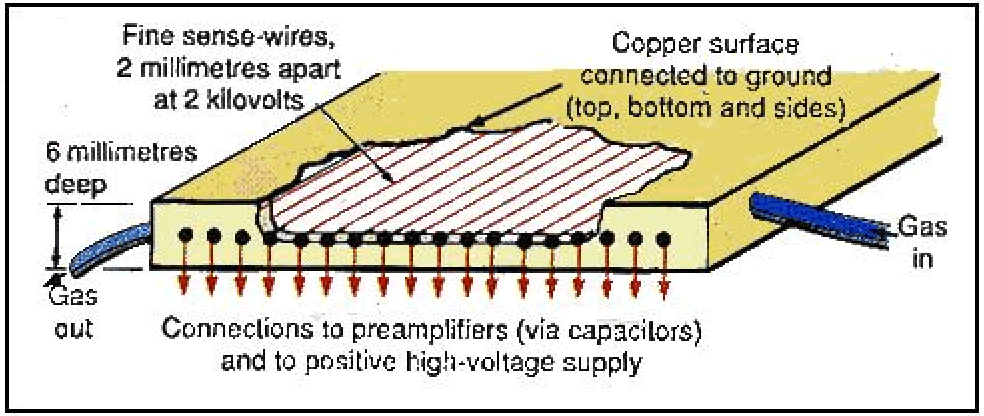




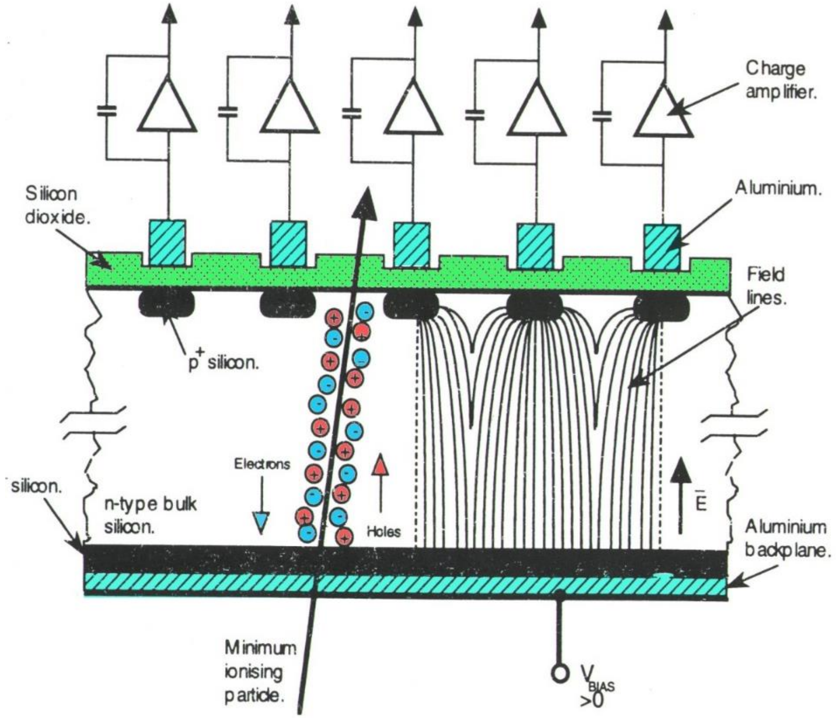
Technologies for HEP detectors

Three major families:

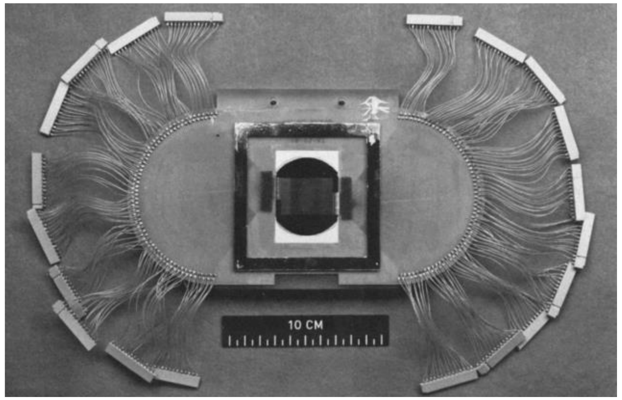
- Gaseous detectors: sensing ionisation in gas (mip charge ~ 90 e/ion pairs cm^{-1})
- Solid state detectors (mip charge ~ 40 to 160 e/h pairs μm^{-1})
- Scintillating detectors (scintillating light detected by photon detectors)

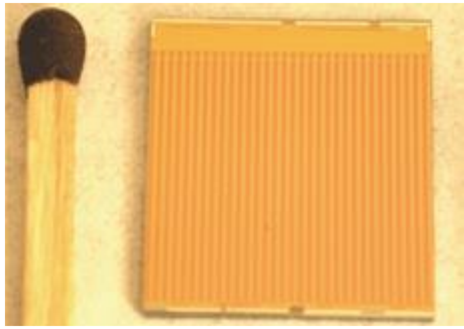


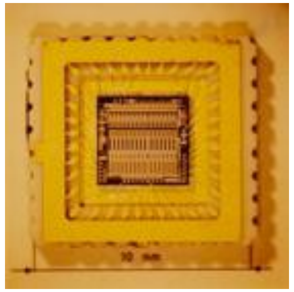
A typical multiwire proportional chamber. The cutaway reveals the fine sense-wires inside

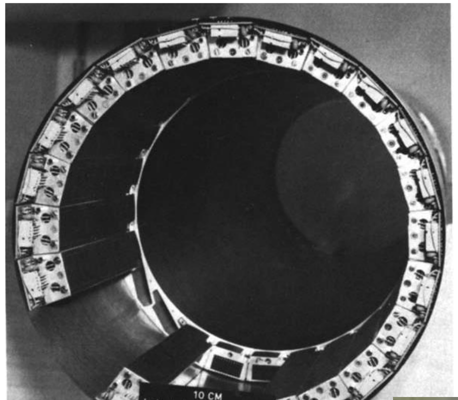


The Spectacular success of Silicon detectors





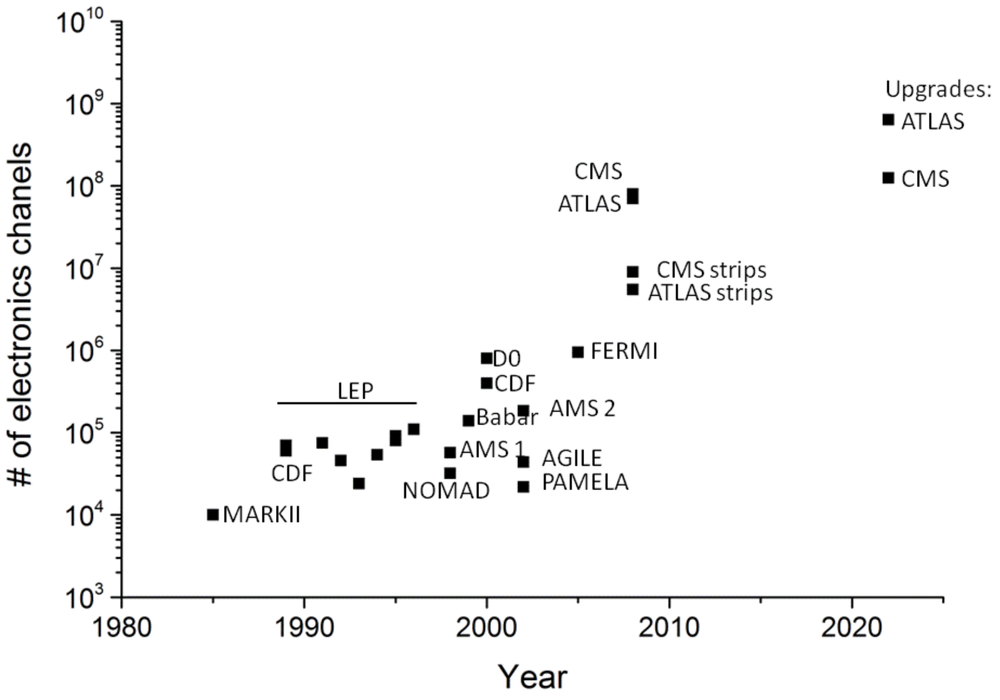


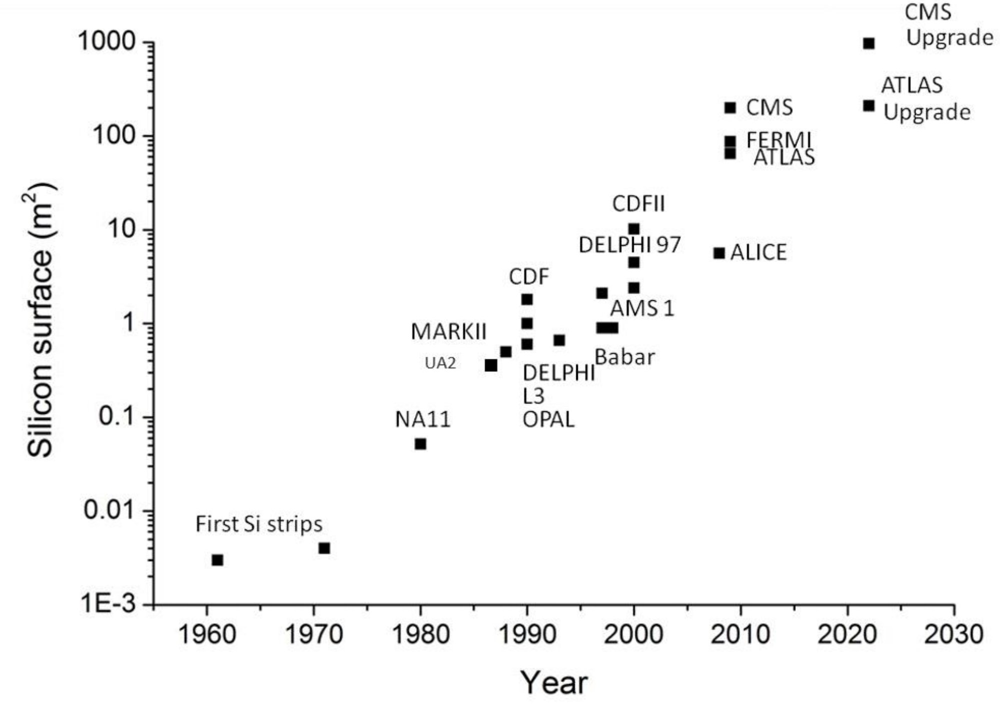


ASIC’s for silicon detector readout: 1988 (UA2 at the CERN/SPS): first collider experiment with silicon detectors with ASIC read-out, namely the AMPLEX, 16 channel, 3 µm Feature Size (S) CMOS chip for read-out and signal multiplexing (E. Heijne, P. Jarron).

The Spectacular success of Silicon detectors

- A virtuous interaction between technology and experiment needs: technology improvements allow better physics performance and experiment requirements push on the technology.
- CMOS technology evolution is driven by motivations outside physics.

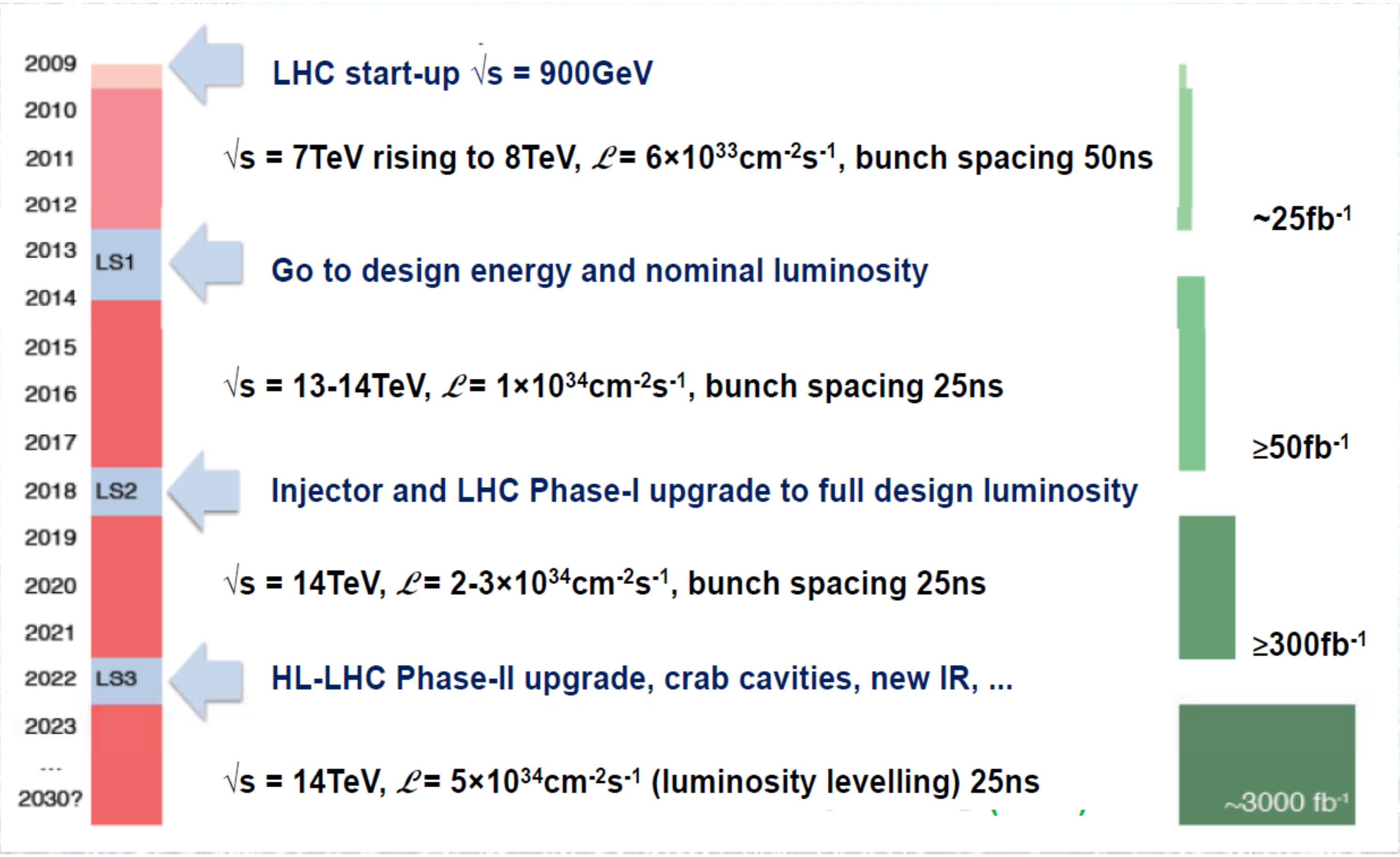




How experiment needs are driving sensor development

Possible 20 Year LHC Schedule

Before 2009



LHC start-up $\sqrt{s}$ = 900GeV

$\sqrt{s}$ = 7TeV rising to 8TeV, $\mathcal{L}$= $6\times10^{33}cm^{-2}s^{-1}$, bunch spacing 50ns

Go to design energy and nominal luminosity

$\sqrt{s}$ = 13-14TeV, $\mathcal{L}$= $1\times10^{34}cm^{-2}s^{-1}$, bunch spacing 25ns

Injector and LHC Phase-I upgrade to full design luminosity

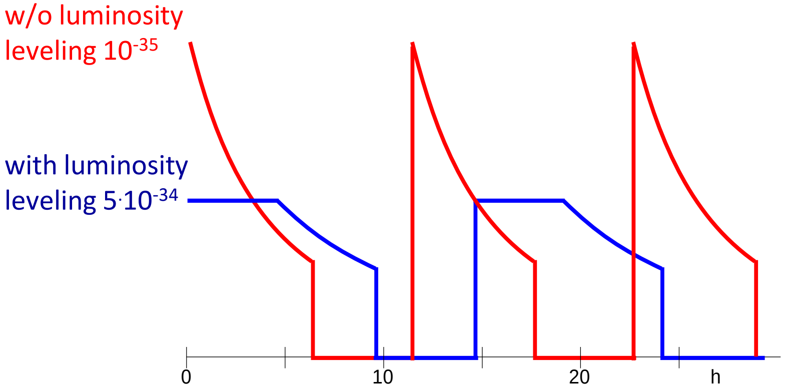
$\sqrt{s}$ = 14TeV, $\mathcal{L}$= $2\text{-}3\times10^{34}cm^{-2}s^{-1}$, bunch spacing 25ns

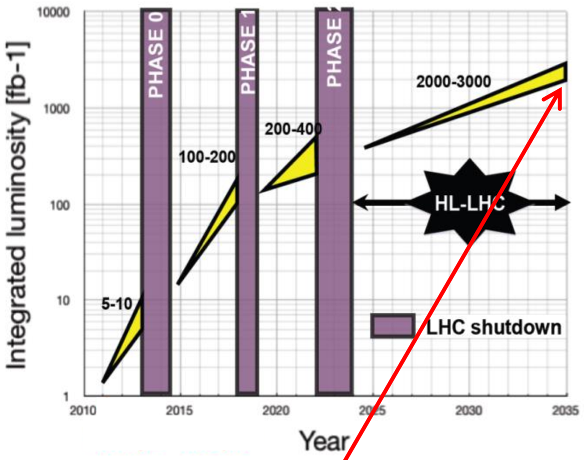
HL-LHC Phase-II upgrade, crab cavities, new IR, ...

$\sqrt{s}$ = 14TeV, $\mathcal{L}$= $5\times10^{34}cm^{-2}s^{-1}$ (luminosity levelling) 25ns

HL-LHC Performance Goals

- Leveled peak luminosity: $L = 5 \times 10^{34}\ \mathrm{cm^{-2}\,sec^{-1}}$
- Virtual peak luminosity: $L = 10 \times 10^{34}\ \mathrm{cm^{-2}\,sec^{-1}}$



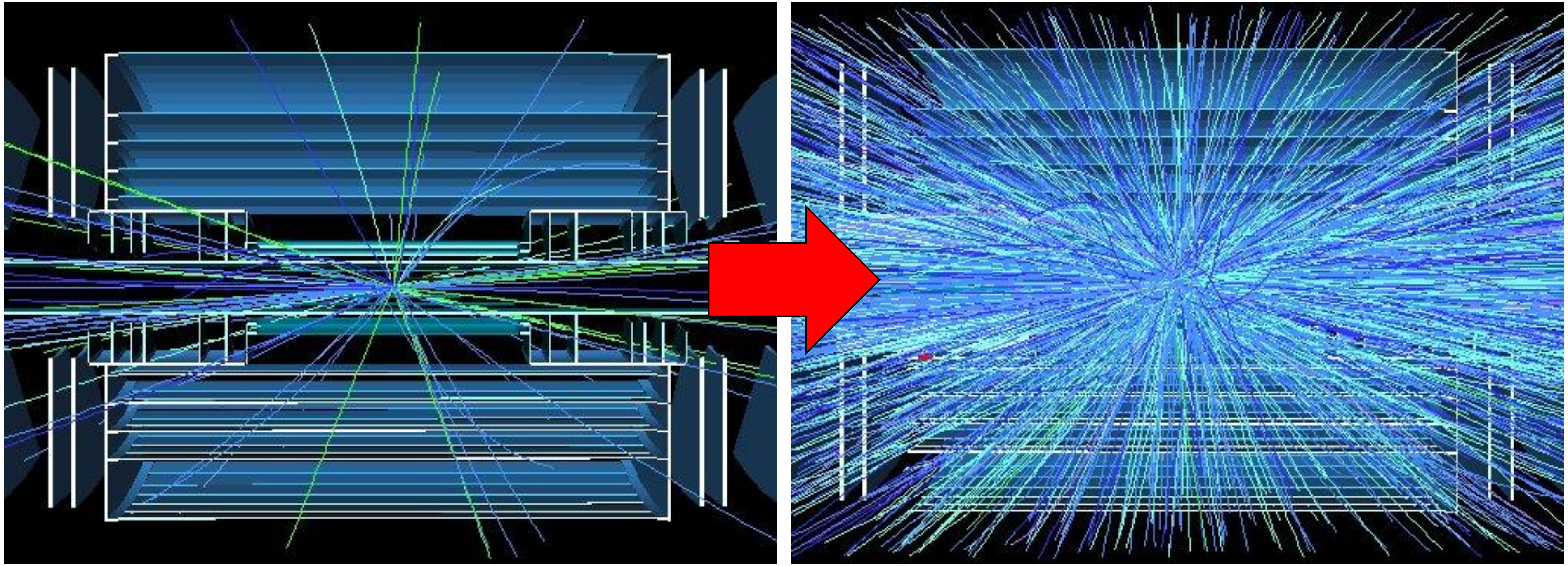


- Integrated luminosity: 200 $\mathrm{fb^{-1}}$ to 300 $\mathrm{fb^{-1}}$ per year
- Total integrated luminosity:: ca. 3000 $\mathrm{fb^{-1}}$

- Finally look to double the energy (HE-LHC)
  16.5+16.5 TeV proton collider in the LHC tunnel

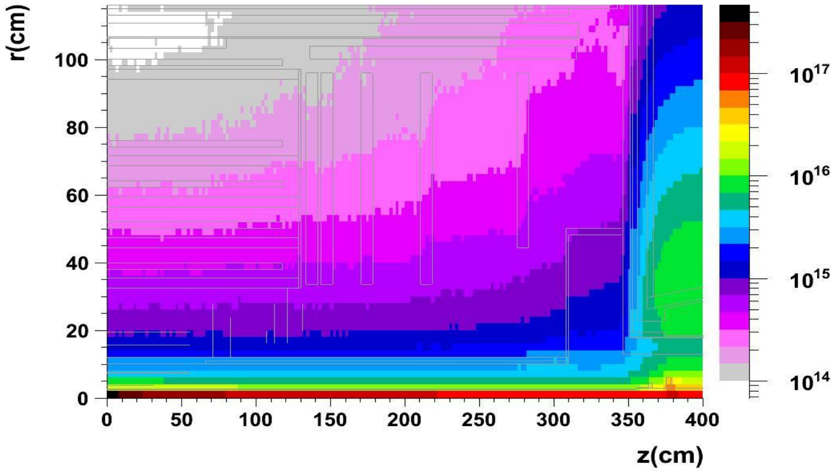
Interaction Simulation

Radiation
Multipicity
Vertexing and tracking precision
PID



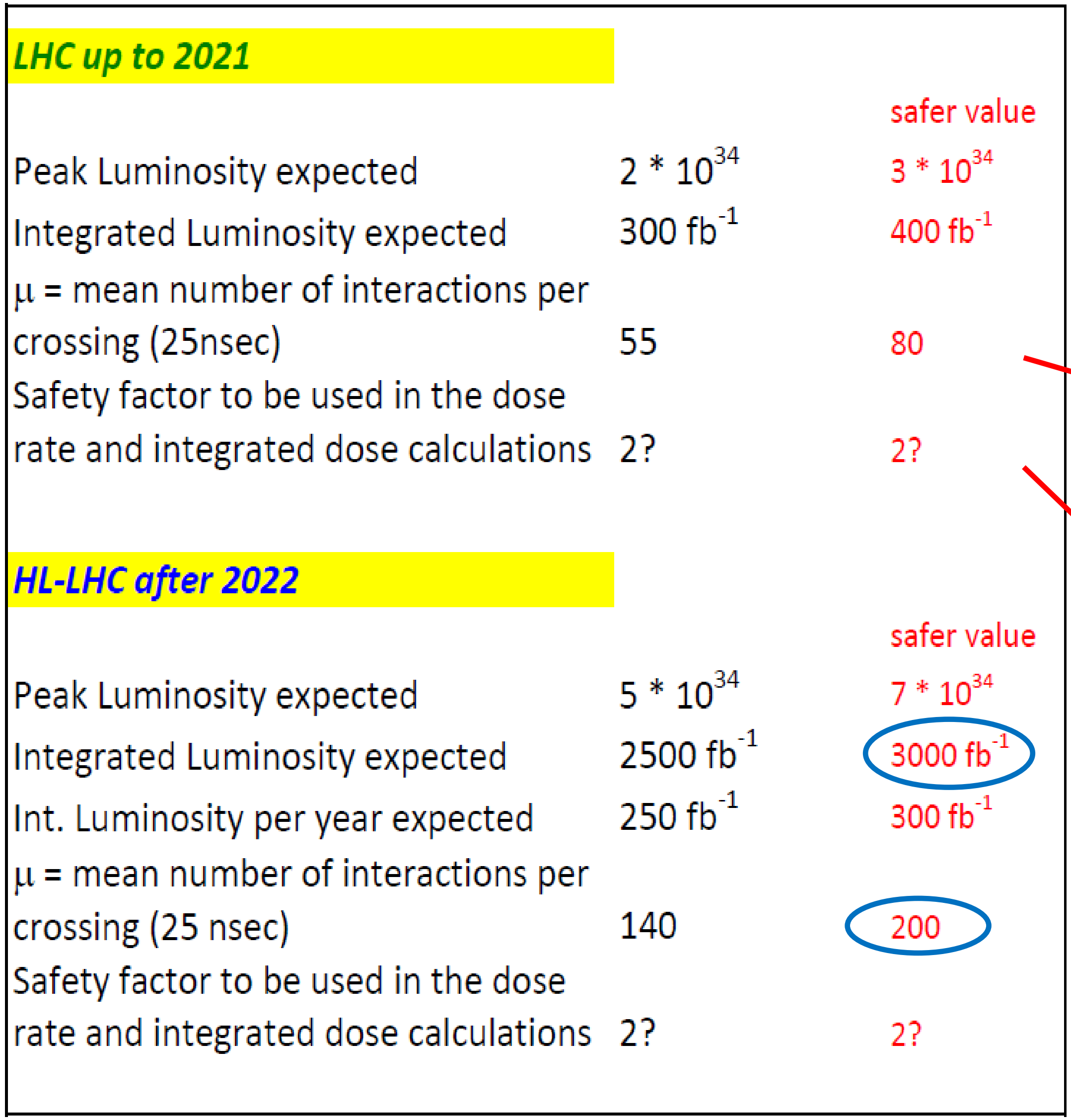
1 MeV neutron eq fluence

At inner pixel radii - target survival to 2-3×10^{16} n_{eq}/cm^2



I. Dawson et al.

Draft Target Specifications



LHC up to 2021

		safer value
Peak Luminosity expected	$2 * 10^{34}$	$3 * 10^{34}$
Integrated Luminosity expected	$300\ fb^{-1}$	$400\ fb^{-1}$
μ = mean number of interactions per crossing (25nsec)	55	80
Safety factor to be used in the dose rate and integrated dose calculations	2?	2?

HL-LHC after 2022

		safer value
Peak Luminosity expected	$5 * 10^{34}$	$7 * 10^{34}$
Integrated Luminosity expected	$2500\ fb^{-1}$	$3000\ fb^{-1}$
Int. Luminosity per year expected	$250\ fb^{-1}$	$300\ fb^{-1}$
μ = mean number of interactions per crossing (25 nsec)	140	200
Safety factor to be used in the dose rate and integrated dose calculations	2?	2?

Plan for occupancy numbers based on this (see µ values below)

Plan integrated dose figures based on this

µ values going with the peak luminosity figure if achieved with 25ns beam crossing

When we calculate the dose figures which are used to specify the radiation hardness of components which can be reliably tested for post-irradiation performance (eg ASICs, silicon sensors, diamond, ...) apply this safety factor to the dose calculations in setting the radiation survival specification

Requirement	Value
Position resolution (µm)	< 20
Power dissipation (mW cm^{-2})	200
Hit rate (GHz)	0.1/1
Timing resolution (ps)	2500
Radiation tolerance ($n_{eq}\ cm^{-2}/Y$)	10^{16}
Low mass (%X_0)	2

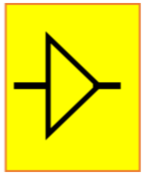
Silicon detectors

A complete detector is made of:

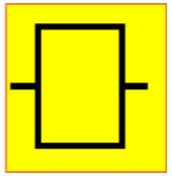
Diodes (reverse biased)

Made in niche foundries (RTO)

Analogue amplifiers

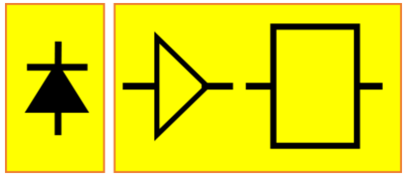


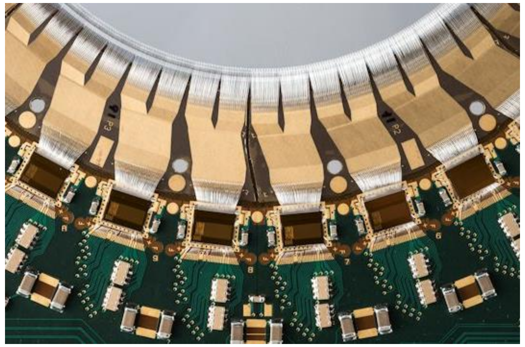
Digital readout

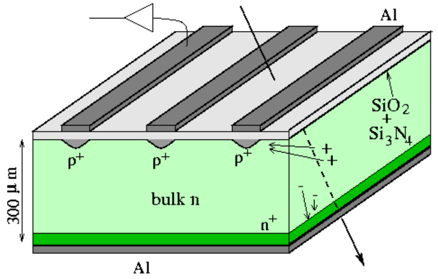


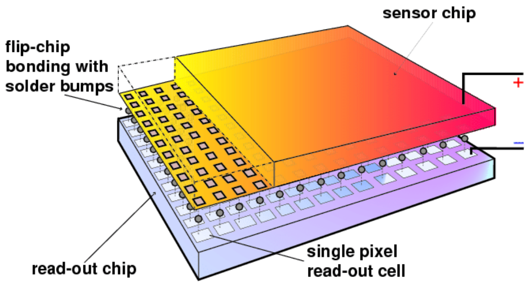
Made in CMOS (industry)

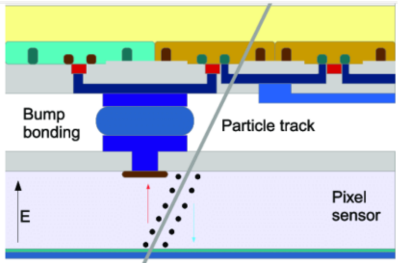
The hybrid solution



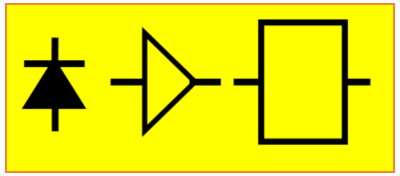


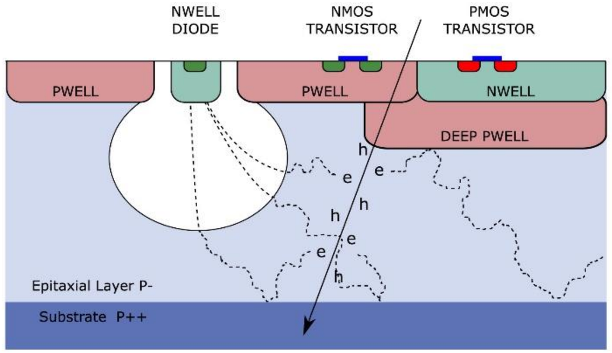


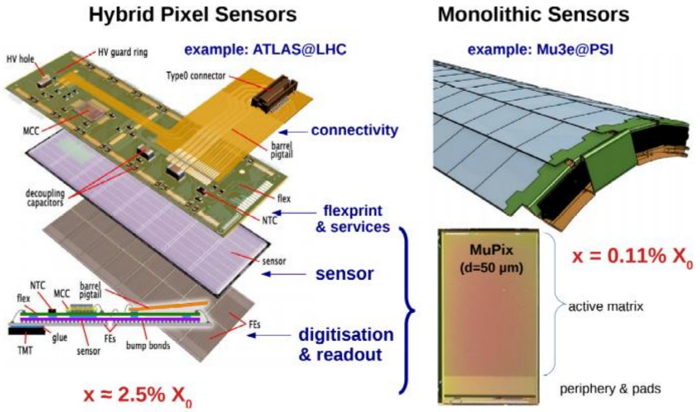




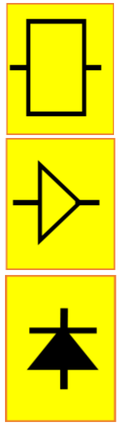
Monolithic solution

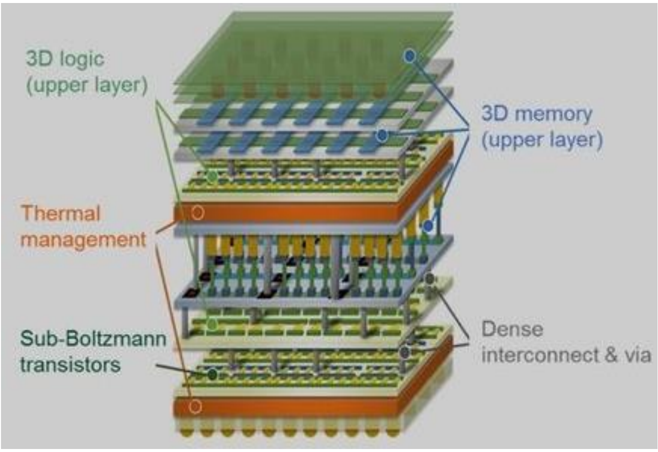






Vertical integration

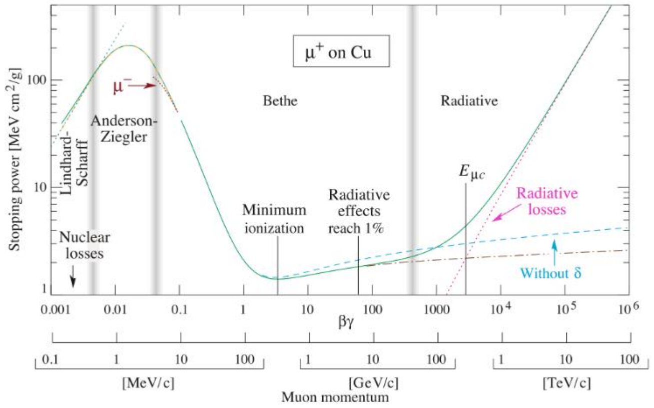


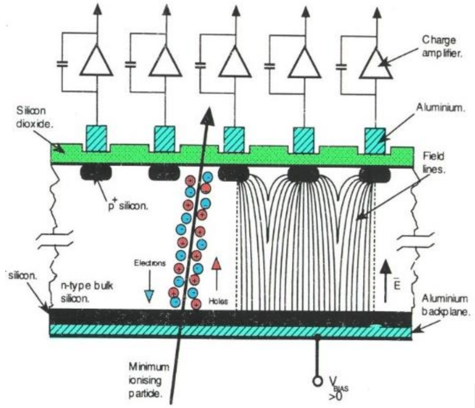


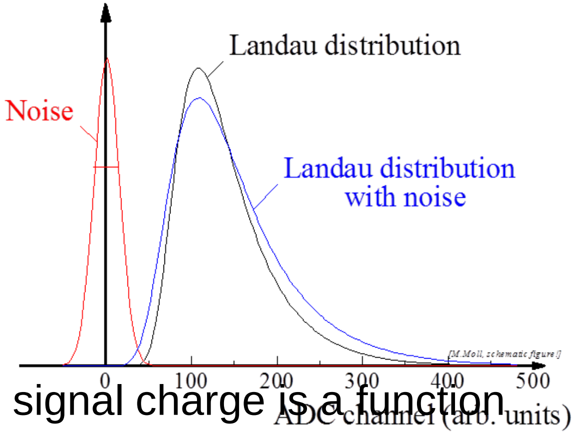
Example industrial development (ASCENT)

G. Casse, Corfu 2023

Diode signal and electronics





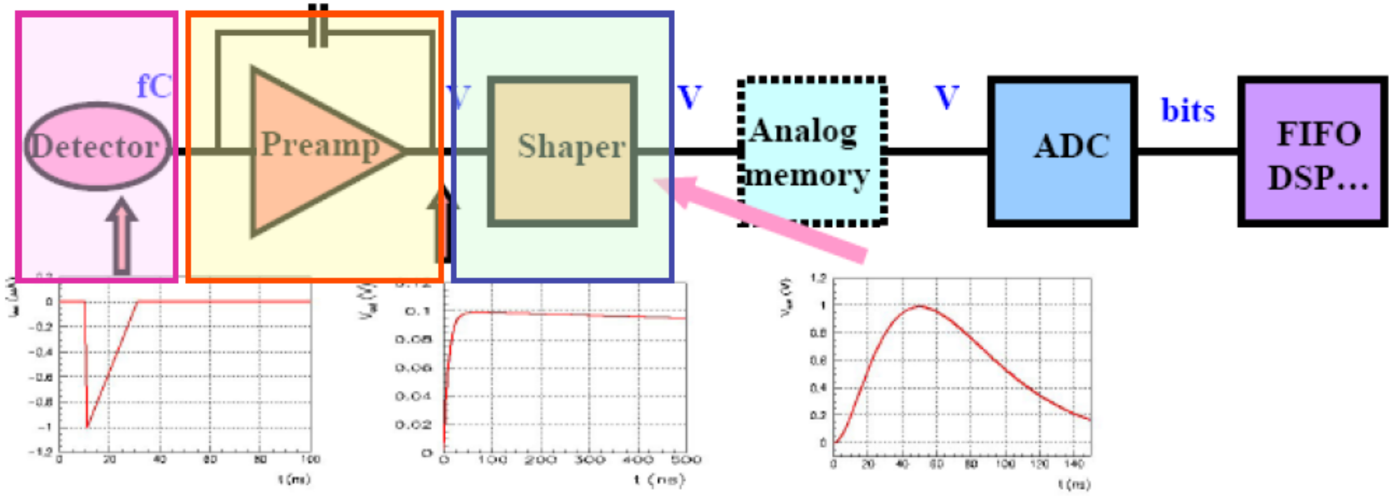


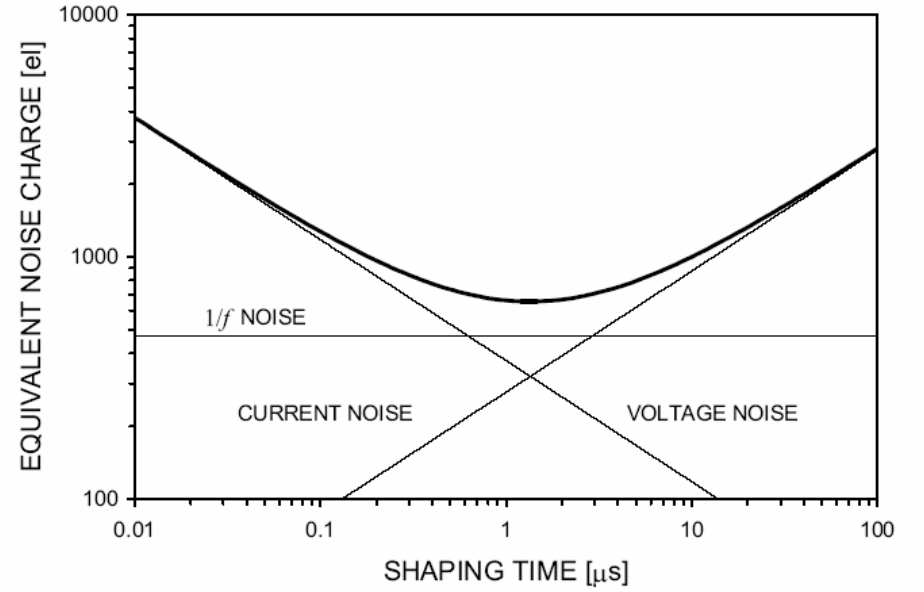
The expected signal charge is a function of the detector

Depleted thickness:

Typical thickness: 100-500 μm

Most probable signal ~ 7.6-38 ke$^-$





C_d = detector capacitance
I_b = bias current
R_p = bias resistor
R_s = strip resistance
V_{na}^2 = Preamplifier noise

$$ENC^{I_b}_{parallel} \approx 108 \cdot \sqrt{I_b(\mu A)\tau(ns)}e^-,$$
$$ENC^{R_p}_{parallel} \approx 24 \cdot \sqrt{\tau(ns)/R_p(M\Omega)}e^-,$$
$$ENC^{R_s}_{series} \approx 24 \cdot C_{tot}(pF) \cdot \sqrt{R_s(\Omega)/\tau(ns)}e^-$$

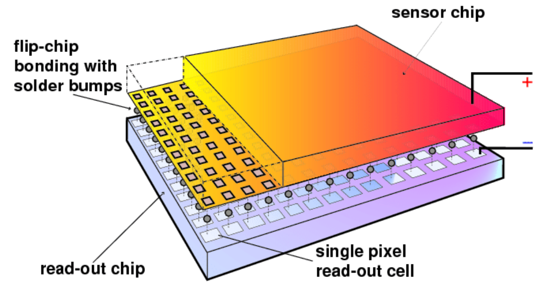
+ front end electronics: $ENC_{fe} = a + bC_d$

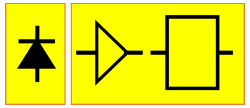
Hybrid sensors

Most used to date.

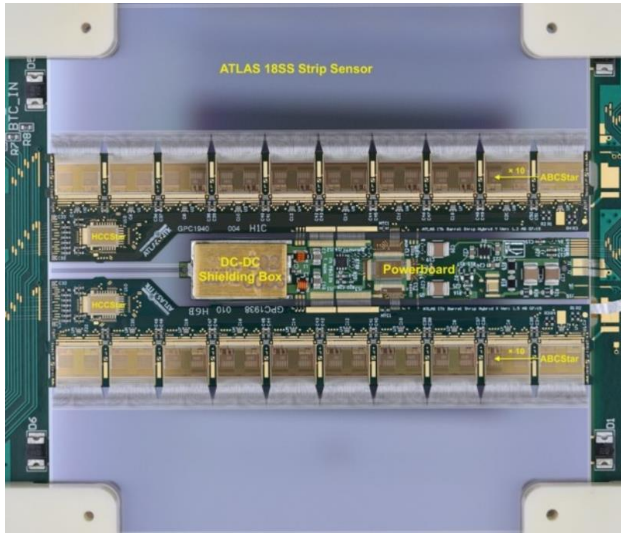
Have satisfied every challenge: resolution, speed, granularity, radiation tolerance. ATLAS, CMS and LHCb upgrades will employ last generation hybrid sensors.

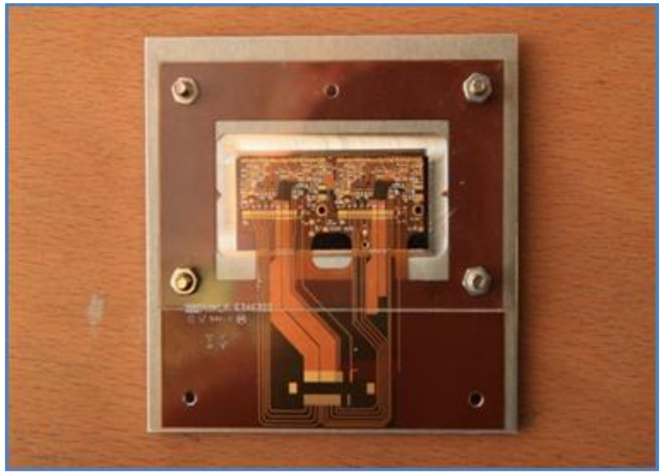
Diodes made by niche manufacturers (CNM, FBK, CIS, Micron UK, Sintef, ….., and HPK).





40 – 110 µm pitch, 1 – 4 cm long strips. Readout: Beetle chip, 0.25 µm CMOS.



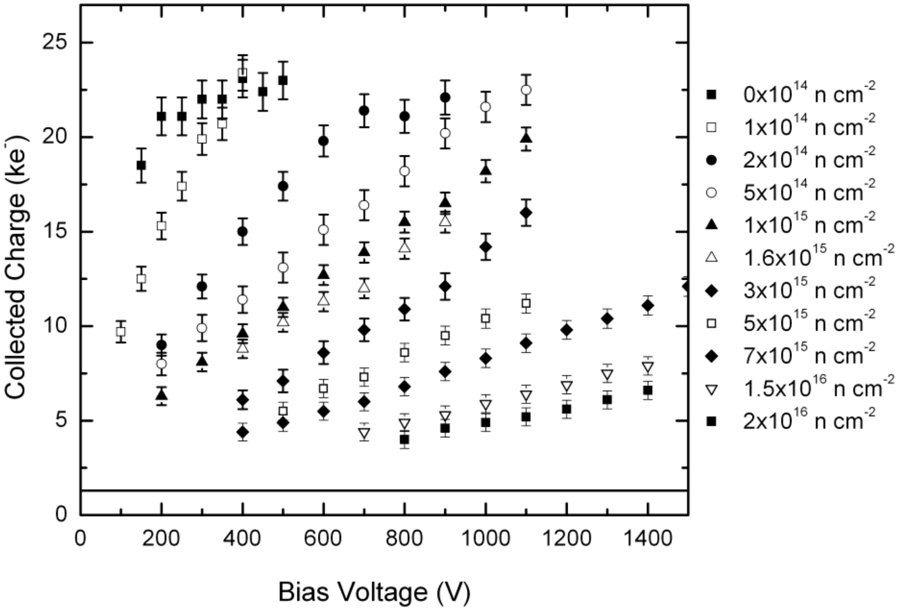


Pixel sensor (200 µm thick) and FE-I4 (400 µm thick) readout hybrid (bump-bonded) assembly. 130 nm CMOS, 20x18.8 mm^2, 26880 pixel, size 50x250 µm^2).

Hybrid sensors: successful development towards unprecedent radiation tolerance

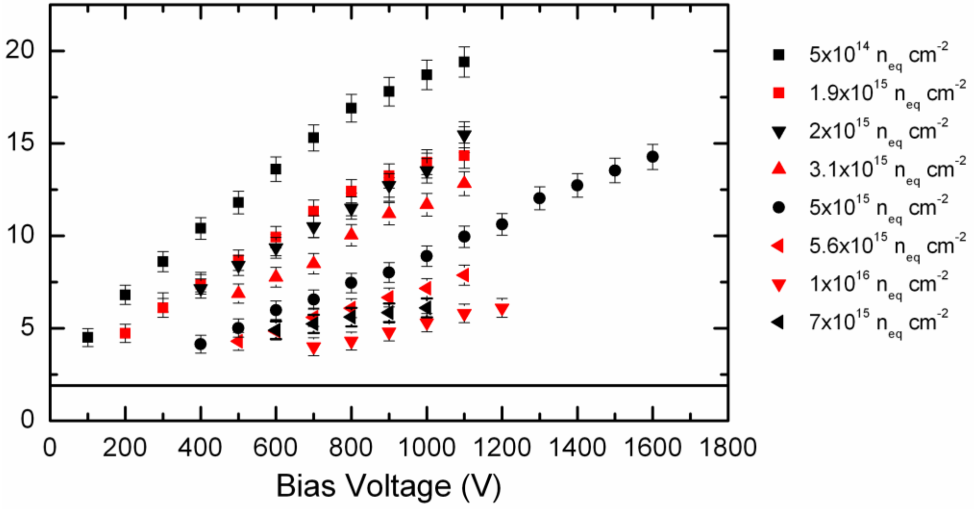
Results with proton irradiated 300 μm n-in-p Micron sensors (up to $1x10^{16}$ n_{eq} cm^{-2})

Irradiated with reactor neutrons



RED: irradiated with 24GeV/c protons

Other: 26MeV protons

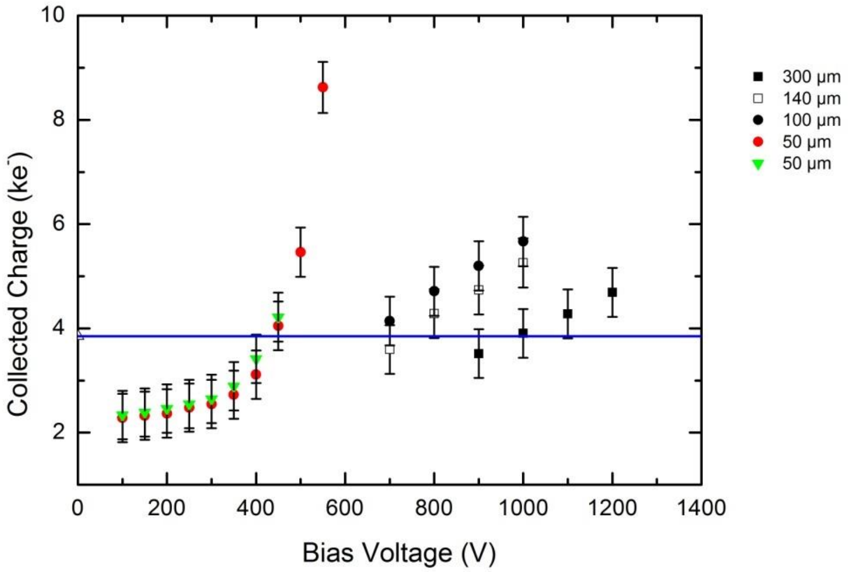


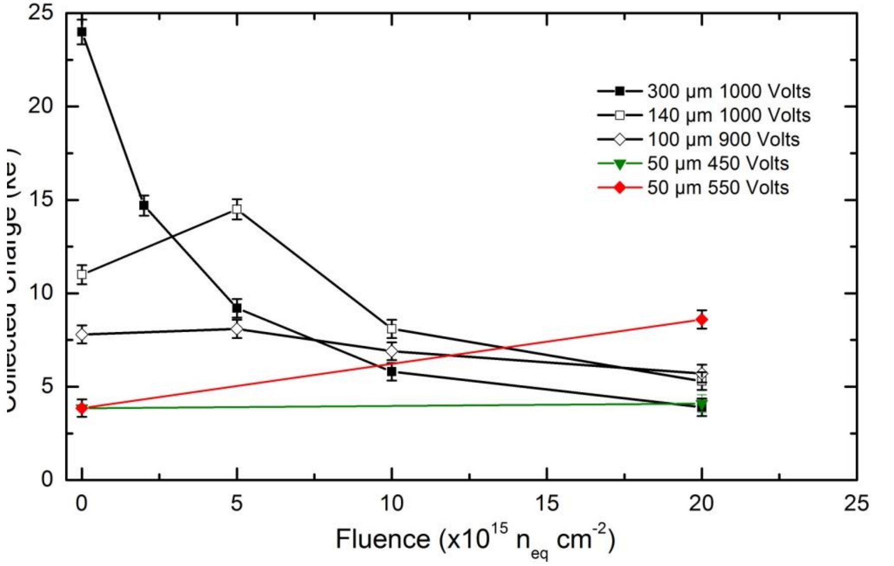
Look at the voltage scale!!

Role of thickness

The onset of Charge Multiplication breaks a few rules, like the proportionality of the signal with thickness.....

Charge degradation vs fluence for silicon sensors with different thicknesses

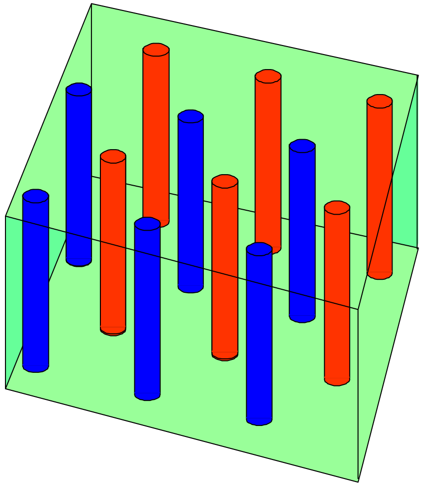




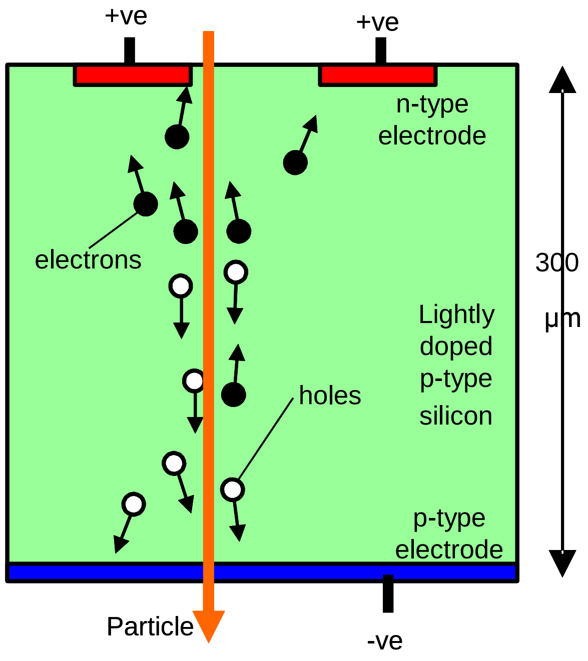
Different detector structure: 3D Detectors

- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30µm:300µm)
- Benefits
  - $V_{depletion}$ (Electrode spacing)^2
  - Collection time ∝ Electrode spacing
  - Reduced charge sharing ∝
- More complicated fabrication - micromachining

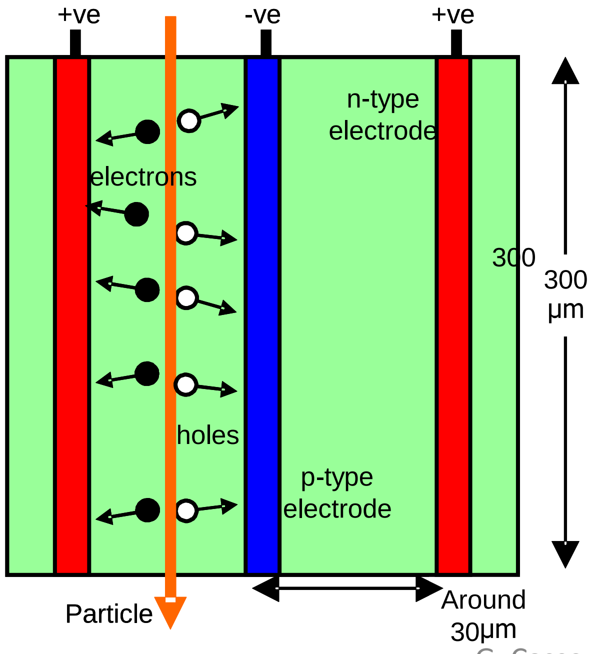
Proposed by S. Parker and C. Kenney of the University of Hawaii in 1995.

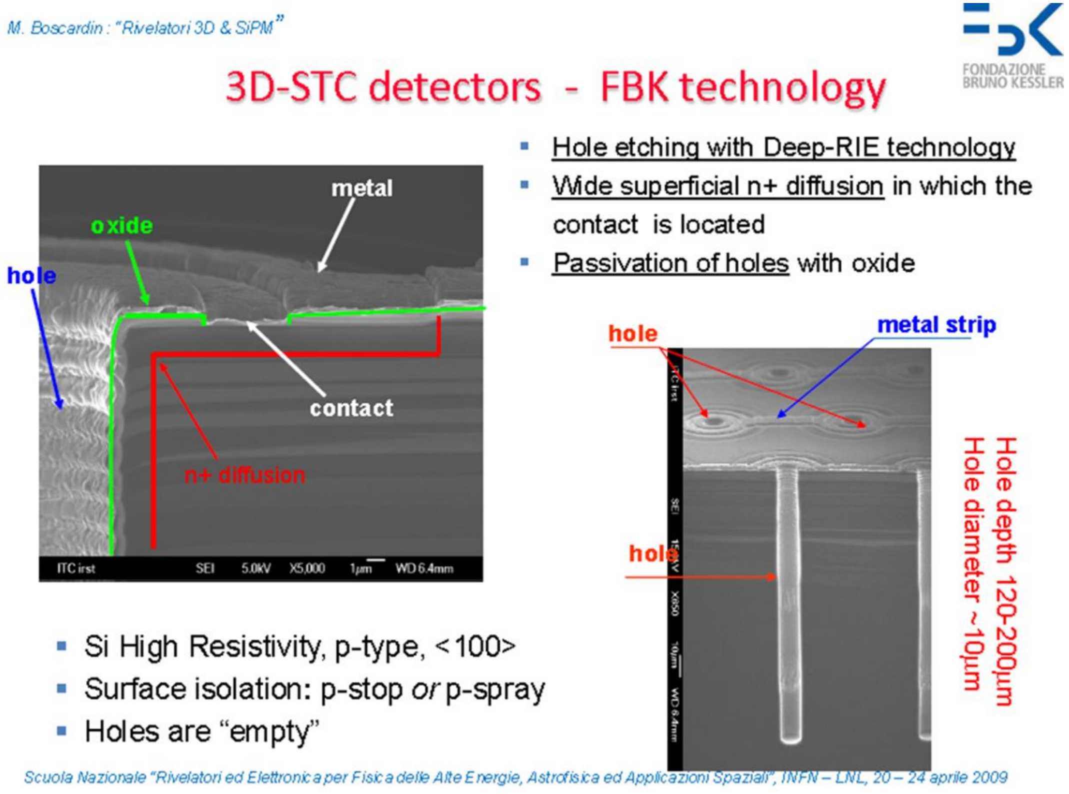


Planar



3D





M. Boscardin : "Rivelatori 3D & SiPM"

FONDAZIONE BRUNO KESSLER

3D-STC detectors - FBK technology

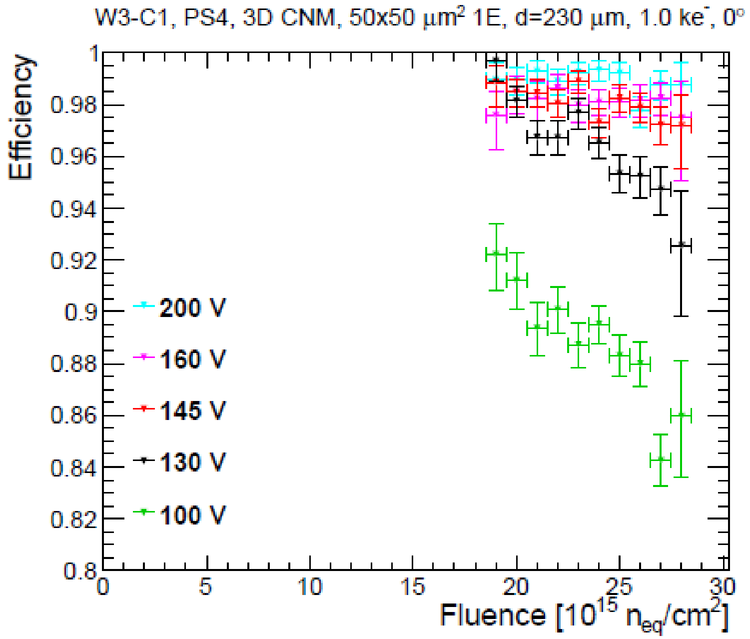
- Hole etching with Deep-RIE technology
- Wide superficial n+ diffusion in which the contact is located
- Passivation of holes with oxide

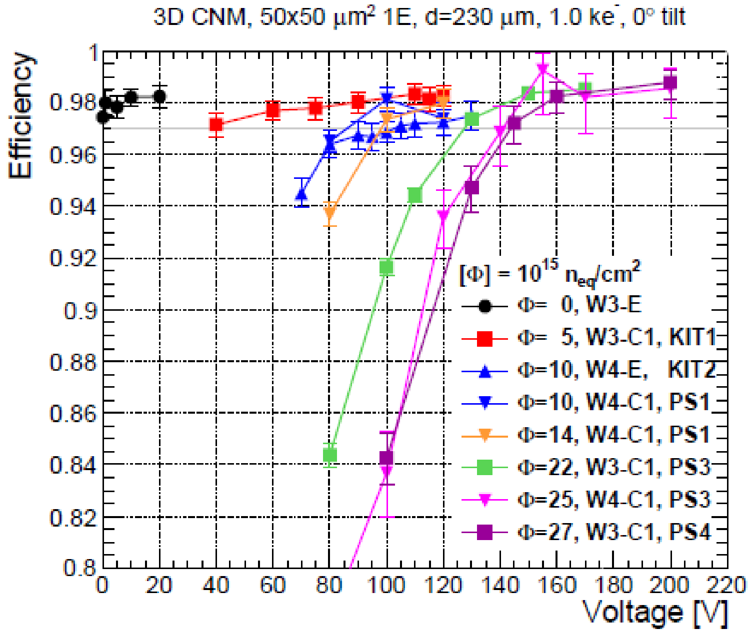
- Si High Resistivity, p-type, <100>
- Surface isolation: p-stop *or* p-spray
- Holes are "empty"

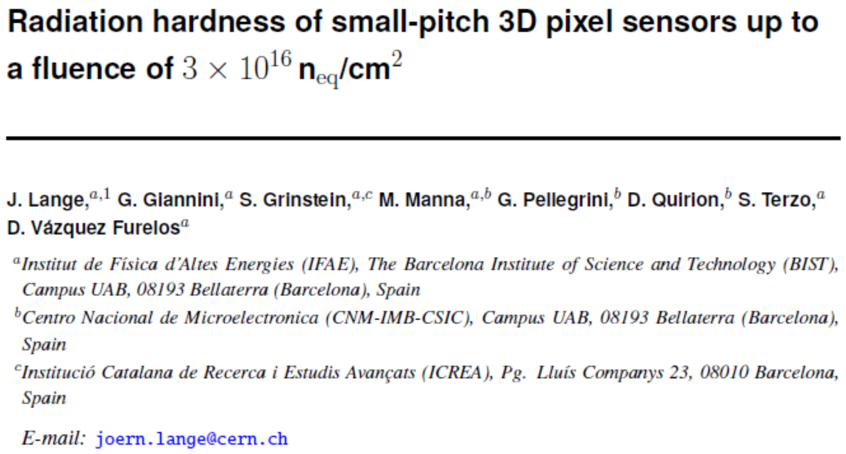
Scuola Nazionale "Rivelatori ed Elettronica per Fisica delle Alte Energie, Astrofisica ed Applicazioni Spaziali", INFN – LNL, 20 – 24 aprile 2009

3d Sensor radiation hardness

- 3D pixel detectors bump bonded to ATLAS FE-I4 show > 98% efficiency after 3×10^{16} n_{eq} cm^{-2}.
- Modern electronics with small feature size show very good radiation tolerance by technology.
- This is also been shown with dedicated irradiation runs with 65 nm circuits (not yet on full assemblies)







Radiation hardness of small-pitch 3D pixel sensors up to a fluence of 3×10^{16} n_{eq}/cm^2

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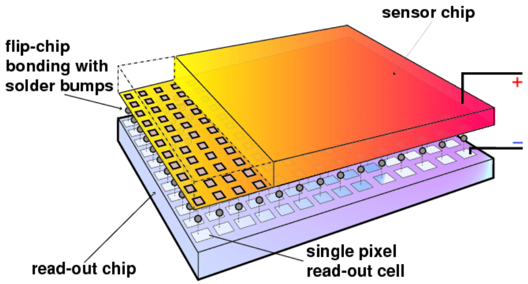
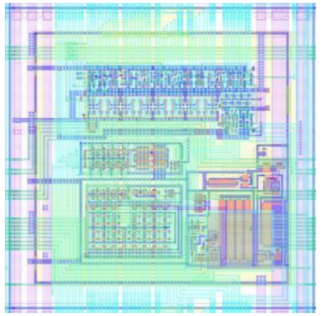
E-mail: `joern.lange@cern.ch`

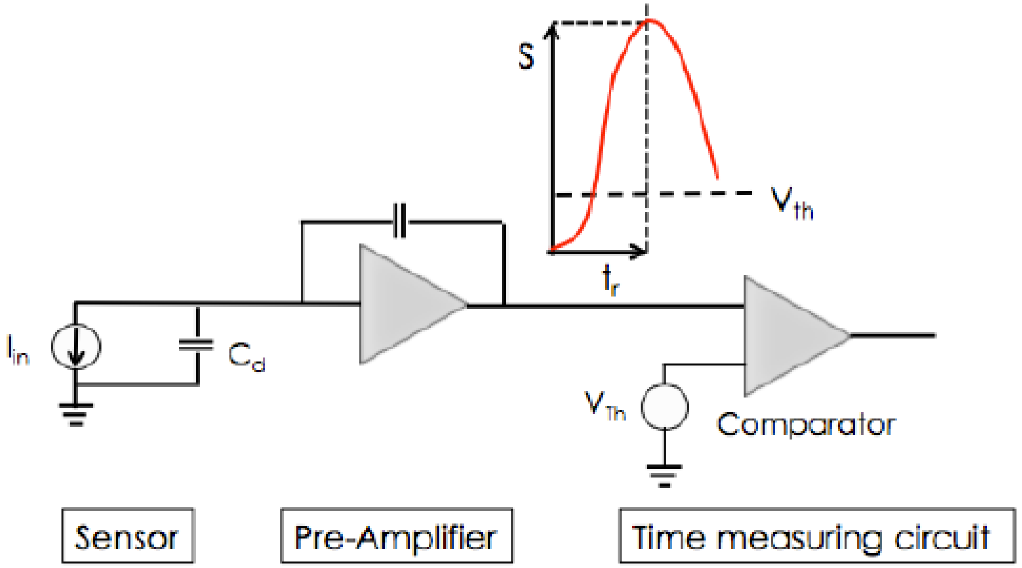
IMB-CNM

Timing (4d Tracking)

Great position resolution (10 μm) combined with < 50 ps time resolution.







Noise and signal are key in term of timing performance.

$\sigma^2_T = \sigma^2_{TW} + \sigma^2_j + \sigma^2_{TDC}$

$\sigma^2_{TW} \propto V_{TH}/S$; V_{TH} = Threshold voltage

S = Signal height

$\sigma^2_j \propto (S/N)^{-1}$; N = Noise

σ^2_{TDC} ; Not considered

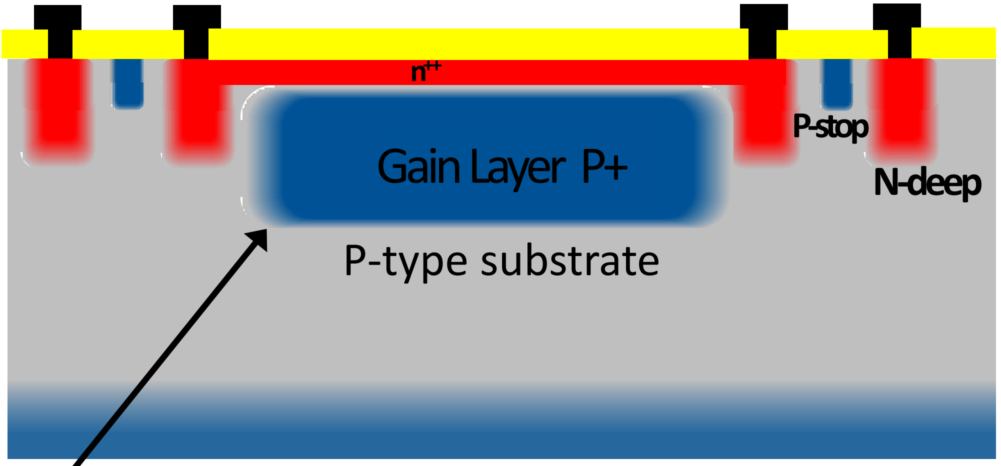
LGAD: introduction

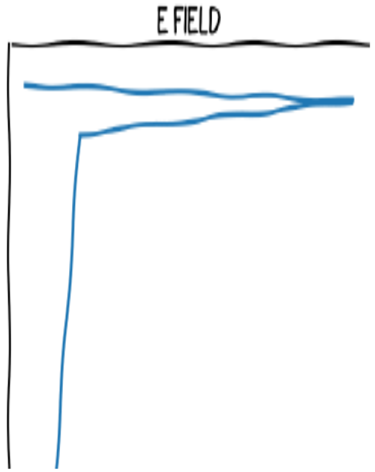
Initial developments with CNM, FBK

LGAD = Silicon detector provided with internal Gain in the range ~ 10 - 20

The basic structure is based on a standard p-i-n planar junction

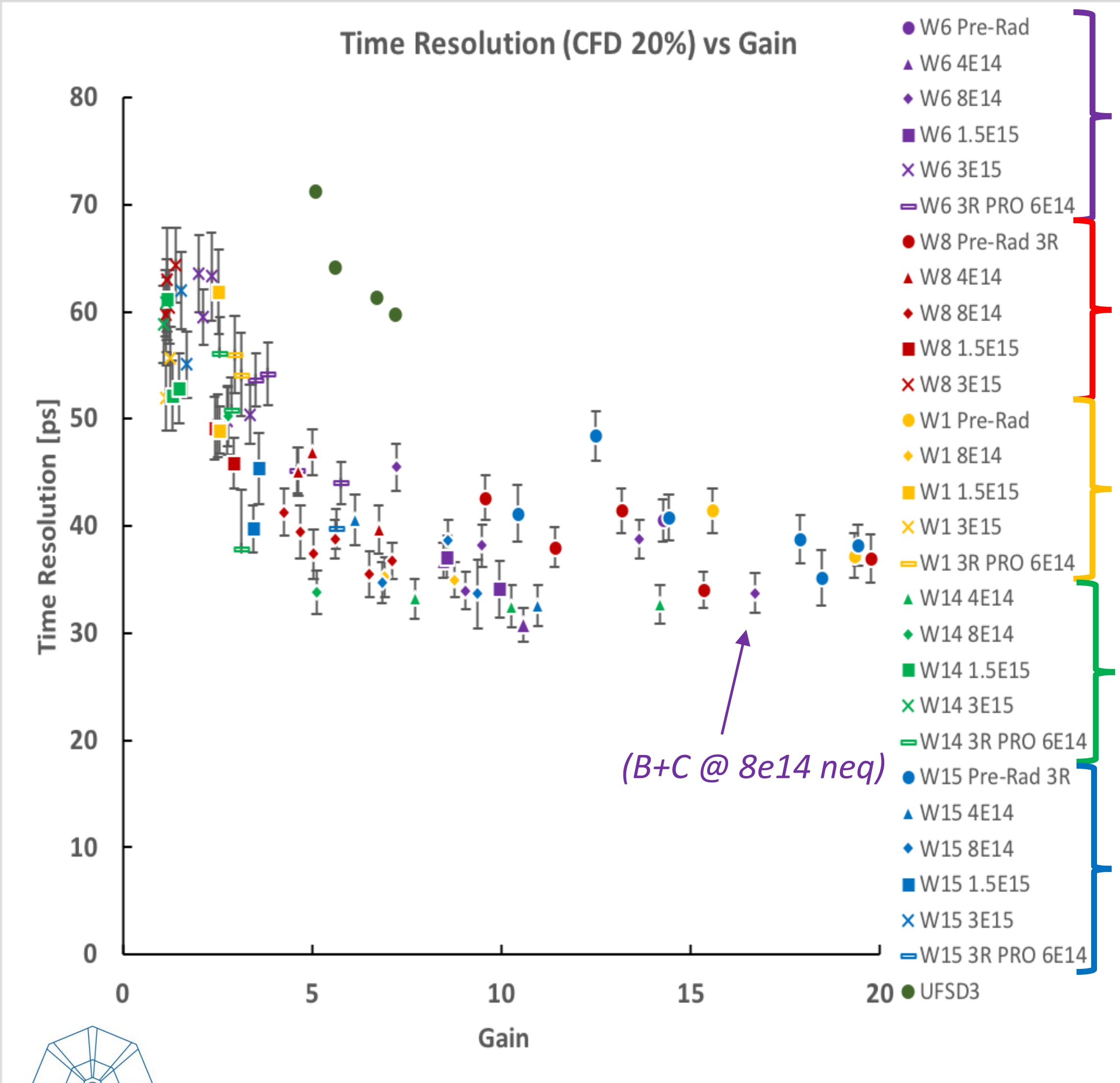
A “multiplication region” or “**gain layer**” is included in the structure (local doping enrichment)





High-Field region: Electric Field > 2e5 V/cm to activate the impact ionizing multiplication

Radiation Hardness: Time Resolution



(B+C @ 8e14 neq)

Boron + Carbon co-impantation

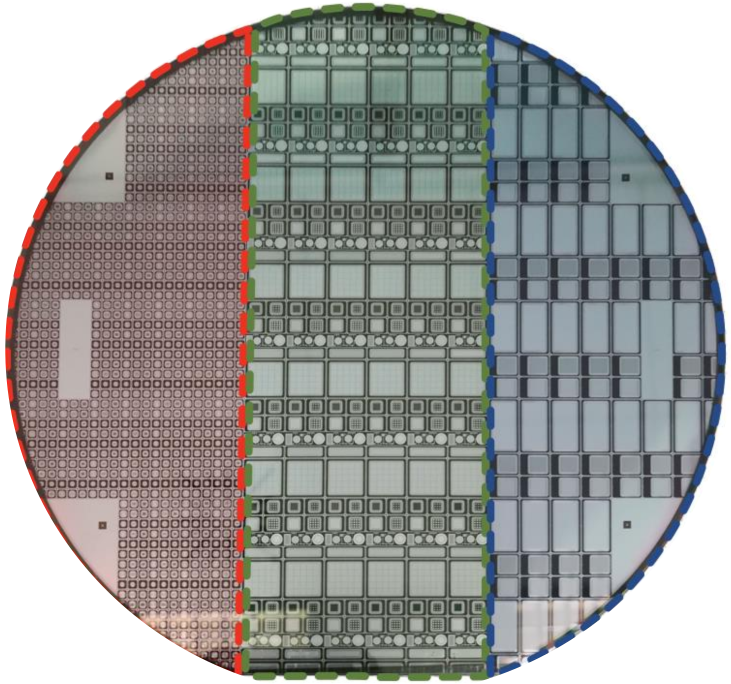
Boron (wide Gain implant profile)

Boron (narrow Gain profile)

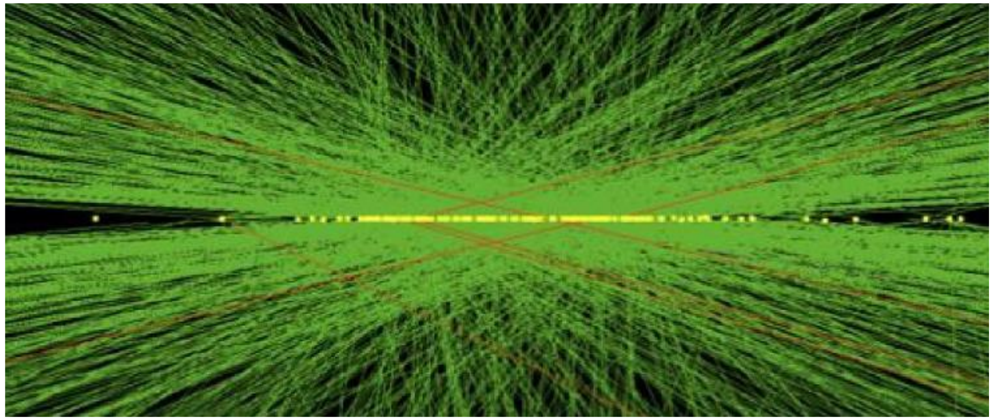
Gallium

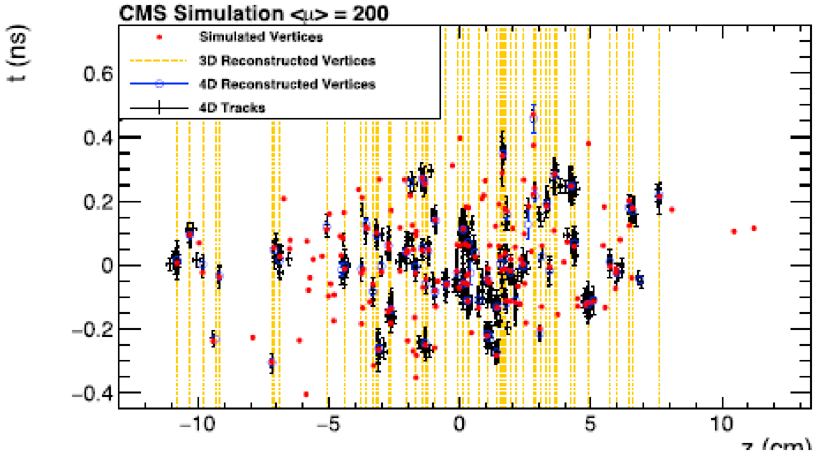
Gallium + Carbon co-implantation

Carbon co-implantation mitigates the acceptor removal effect and preserves the time resolution up to 8e14 neq/cm2

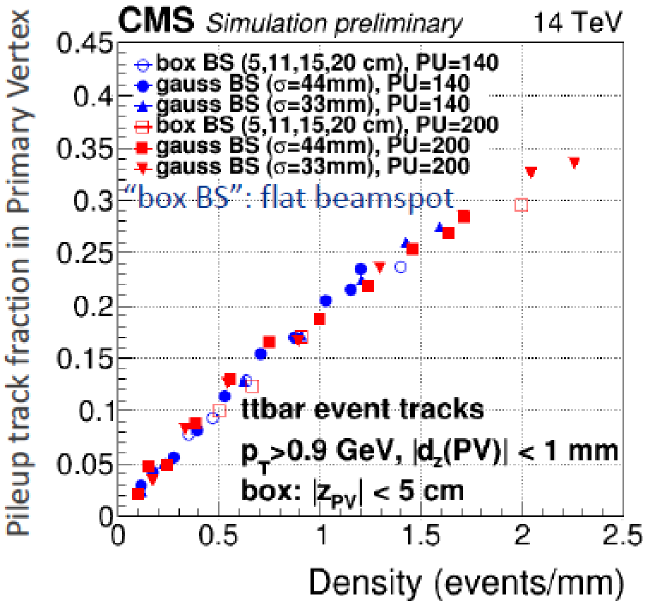


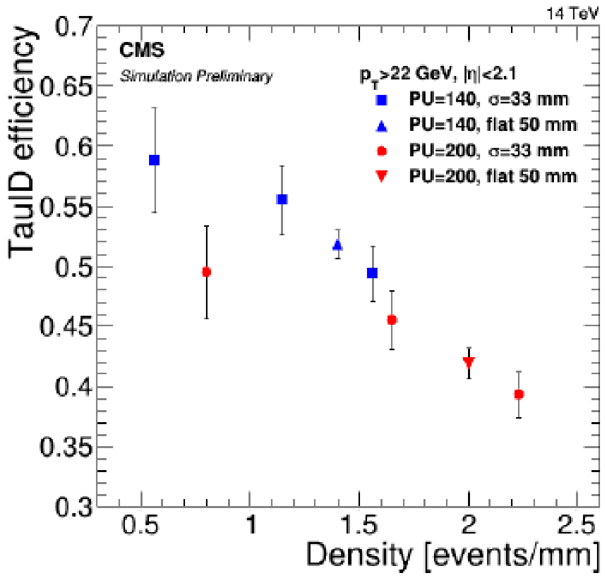
G. Casse, Corfu 2023

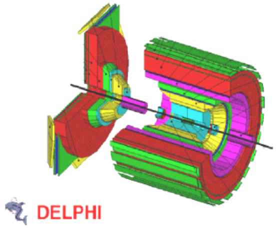




<μ>	4D Merged Vertex Fraction	3D Merged Vertex Fraction	Ratio of 3D/4D
50	0.5%	3.3%	6.6
200	1.5%	13.4%	8.9





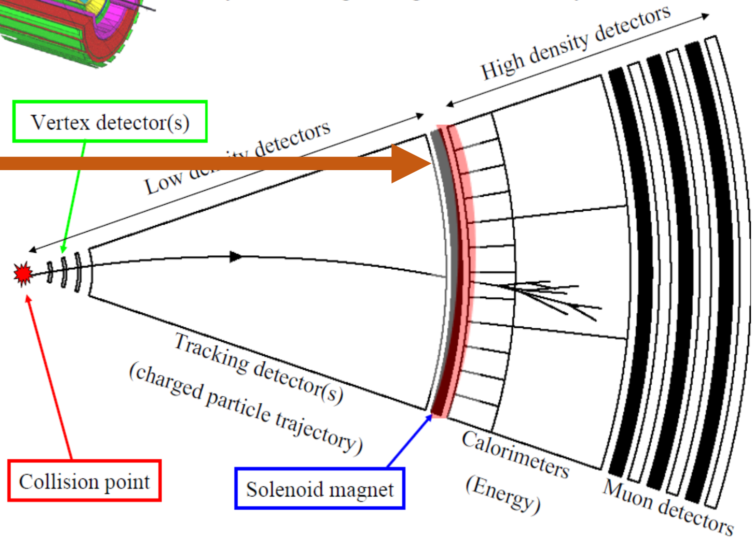


Global detector layout:

- barrel-shape surrounding beam-pipe
- 2 cone- or wheel-shaped end-caps

Nearly 4π coverage and good accessibility!

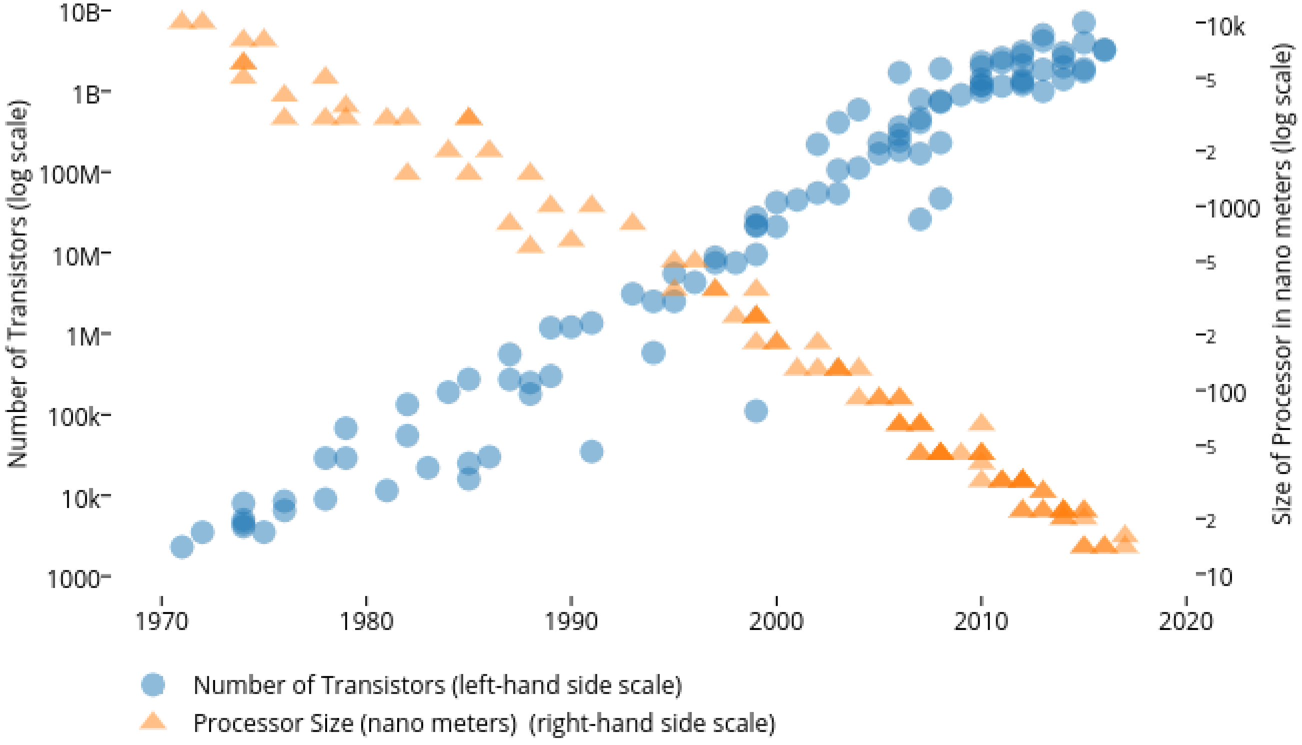
New concept: Timing layer



Microelectronics: the Moore's law

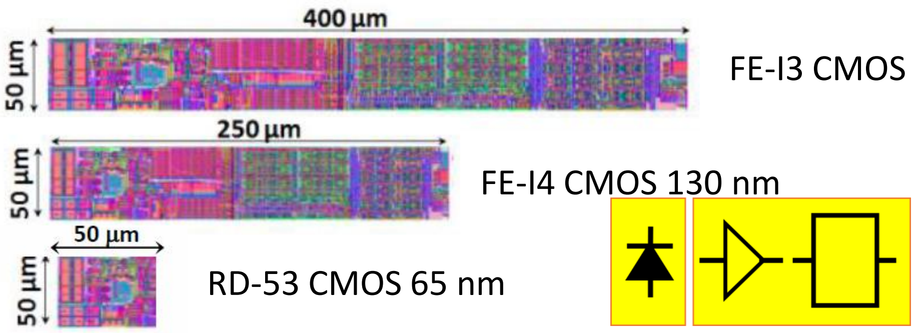
Microelectronics evolved fast (evolution here is entirely independent on Physics needs)

- Moores law made transistors ever smaller



Mosfet Scaling in microelectronics enabled, together with R&D in the sensor (diode), the accelerated improvement of detectors for Physics.

Moore’s law in electronics for pixel sensors



One ‘lucky’ effect: smaller CMOS nodes are intrinsically more robust to radiation

Name	D-OMEGA Ion	LHC1	FE-I3	FE-I4	RD53A	RD53(B)
Year	1991	~1996	~2005	~2011	2017	**2019**
Technology Node	3 µm	1µ	0.25 µm	0.13 µm	65 nm	**65 nm**
Chip size	8.3x6.6 mm^2	8x6.35 mm^2	10.8x7.6 mm^2	10.2x19 mm^2	20x10mm^2	**20x20mm^2**
Pixel size	75x500 µm^2	50x500 µm^2	50x400 µm^2	50x250 µm^2	50x50 µm^2	**50x50 µm^2**
Pixel array	16x63	16x127	18x160	80x336	400x198	**400x396**
Transistor count	???	800k	3.5M	80M	311M	**600M**

T. Hemperek, Future of Tracking, Oxford 1-2 April 2019.

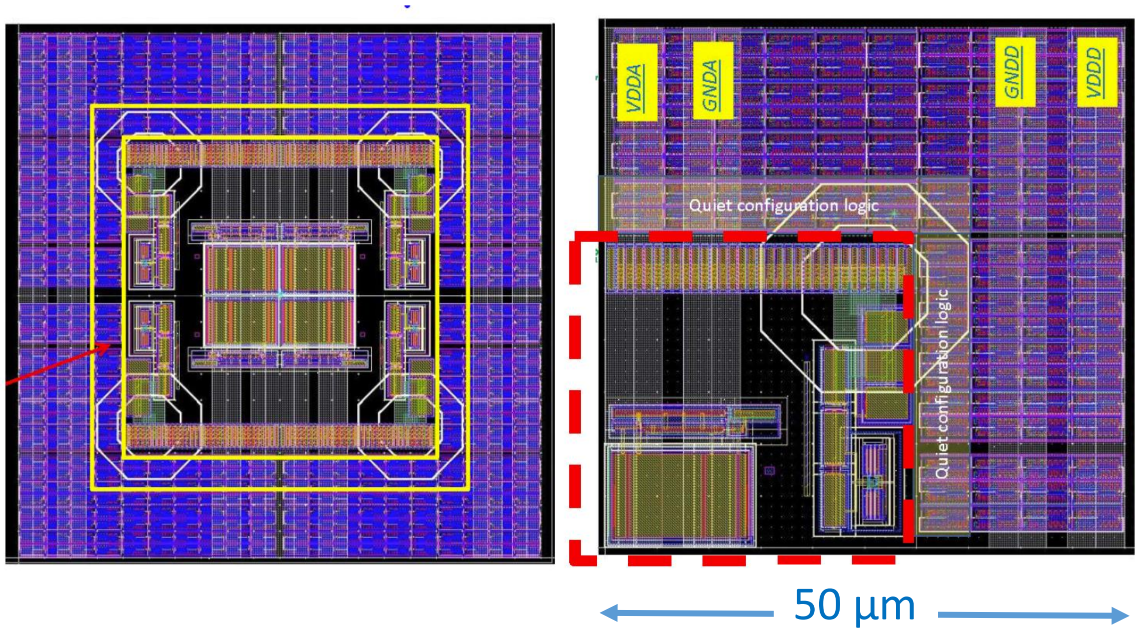
CMOS and detectors today

State-of-the-art

Moving to smaller nodes (e.g. 28nm) with a mixed signal chip is not going to be easy or maybe convenient.

RD53 **65 nm CMOS** pixel readout chip for extreme data rates and radiation levels (V. Re et al., CERN/RD53 collaboration)

Advanced readout chip for the pixel layers of ATLAS and CMS Upgrades at CERN

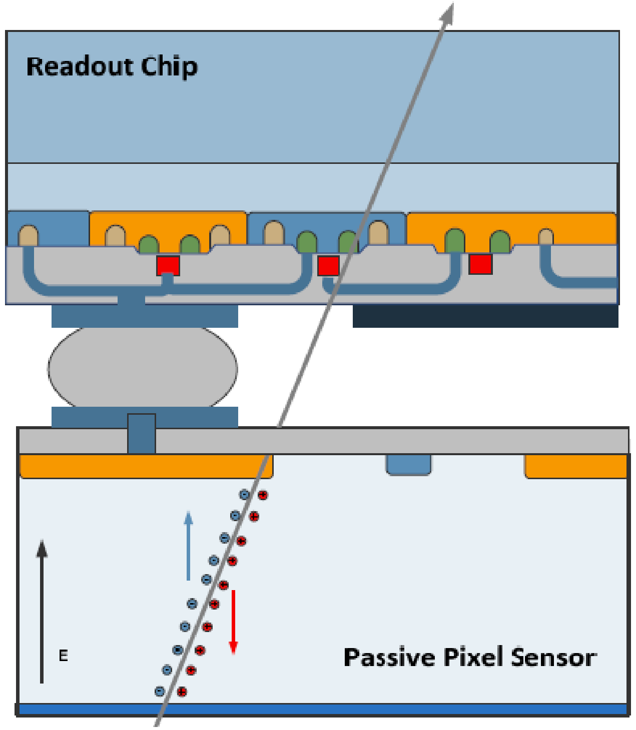


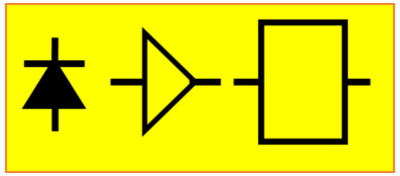
Expected position resolution > 15 µm.

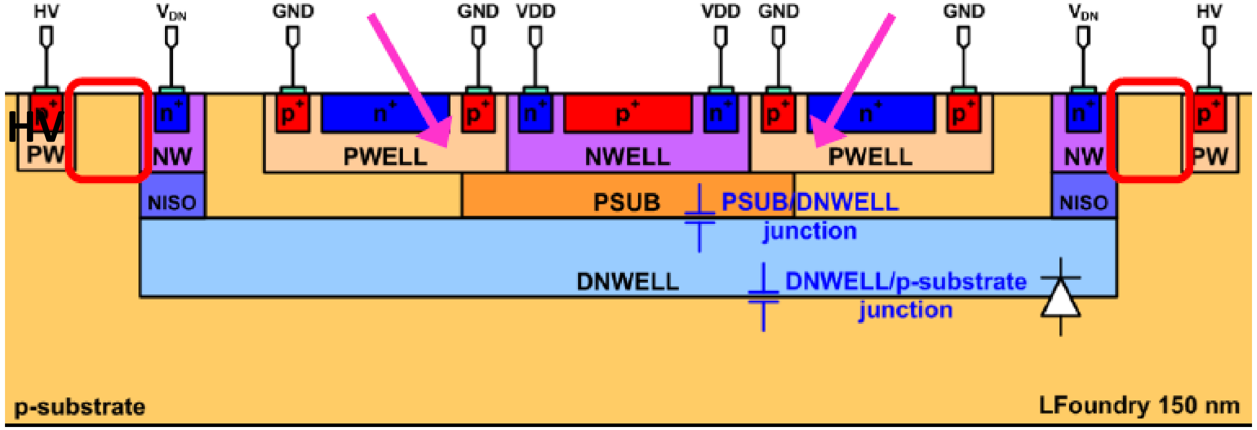
Thanks to small (65 nm) feature size, 600M transistors in total, most in the digital section. The analogue area needs much larger transistors!!

The pixel size cannot scale down with the technology feature size.

Monolithic sensors: technology gaining application





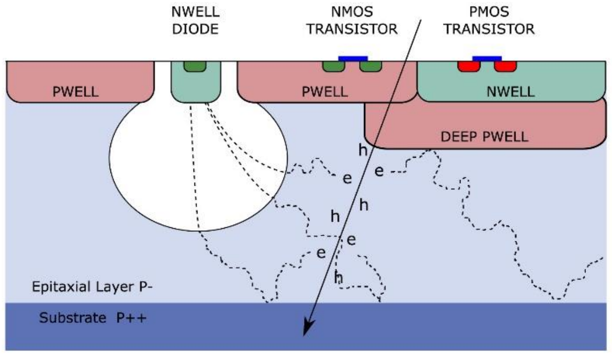


Available technology nodes: Tower (180 nm, 65 nm), LF (150 nm, 110 nm), IHP microelectronics (RI) …

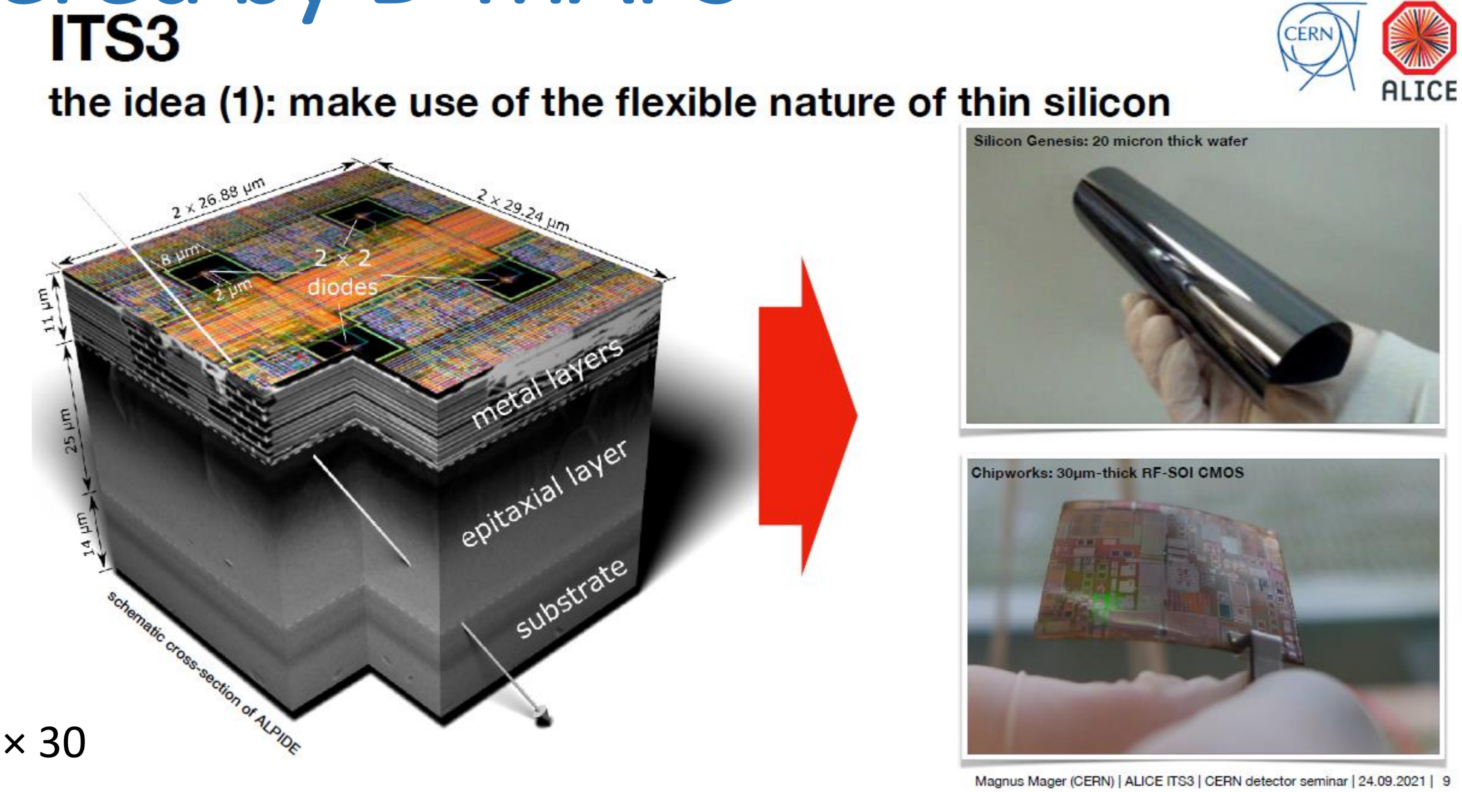
Obvious advantages of monolithic sensors (DMAPS, HV-CMOS, …):
Lower mass
Ease of deployment
Cost
Manufacturing in industrial CMOS sites
Small pixel size

To make them competitive to hybrid sensors:
Achieve high radiation tolerance
Demonstrate timing resolution (with and without multiplication layer).

A lot of *flexibility* is offered by D-MAPS



Pixel size (μm^2)	28 x 28	
Sensor thickness (µm)	50	50
Spatial resolution (µm)	5	10
Dimensions (mm^2)	15 × 30	15 × 30
Power density ($mW\ cm^{-2}$)	300	100
Time resolution (µs)	30	30
Detection efficiency (%)	99	99
Fake hit rate	10^{-5}	10^{-5}
TID radiation hardness (krad)	2700	100
NIEL radiation hardness	1.7×10^{13}	10^{12}



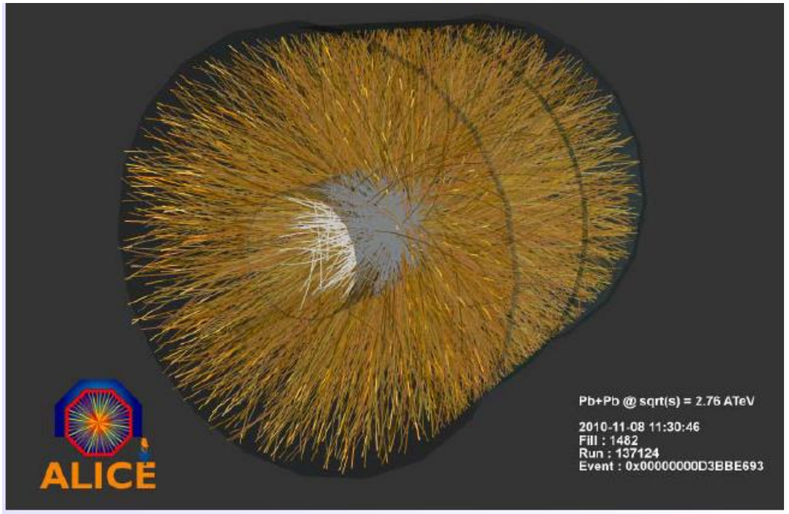
ITS3

the idea (1): make use of the flexible nature of thin silicon

Silicon Genesis: 20 micron thick wafer

Chipworks: 30µm-thick RF-SOI CMOS

Magnus Mager (CERN) | ALICE ITS3 | CERN detector seminar | 24.09.2021 | 9



Radiation tolerance (and timing) for MAPS: Apply High Voltage

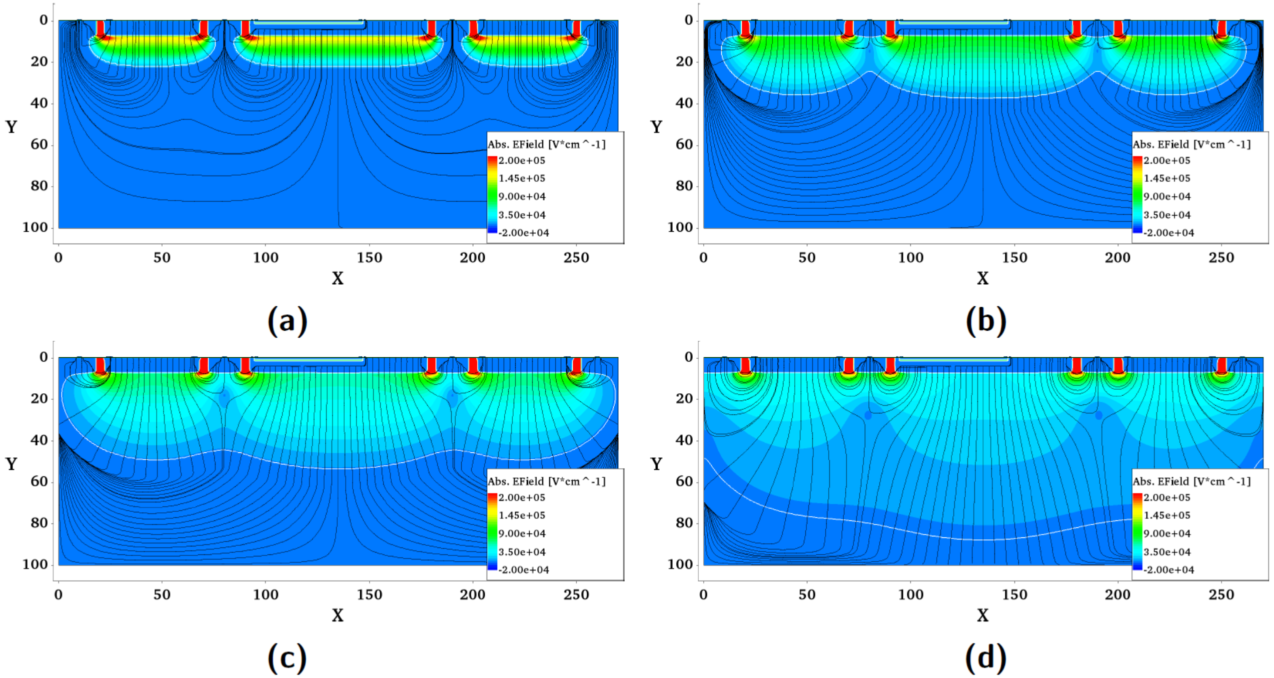
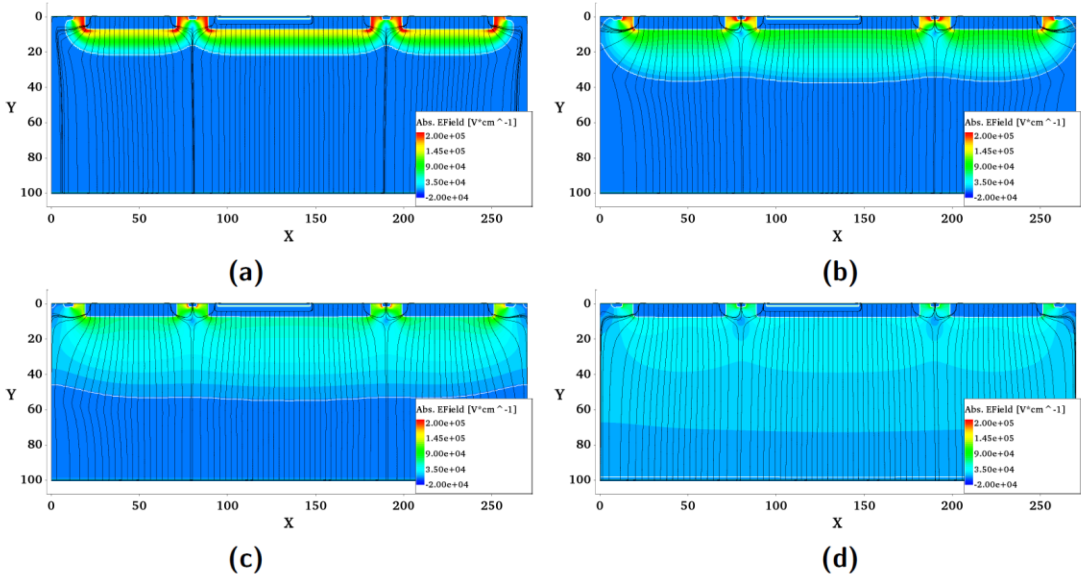


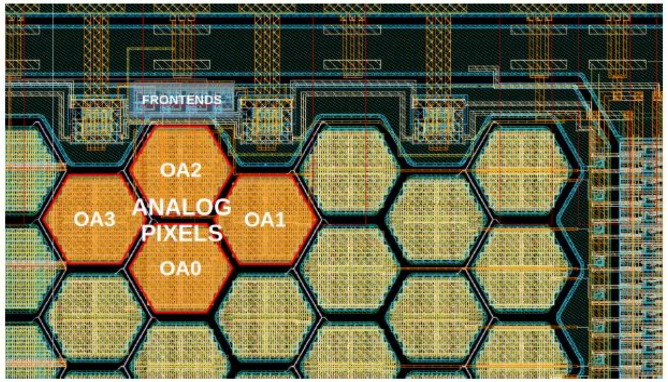
Figure 5.8: Absolute electric field strength of H35DEMO for resistivities 20 (a), 80 (b), 200 (c) and 1000 Ωcm (d), biased from the top at −120 V for the standard layout.

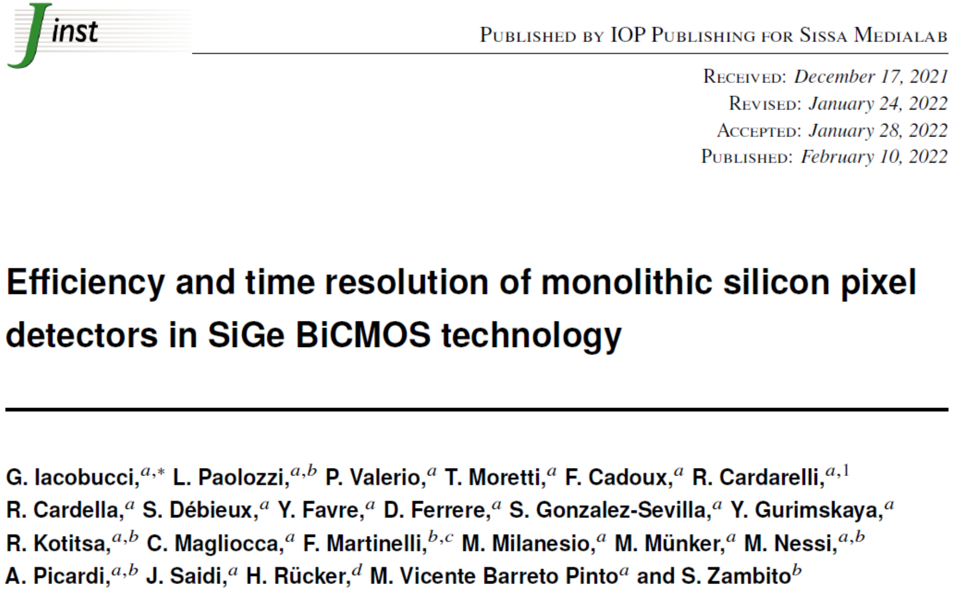
From Lingxin Meng
PhD thesis.



Over 600V on a 200µm thick substrate achieved.

MAPS + Timing

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Accepted: *January 28, 2022*
Published: *February 10, 2022*

Efficiency and time resolution of monolithic silicon pixel detectors in SiGe BiCMOS technology

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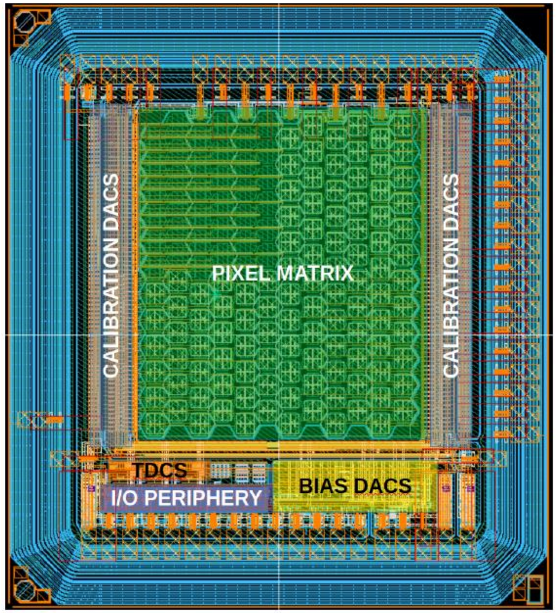


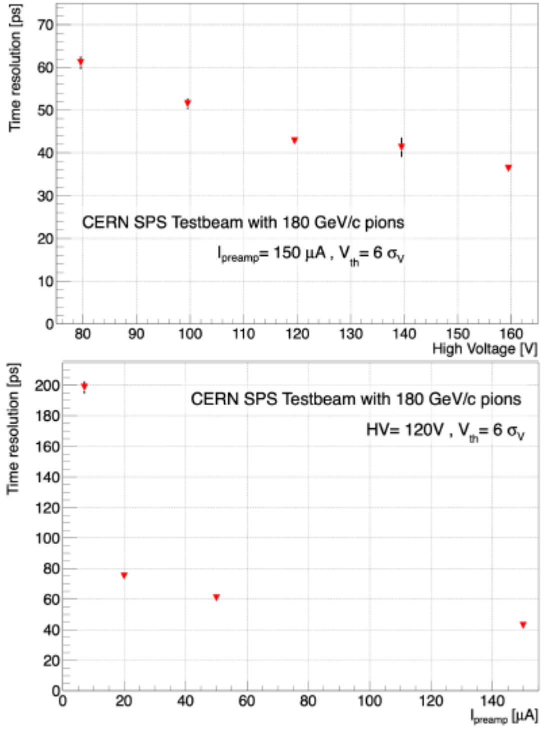


Figure 14. Top: time resolution as a function of sensor bias voltage at $I_{\text{preamp}} = 150\,\mu\text{A}$. Bottom: time resolution as a function of I_{preamp} for sensor bias voltage $HV = 120\ V$. The time resolution is defined as $(\sigma_{\text{TOA0-TOA1}})/\sqrt{2}$. It refers to the Gaussian component of the data, which is approximately 95% of the total.

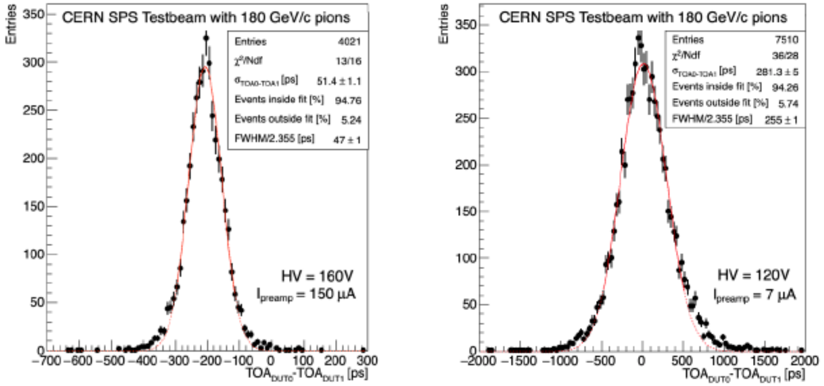
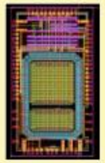


Figure 13. TOA difference between pixels OA0 of DUT0 and DUT1 after time-walk correction for the two working points reported in the panels. A constant arbitrary offset is present, which is irrelevant for the time-resolution calculation. The red lines show the results of the Gaussian fit using only the bins with more than 25% of the entries in the maximum of the distribution. The full red lines show the ranges used for the fits, while the dashed red lines allow the estimation of the non-Gaussian components in the tails.

Monolithic SiGe BiCMOS for timing

Monolithic prototypes with SiGe BiCMOS (without internal gain layer)

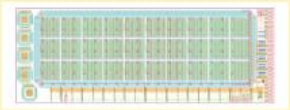
2016



200ps

- 1 and 0.5 mm^2 pixels
- Discriminator output

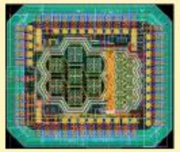
2017



110ps

- 30 pixels 500x500µm^2
- 100ps TDC +I/O logic

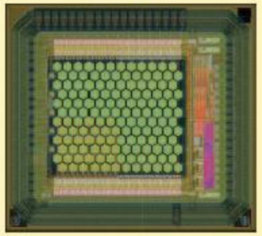
2018



50ps

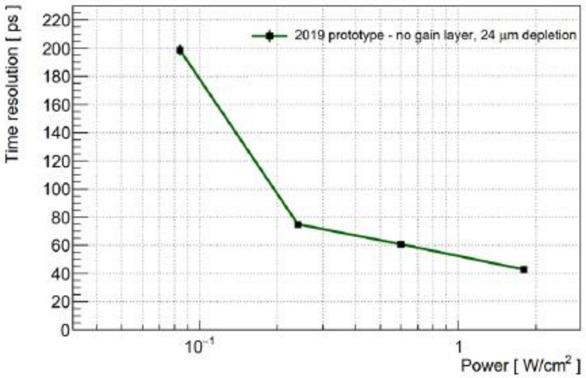
- Hexagonal pixels 65µm and 130µm side
- Discriminator output

2019



36 ps

- Hexagonal pixels 65µm side
- 30ps TDC +I/O logic
- Analog channels



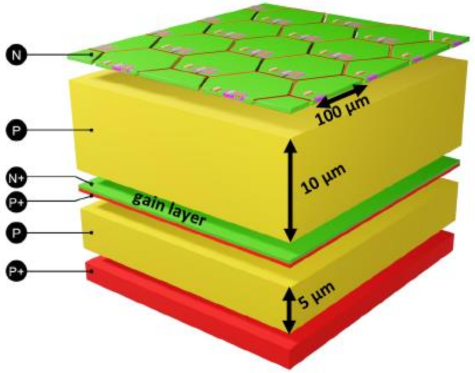
Sensor with no gain test beam results: JINST **P02019** *2022*

ncept

Multi-Junction Picosecond-Avalanche Detector with continuous deep gain layer.

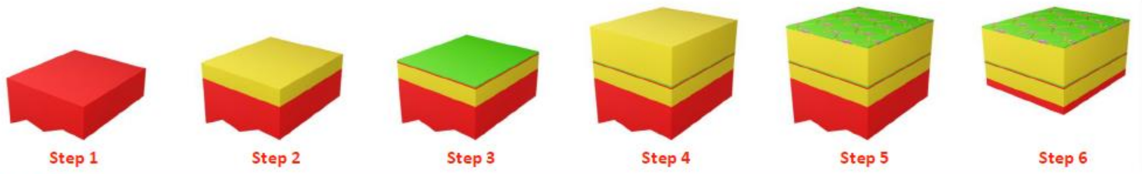
De-correlation from implant size/geometry

- **high pixel granularity and full fill factor**
- **Can be implemented on an existing monolithic detector design.**



Proof of concept tested at University of Geneva

Boost of $Power \cdot \sigma_t$ product demonstrated



Future Circular Collider

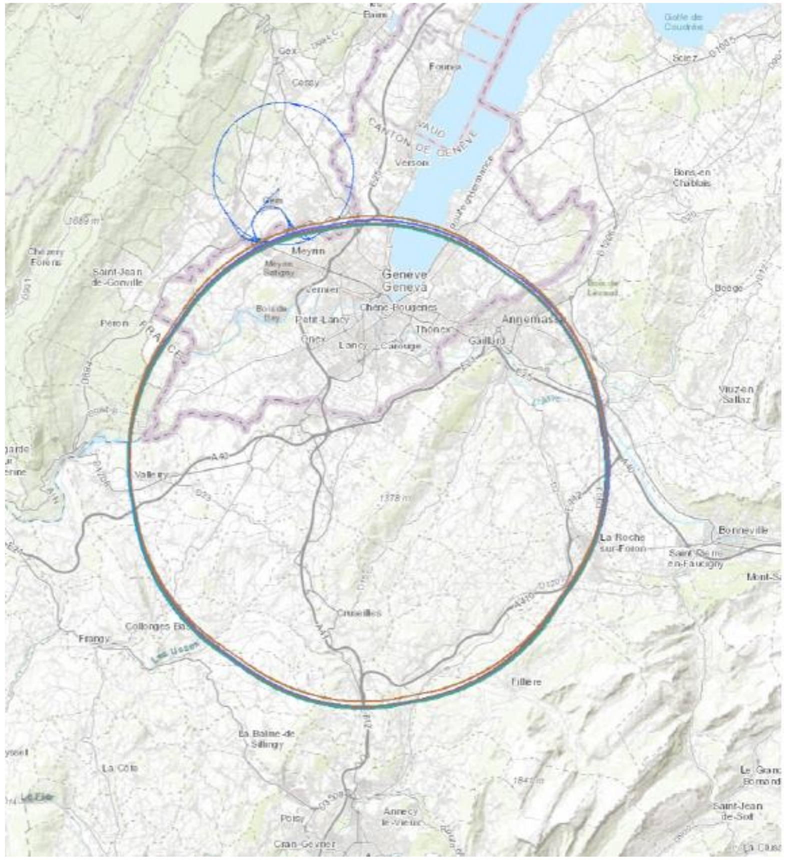
http://cern.ch/fcc

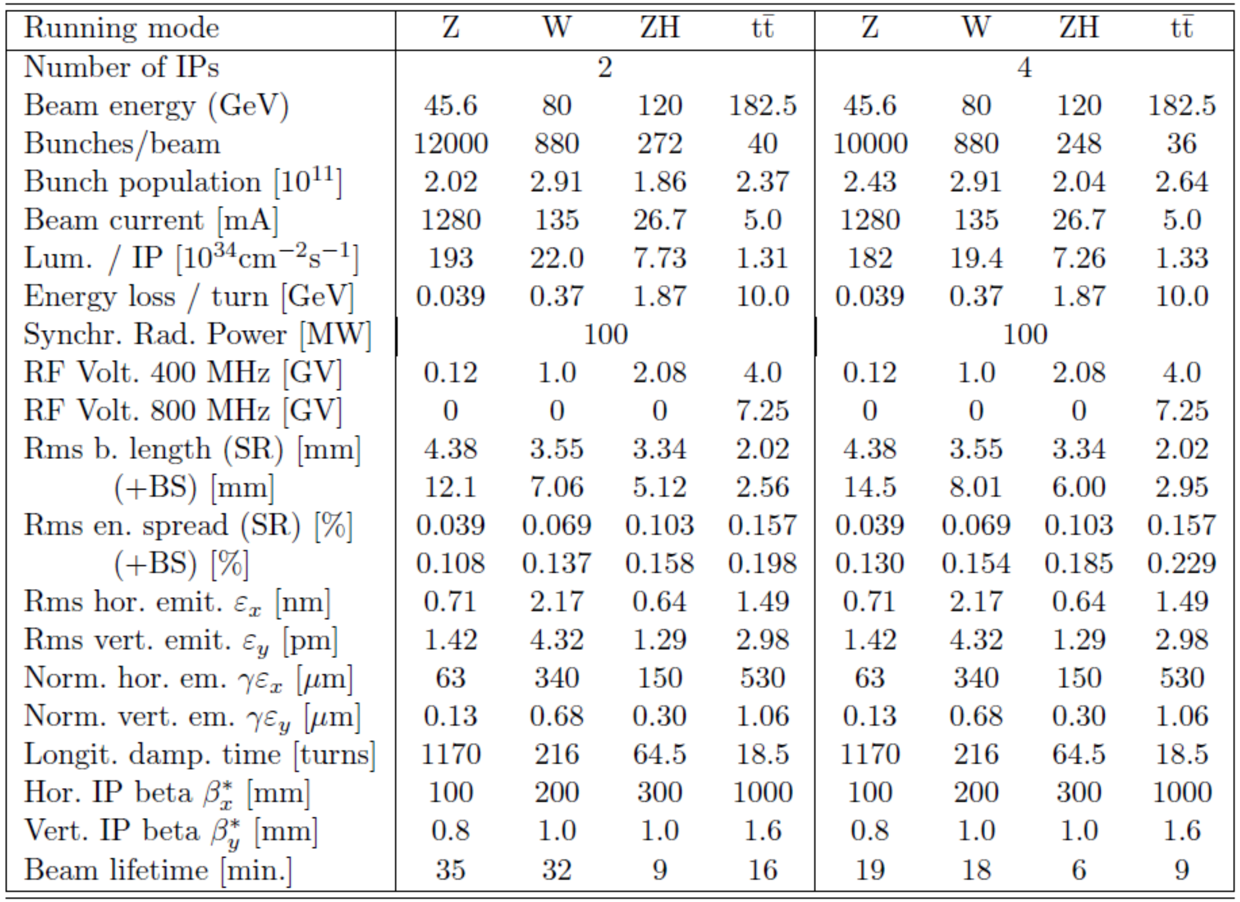
*Work supported by the **European Commission** under the **HORIZON 2020 projects EuroCirCol**, grant agreement 654305; **EASITrain,** grant agreement no. 764879; **ARIES**, grant agreement 730871; and **E-JADE,** contract no. 64547*

photo: J. Wenninger

Future Circular Lepton Collider FCC-ee: Overview and Status

I. Agapov[1], M. Benedikt[2], A. Blondel[3], M. Boscolo[4], O. Brunner[2],
M. Chamizo Llatas[5], T. Charles[6], D. Denisov[5], W. Fischer[5],
E. Gianfelice-Wendt[7], J. Gutleber[2], P. Janot[2], M. Koratzinos[8], R. Losito[2],
S. Nagaitsev[7,9], K. Oide[2,10], T. Raubenheimer[11], R. Rimmer[12], J. Seeman[11],
D. Shatilov[2], V. Shiltsev[7], M. Sullivan[11], U. Wienands[13], F. Zimmermann[2]





Running mode	Z	W	ZH	$t\bar{t}$	Z	W	ZH	$t\bar{t}$
Number of IPs	2				4			
Beam energy (GeV)	45.6	80	120	182.5	45.6	80	120	182.5
Bunches/beam	12000	880	272	40	10000	880	248	36
Bunch population [10^{11}]	2.02	2.91	1.86	2.37	2.43	2.91	2.04	2.64
Beam current [mA]	1280	135	26.7	5.0	1280	135	26.7	5.0
Lum. / IP [$10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$]	193	22.0	7.73	1.31	182	19.4	7.26	1.33
Energy loss / turn [GeV]	0.039	0.37	1.87	10.0	0.039	0.37	1.87	10.0
Synchr. Rad. Power [MW]	100				100			
RF Volt. 400 MHz [GV]	0.12	1.0	2.08	4.0	0.12	1.0	2.08	4.0
RF Volt. 800 MHz [GV]	0	0	0	7.25	0	0	0	7.25
Rms b. length (SR) [mm]	4.38	3.55	3.34	2.02	4.38	3.55	3.34	2.02
(+BS) [mm]	12.1	7.06	5.12	2.56	14.5	8.01	6.00	2.95
Rms en. spread (SR) [%]	0.039	0.069	0.103	0.157	0.039	0.069	0.103	0.157
(+BS) [%]	0.108	0.137	0.158	0.198	0.130	0.154	0.185	0.229
Rms hor. emit. ε_x [nm]	0.71	2.17	0.64	1.49	0.71	2.17	0.64	1.49
Rms vert. emit. ε_y [pm]	1.42	4.32	1.29	2.98	1.42	4.32	1.29	2.98
Norm. hor. em. $\gamma\varepsilon_x$ [μm]	63	340	150	530	63	340	150	530
Norm. vert. em. $\gamma\varepsilon_y$ [μm]	0.13	0.68	0.30	1.06	0.13	0.68	0.30	1.06
Longit. damp. time [turns]	1170	216	64.5	18.5	1170	216	64.5	18.5
Hor. IP beta β_x^* [mm]	100	200	300	1000	100	200	300	1000
Vert. IP beta β_y^* [mm]	0.8	1.0	1.0	1.6	0.8	1.0	1.0	1.6
Beam lifetime [min.]	35	32	9	16	19	18	6	9

Hadron Collider Parameters

	LHC / HL-LHC	HE-LHC (tentative)	FCC-hh Initial	FCC-hh Ultimate
Cms energy [TeV]	14	27	100	100
Luminosity [$10^{34}cm^{-2}s^{-1}$]	1 / 5	28	5	20-30
Machine circumference	27	27	97.75	97.75
Arc dipole field [T]	8	16	16	16
Bunch charge	1.15 / 2.2	2.2	1	1
Bunch distance [ns]	25	25	25	25
Background events/bx	27 / 135	800	170	<1020
Bunch length [cm]	7.5	7.5	8	8

D. Schulte

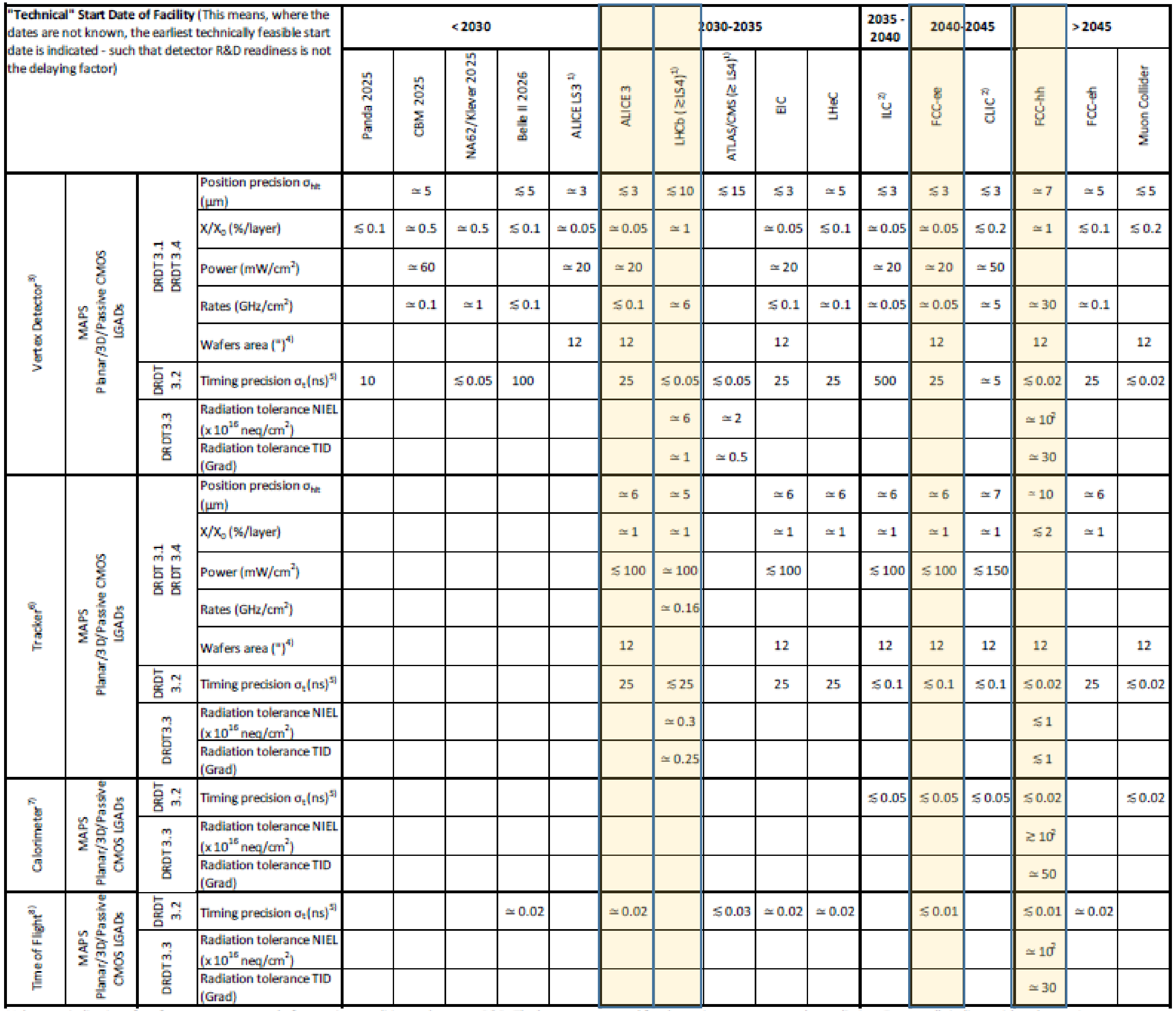
FCC-hh, CERN, March 2019

Target survival 1×10^{17} n_{eq}/cm^2/Y

Sensor requirements for Future Accelerators

Not necessarily all at the same time!

Requirement	Value	
Position resolution (µm)	< 3	
Power dissipation ($\mathrm{mW\ cm^{-2}}$)	20	
Hit rate (GHz)	5/30	750kHz/pixel ($50\mu m^2$)
Timing resolution (ps)	10	
Radiation tolerance ($n_{eq}\ cm^{-2}/Y$)	10^{17}	
Low mass ($\%X_0$)	5	



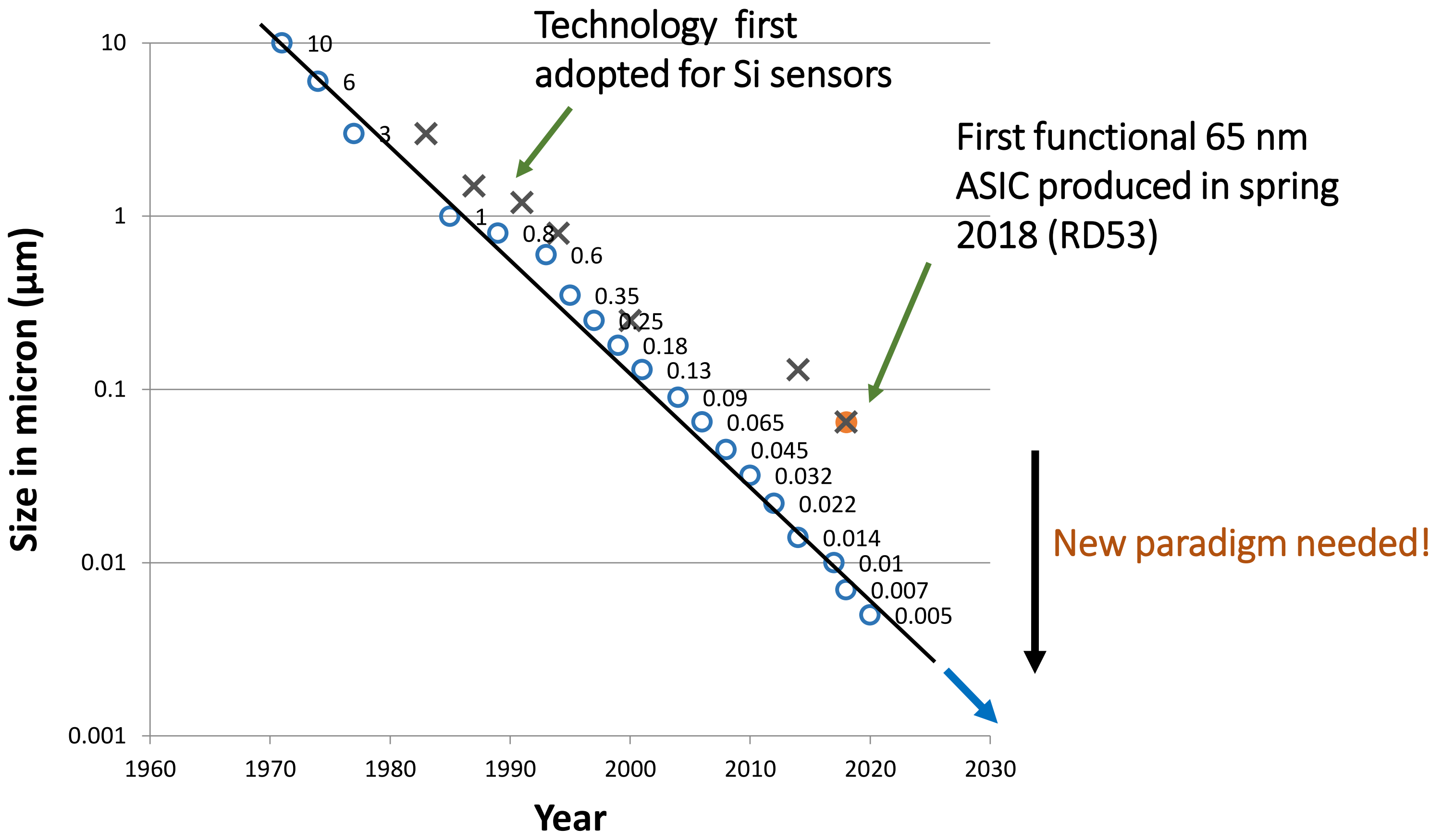
"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				< 2030					2030-2035					2035 - 2040	2040-2045		> 2045		
				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 1)	ALICE 3	LHCb (≳LS4) 2)	ATLAS/CMS (≳ LS4) 1)	EIC	LHeC	ILC 2)	FCC-ee	CLIC 2)	FCC-hh	FCC-eh	Muon Collider
Vertex Detector 3)	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)		≃ 5		≲ 5	≃ 3	≲ 3	≲ 10	≲ 15	≲ 3	≃ 5	≲ 3	≲ 3	≲ 3	≃ 7	≃ 5	≲ 5
			X/X_0 (%/layer)	≲ 0.1	≃ 0.5	≃ 0.5	≲ 0.1	≃ 0.05	≃ 0.05	≃ 1		≃ 0.05	≲ 0.1	≃ 0.05	≃ 0.05	≲ 0.2	≃ 1	≲ 0.1	≲ 0.2
			Power ($\mathrm{mW/cm^2}$)		≃ 60			≃ 20	≃ 20			≃ 20		≃ 20	≃ 20	≃ 50			
			Rates ($\mathrm{GHz/cm^2}$)		≃ 0.1	≃ 1	≲ 0.1		≲ 0.1	≃ 6		≲ 0.1	≃ 0.1	≃ 0.05	≃ 0.05	≃ 5	≃ 30	≃ 0.1	
			Wafers area (") 4)					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t(ns) 5)	10		≲ 0.05	100		25	≲ 0.05	≲ 0.05	25	25	500	25	≃ 5	≲ 0.02	25	≲ 0.02
		DRDT 3.3	Radiation tolerance NIEL ($\mathrm{x\ 10^{16}\ neq/cm^2}$)							≃ 6	≃ 2						≃ 10^2		
			Radiation tolerance TID (Grad)							≃ 1	≃ 0.5						≃ 30		
Tracker 6)	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (µm)						≃ 6	≃ 5		≃ 6	≃ 6	≃ 6	≃ 6	≃ 7	≃ 10	≃ 6	
			X/X_0 (%/layer)						≃ 1	≃ 1		≃ 1	≃ 1	≃ 1	≃ 1	≃ 1	≲ 2	≃ 1	
			Power ($\mathrm{mW/cm^2}$)						≲ 100	≃ 100		≲ 100		≲ 100	≲ 100	≲ 150			
			Rates ($\mathrm{GHz/cm^2}$)							≃ 0.16									
			Wafers area (") 4)						12			12		12	12	12	12		12
		DRDT 3.2	Timing precision σ_t(ns) 5)						25	≲ 25		25	25	≲ 0.1	≲ 0.1	≲ 0.1	≲ 0.02	25	≲ 0.02
		DRDT 3.3	Radiation tolerance NIEL ($\mathrm{x\ 10^{16}\ neq/cm^2}$)							≃ 0.3							≲ 1		
			Radiation tolerance TID (Grad)							≃ 0.25							≲ 1		
Calorimeter 7)	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.2	Timing precision σ_t(ns) 5)											≲ 0.05	≲ 0.05	≲ 0.05	≲ 0.02		≲ 0.02
		DRDT 3.3	Radiation tolerance NIEL ($\mathrm{x\ 10^{16}\ neq/cm^2}$)														≳ 10^2		
			Radiation tolerance TID (Grad)														≃ 50		
Time of Flight 8)	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.2	Timing precision σ_t(ns) 5)				≃ 0.02		≃ 0.02		≲ 0.03	≃ 0.02	≃ 0.02		≲ 0.01		≲ 0.01	≃ 0.02	
		DRDT 3.3	Radiation tolerance NIEL ($\mathrm{x\ 10^{16}\ neq/cm^2}$)														≃ 10^2		
			Radiation tolerance TID (Grad)														≃ 30		

The 2021 ECFA detector research and development roadmap, https://cds.cern.ch/record/2784893.

Moore’s law and sensor evolution.

○ Reduction of the transistor channel length (feature size, S) over the years.

✕ Feature size exploited for mixed signal pixel devices for particle detection.



Technology first adopted for Si sensors

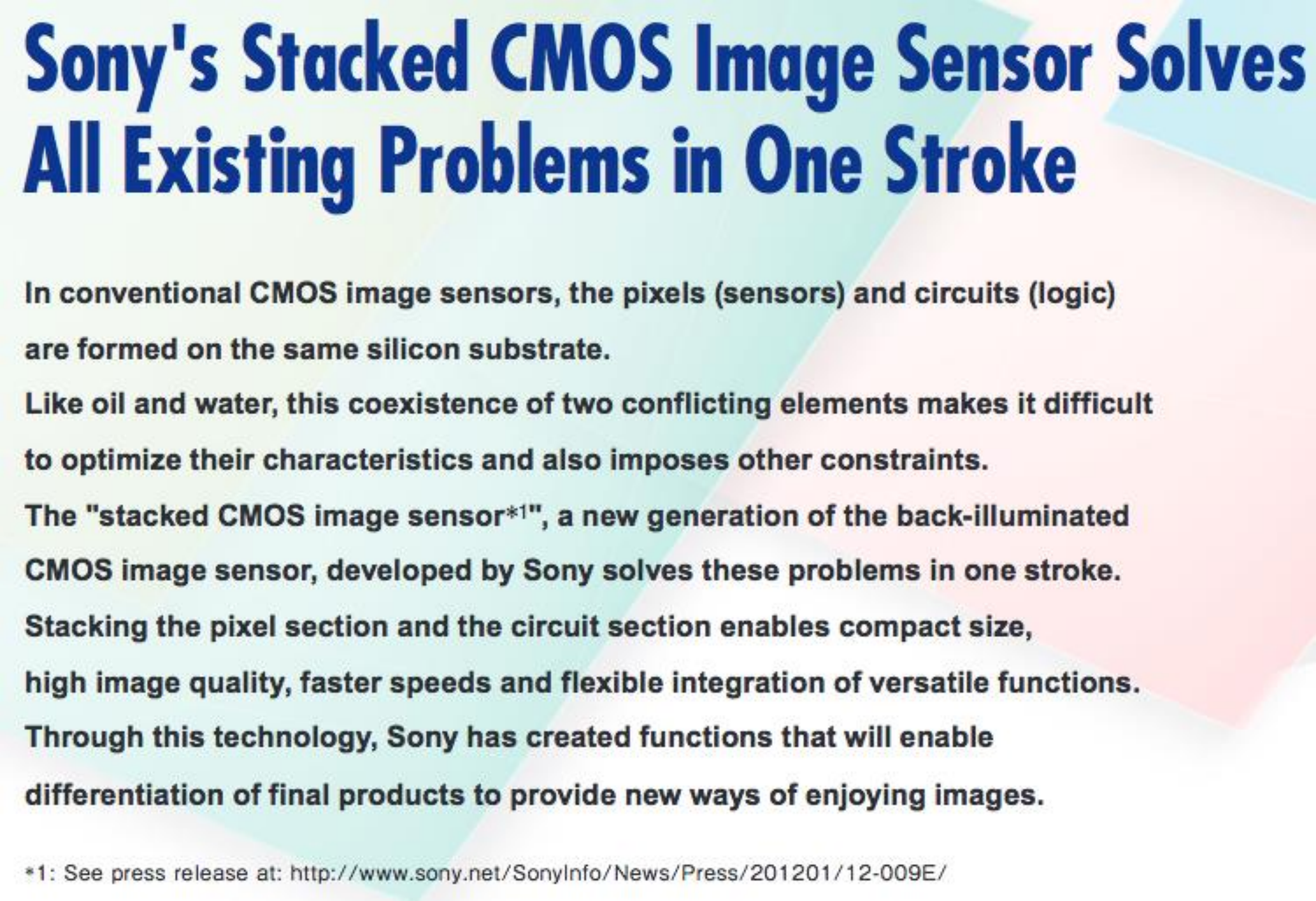
First functional 65 nm ASIC produced in spring 2018 (RD53)

New paradigm needed!

End of technological trajectory for mixed signal devices is now.
There is little gain in going beyond the 65 nm process.

DESiRES proposal: particle detection in a fully digital device

How does see it industry?



Sony's Stacked CMOS Image Sensor Solves All Existing Problems in One Stroke

In conventional CMOS image sensors, the pixels (sensors) and circuits (logic) are formed on the same silicon substrate.

Like oil and water, this coexistence of two conflicting elements makes it difficult to optimize their characteristics and also imposes other constraints.

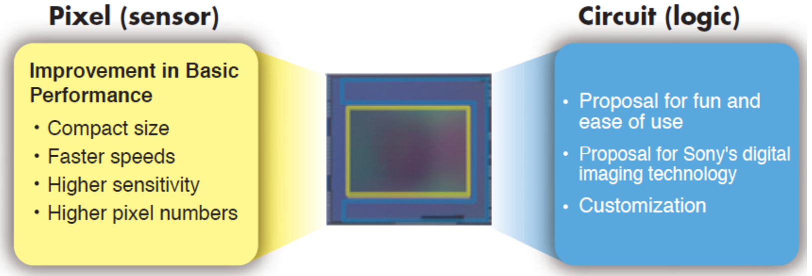
The "stacked CMOS image sensor*1", a new generation of the back-illuminated CMOS image sensor, developed by Sony solves these problems in one stroke.

Stacking the pixel section and the circuit section enables compact size, high image quality, faster speeds and flexible integration of versatile functions.

Through this technology, Sony has created functions that will enable differentiation of final products to provide new ways of enjoying images.

*1: See press release at: http://www.sony.net/SonyInfo/News/Press/201201/12-009E/

■ **Figure 1** **Demands by Customers that Use Image Sensors in Final Products**



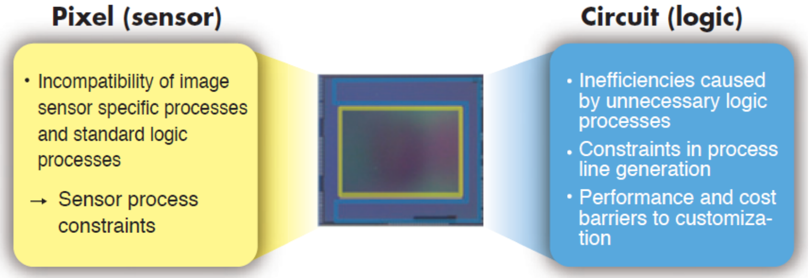
Pixel (sensor)

Improvement in Basic Performance
- Compact size
- Faster speeds
- Higher sensitivity
- Higher pixel numbers

Circuit (logic)

- Proposal for fun and ease of use
- Proposal for Sony's digital imaging technology
- Customization

■ **Figure 2** **Sony's Objectives as an Image Sensor Supplier**



Pixel (sensor)

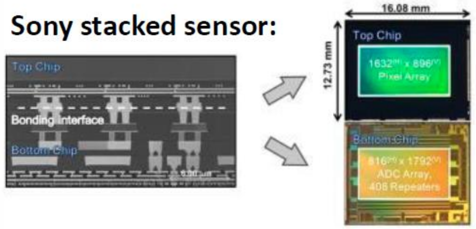
- Incompatibility of image sensor specific processes and standard logic processes

→ Sensor process constraints

Circuit (logic)

- Inefficiencies caused by unnecessary logic processes
- Constraints in process line generation
- Performance and cost barriers to customization

Sony stacked sensor:



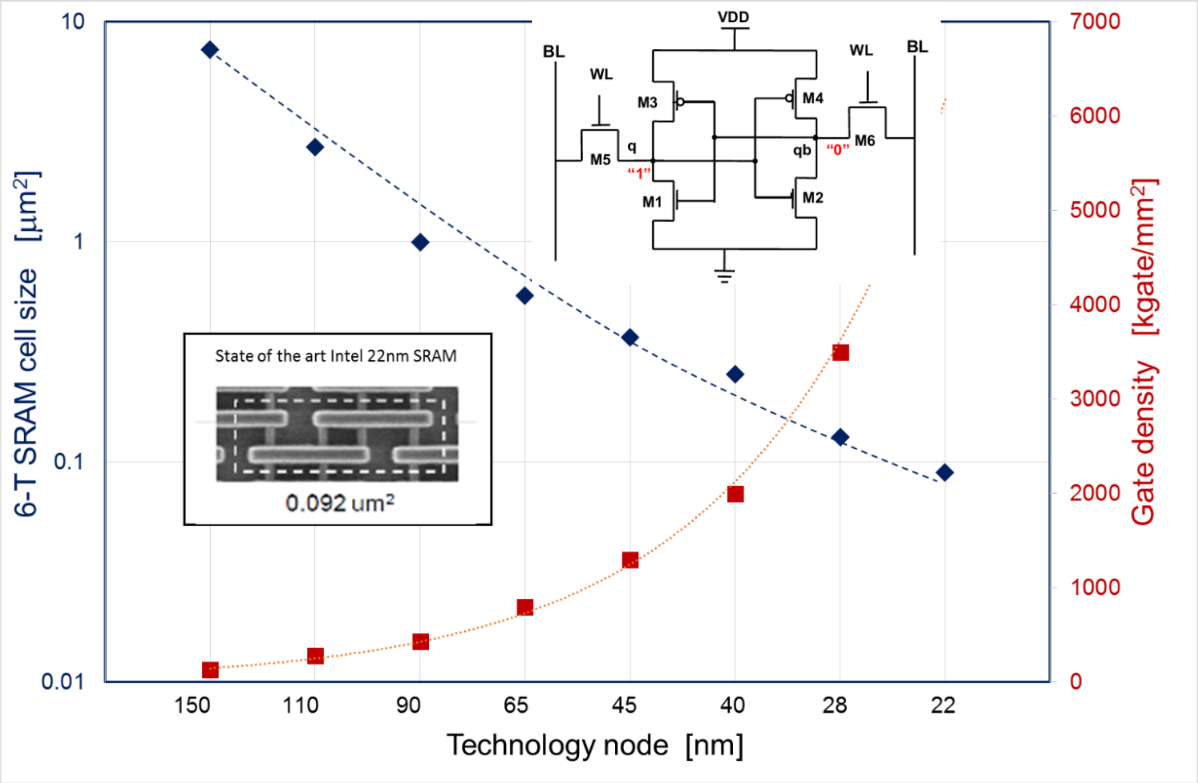
Pixel pitch: 1.22x1.22 μm^2
Bonding pitch: 6.3x6.3 μm

http://www.sony.net/Products/SC-HP/cx_news/vol68/pdf/sideview_vol68.pdf#page=1

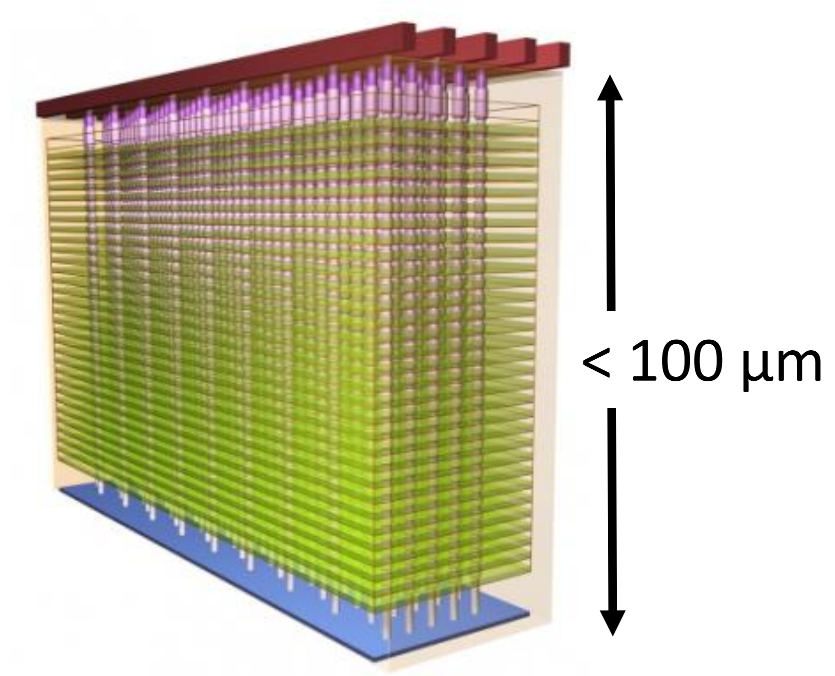
Towards a fully digital particle sensor: memory cells

Very small, fully digital circuits that scale with feature size, S.

Example: size of a 6-transistor memory cell.



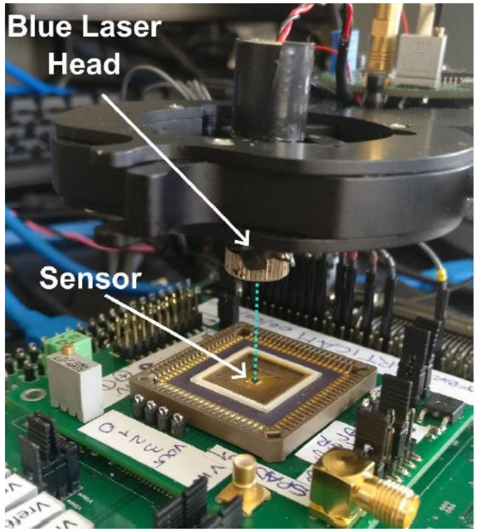
Memory cell layers can be stacked for high density per area.

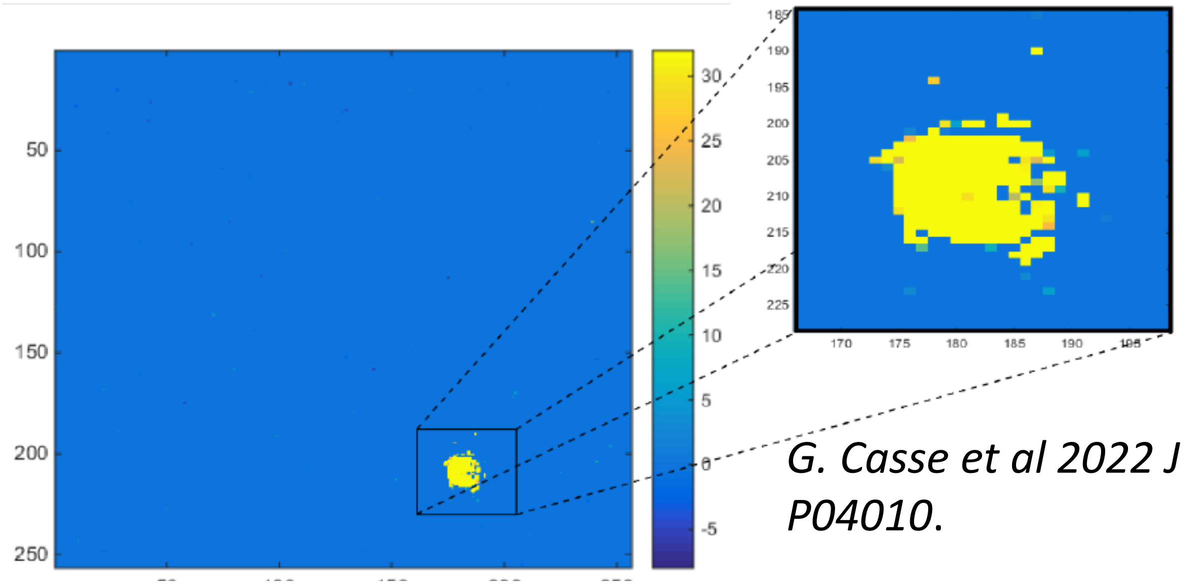


Schematic of a stacked memory chip, with vertical through silicon metal or doped poly-Si interconnections.

Issue in small size memory cells: Single or Multiple Event Upsets. Ionising particles are a known cause of such bit-flips!

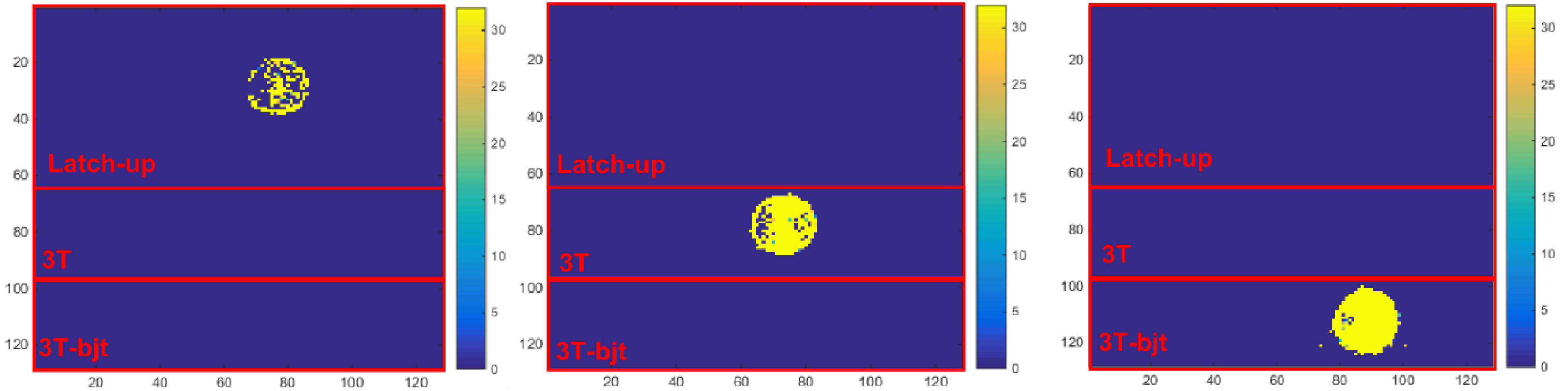
Results: pulsed laser (410 nm) injection in Digital Detectors



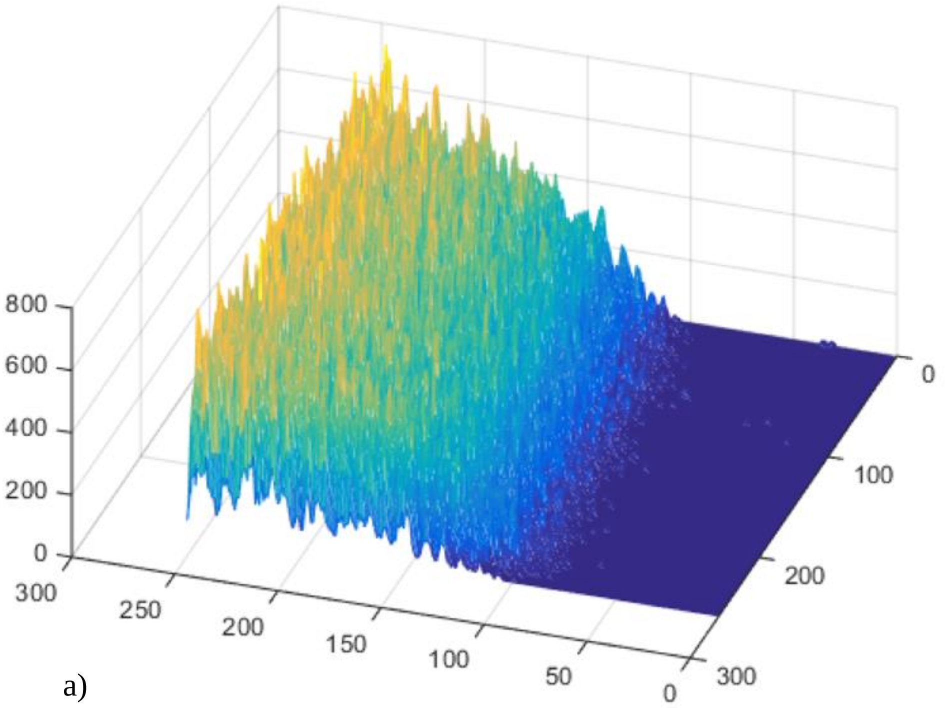


G. Casse et al 2022 JINST 17 P04010.

Response to laser with 10 pulses for each integration time (>DV ~ 100mV).

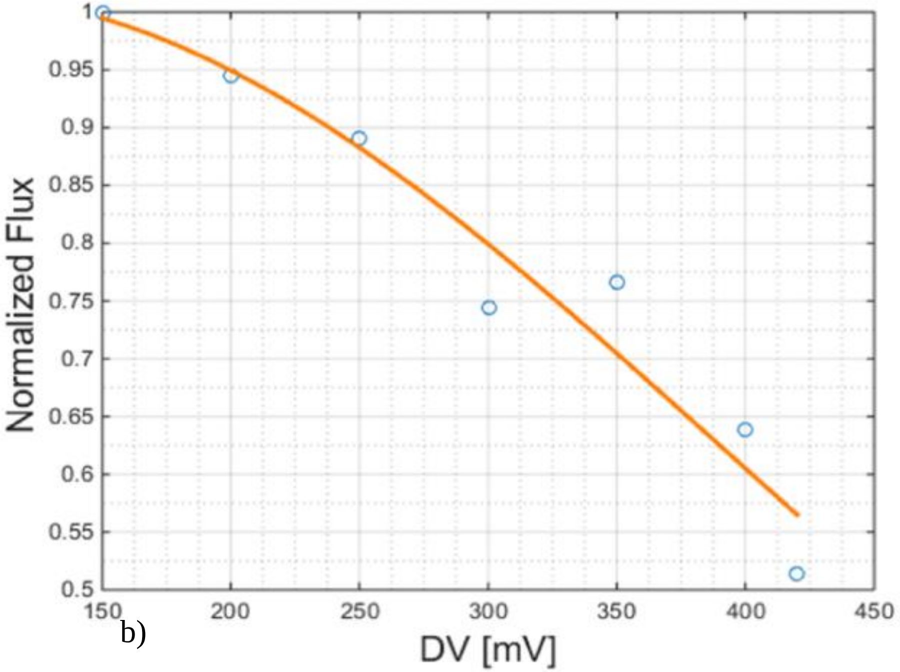


Results: alpha particles (^{241}Am) injection



a)

Lemu response to alpha particles: A metallic shield is interposed between the source and the detector in order to cover about half of the surface to the radiation.



b)

Variation of the detected flux of particles as a function of DV.

G. Casse et al 2022 JINST 17 P04010.

Achievements and trends:

- Hybrid sensors with 65nm electronics achieving great radiation tolerance, keep rather high mass, cost and difficult to significantly reduce pixel size. Less favoured for experiments after HL-LHC, until possibly FCC-hh.
- DMAPS impressive improvements for low mass and position resolution. Improvements on radiation tolerance and timing possible and ongoing. Pixel sizes down to about 25x25 μm^2 achieved. Well placed to approach performance needed for future accelerators except FCC-hh.
- The other future option, a reality in industrial CMOS: vertically integrated diode, analogue circuit and digital circuits (possibly more than one layer for readout in extremely high multiplicity and high pixel density environments). Layers with different and optimised technology would take sensor performance significantly forward.
- The radiation environment of FCC-hh still looks prohibitive.