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ATLAS EXPERIMENT

Hybridisation and assembly of LGAD devices for the HGTD ATLAS upgrade

WORKSHOP ON FUTURE ACCELERATORS
CORFU, GREECE 2023

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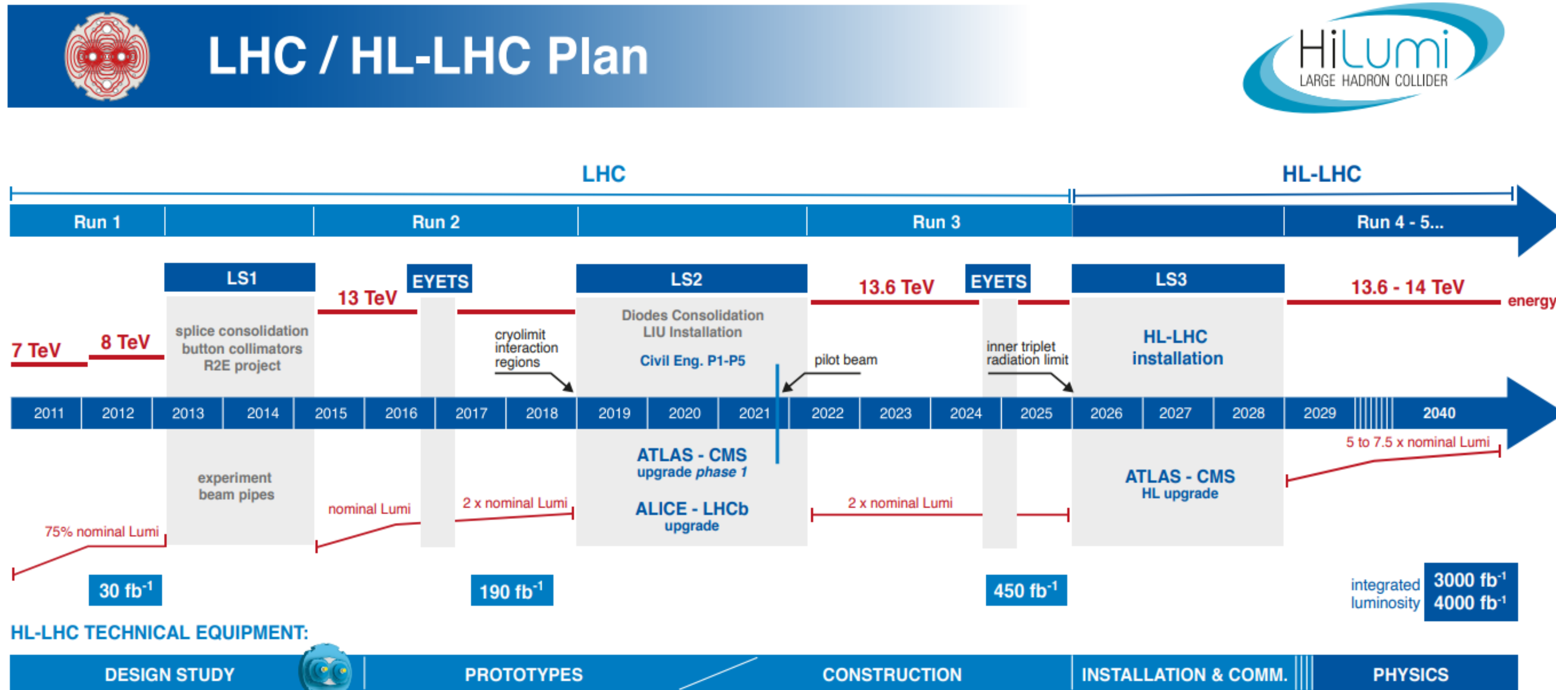
For the ATLAS HGTD group

Introduction

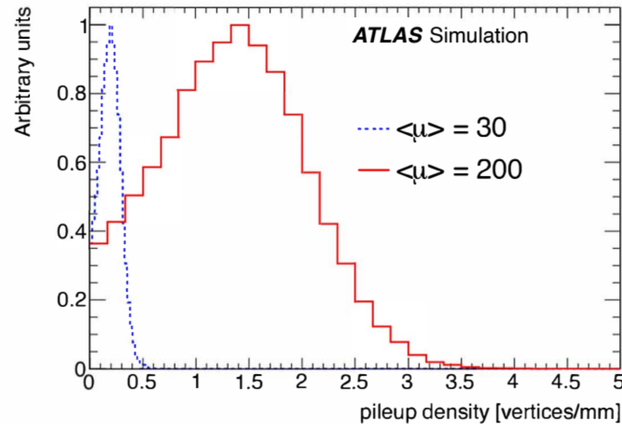


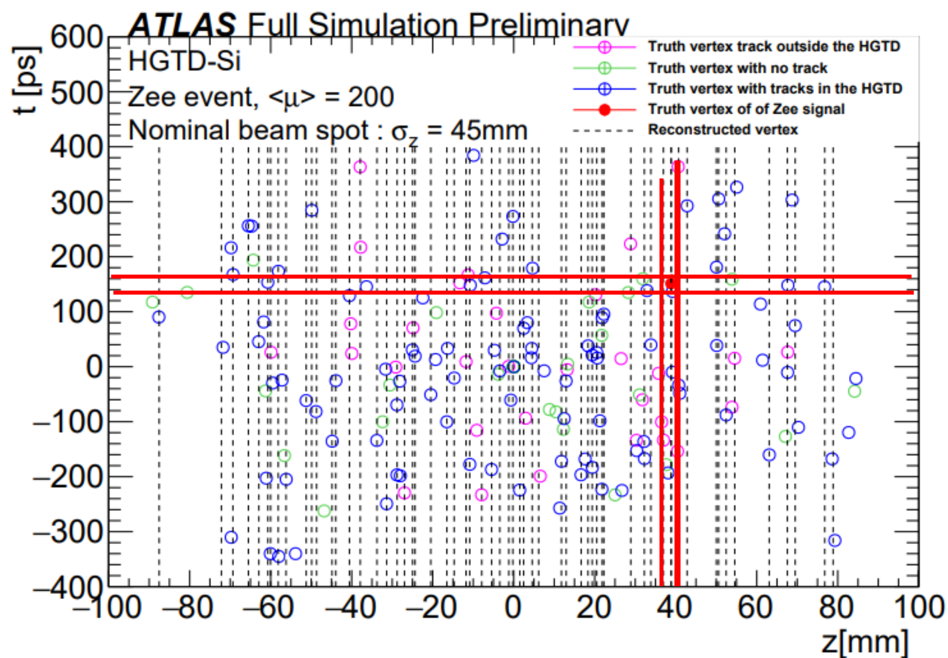
This talk will include:

1. Introduction to HGTD
2. Module hybridisation and assembly process
3. Bump size effect on noise in early module prototypes
4. Studies with full size modules
5. Studies with full HGTD modules
6. First thermal studies

- LHC upgrade to HL-LHC: Planned to start operating in 2029
- Instantaneous luminosity $7.5 \times 10^{34} \mathrm{cm}^{-2}\, \mathrm{s}^{-1}$ (7 times present luminosity)
- Increase in luminosity results in more pile-up and radiation damage
- ATLAS experiment also needs to be upgraded to meet the new requirements

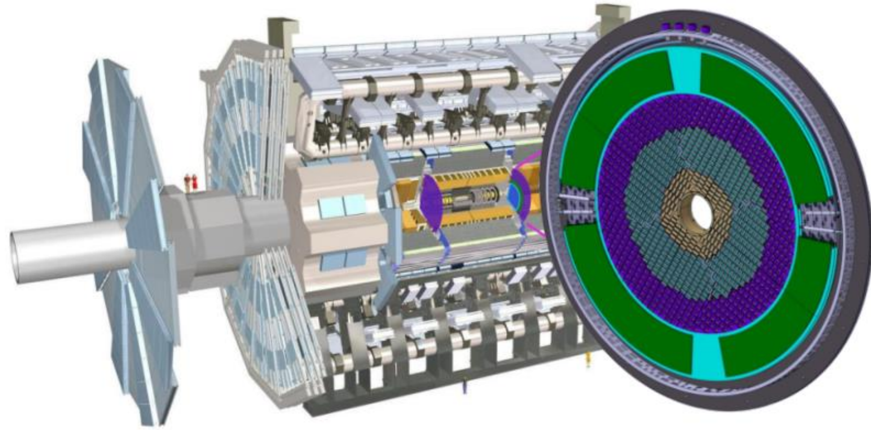
Motivation

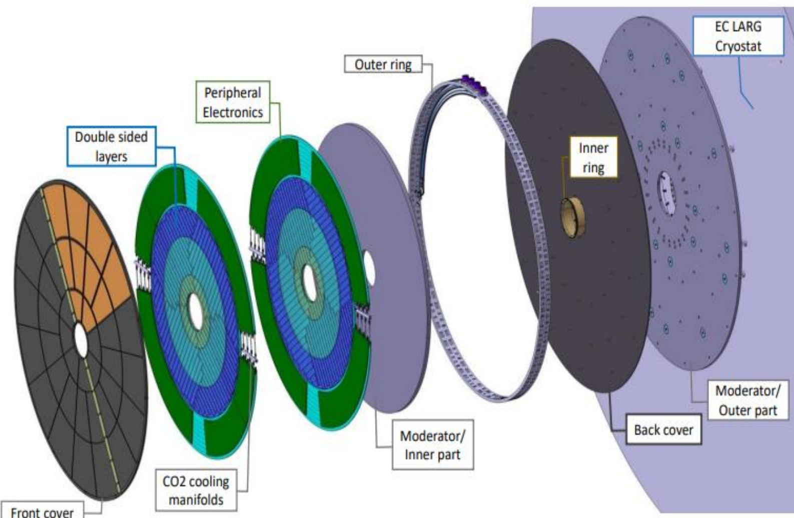




- Pile-up Challenge
  - $< \mu > = 200$ interactions/bunch crossing
  - ~ 1.8 vertices/mm
  - Current conditions (Run 3): < μ > ~ 40 interactions/bunch crossing
- High Granularity Timing Detector (HGTD) proposed in front of the end-cap calorimeter for pile-up mitigation
- Performance improved by combining HGTD timing and Inner-Tracker (Itk) position information
- Blue points in z vs t plot show vertices with tracks in HGTD
- Red point represents the single interaction.
  - There are also other pile-up interaction at almost the same position
  - But, timing information separates them from the primary vertex

High Granularity Timing Detector





- Two disks located in the gap region between the barrel and the end-cap calorimeters
- Distance in z of ~ $\pm 3.5\ \mathrm{m}$ from the nominal interaction point
- 8032 HGTD modules instrumented:
  - Low Gain Avalanche Detectors (LGAD) demonstrated to provide excellent time resolution ($\sim 30\ \mathrm{ps}$ before irradiation).
  - ALTIROC readout chip (more in next slides)

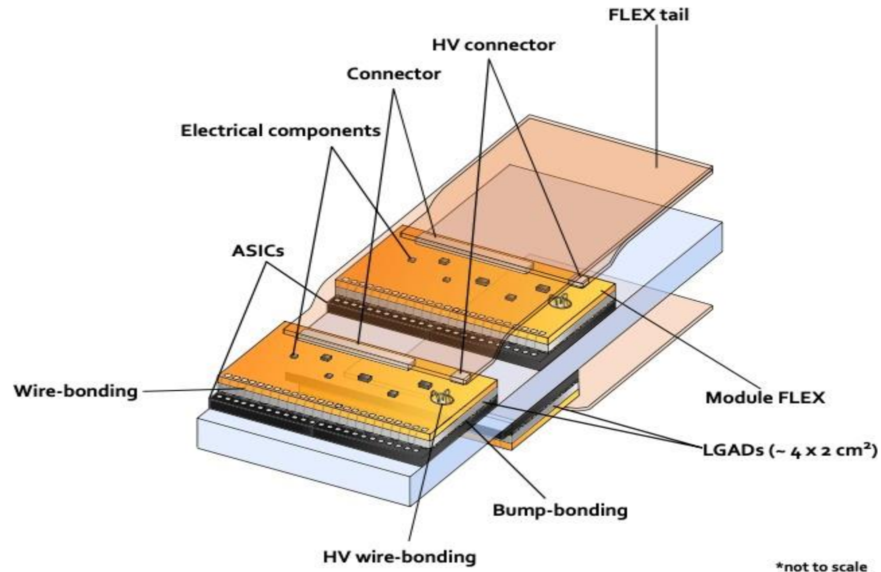
HGTD Requirements :

- Performance
  - Minimum charge of 4 fC
  - Time resolution per track of 30 ps (start) and 50 ps (after 4000 fb^{-1})
- Assembly
  - Bump size of around 80 $\mu\mathrm{m}$
  - Bump shear stress of 40 gf/bump
  - Wire-bond pull force of 5 gf

Module prototypes:

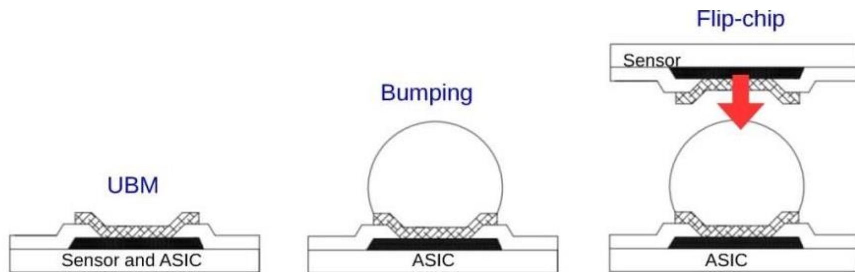
- Early module prototype: 5×5 matrix of LGAD + ALTIROC1
- Full module: 15×15 matrix of LGAD + ALTIROC2
- Full HGTD modules: $2 \times (15 \times 15)$ matrix of LGAD+ ALTIROC2

Module hybridization



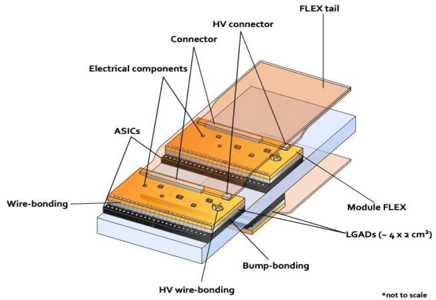
- HGTD hybrid consists of a LGAD sensor $(15 \times 15$ pads) interconnected to the ALTIROC readout chip through bump-bonding
- 2x (15 × 15) pads (4 cm × 2 cm). Pad size: 1.3 mm × 1.3 mm
- A module consists of two hybrids joined by a module flex printed circuit board (PCB)

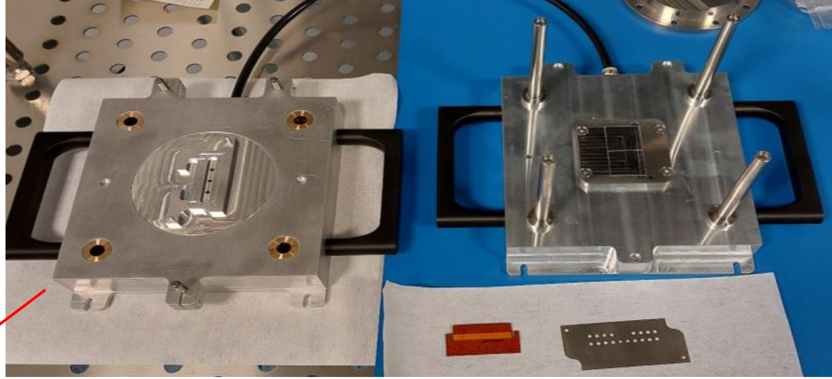
Bump-bond process:



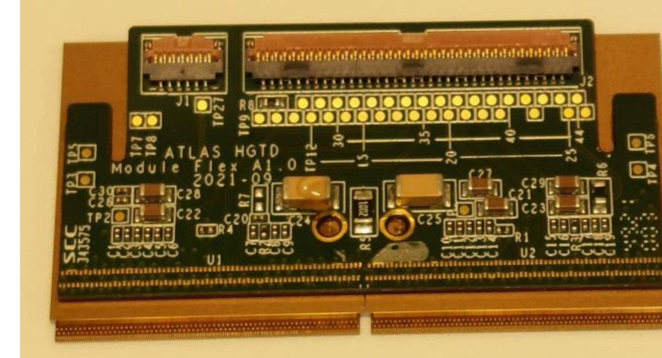
1. Deposition of metal (Ni/Au) on the Al pads (UBM)
2. Solder bump deposition (ball placement)
3. Flip chip to connect ASIC and sensor through alignment and thermal compression cycle
4. First full size prototypes hybridized in China and Spain (bump shear > 40 gf/bump)

Module assembly process



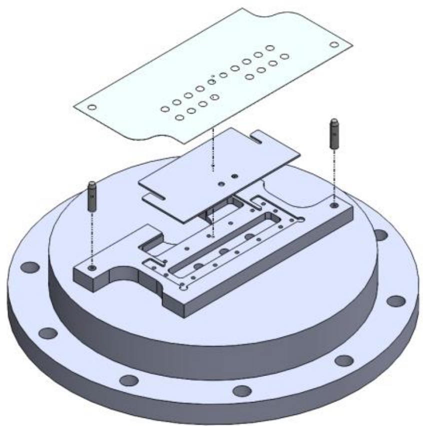


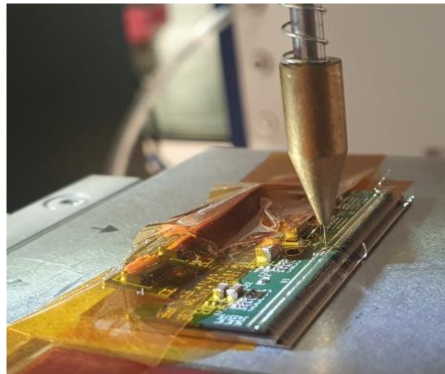
Assembly method: based on custom made Jigs
Glue distribution: Through Stencil



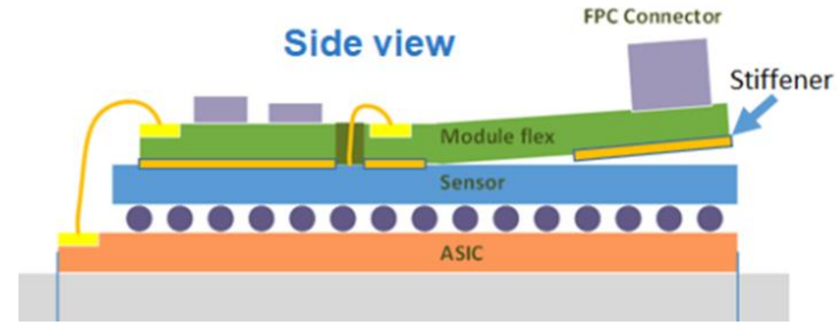
Chip 0 Chip 1

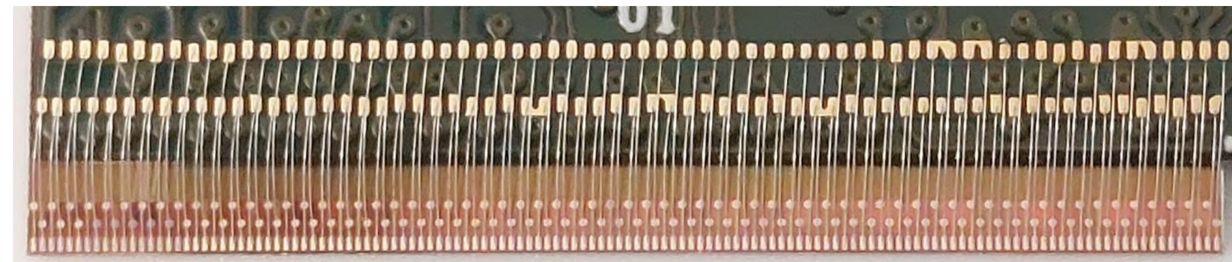
Assembled module : Full HGTD module It consists of two hybrids and a module Flex



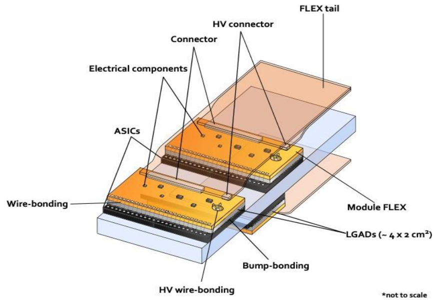


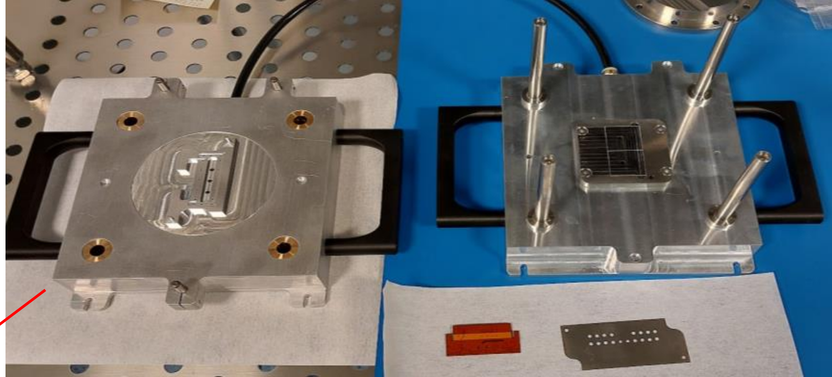
Wire-bonded (wedge to wedge bonding). Pull tests done for quality assurance





Module assembly process





Assembly method: based on custom made Jigs
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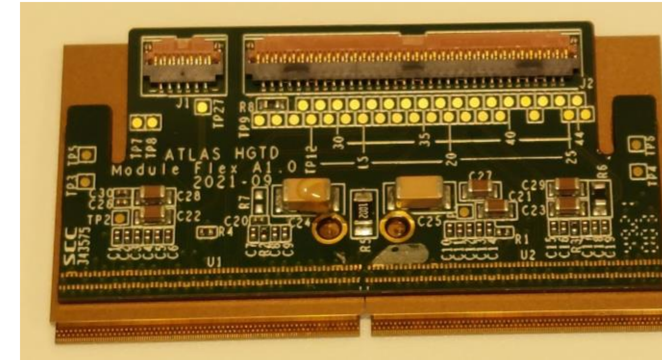
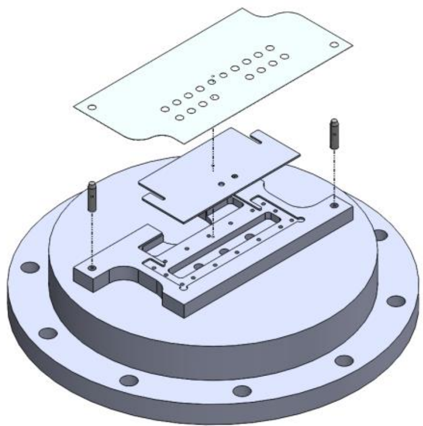
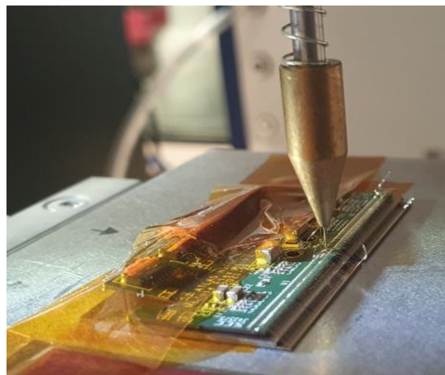


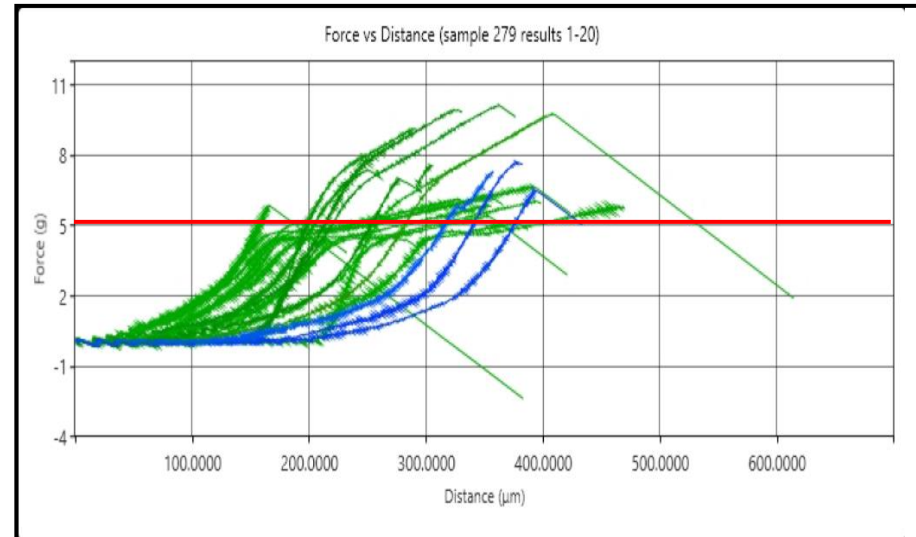
Chip 0 **Chip 1**

Assembled module : Full HGTD module It consists of two hybrids and a module Flex





Wire-bonded (wedge to wedge bonding). Pull tests done for quality assurance

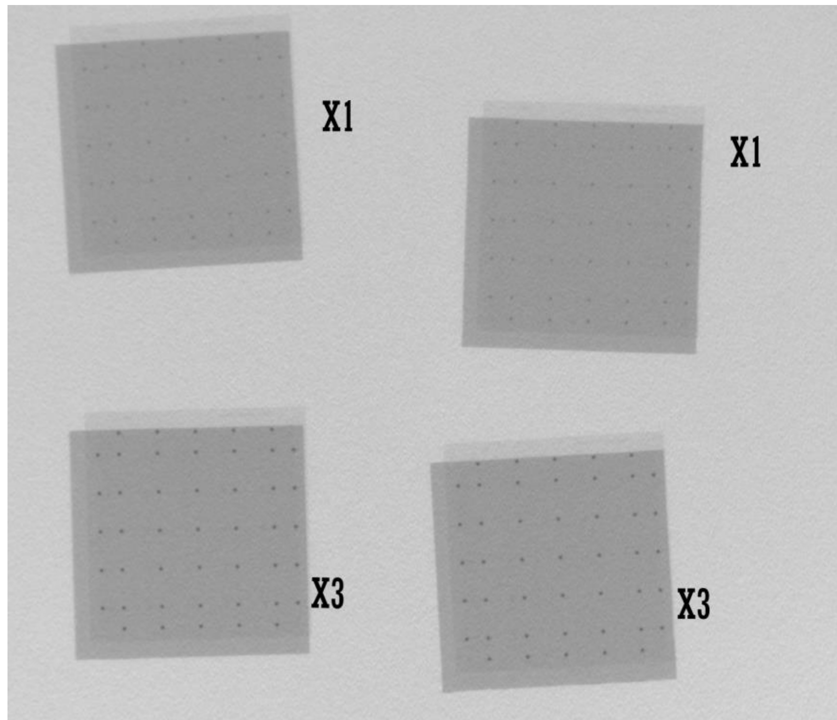


- HGTD requires 5 gf minimum
- All wires satisfy this requirement
- No lift-offs
- Overall, wire bonding tests are OK

Studies to see effect of bump size on ASIC noise

Motivation for this study:

- Connection between the sensor and ASIC is a critical step in HGTD module fabrication
- The timing performance of these devices is critical for the project. It is important to understand the sources of noise in the system
- Bump size can affect the system performance:
  - Different bump sizes can affect the input capacitance seen by the pre-amplifier of ASIC (and so noise)
  - The separation between the chip and the sensor could affect the noise of the device through coupling between the substrates

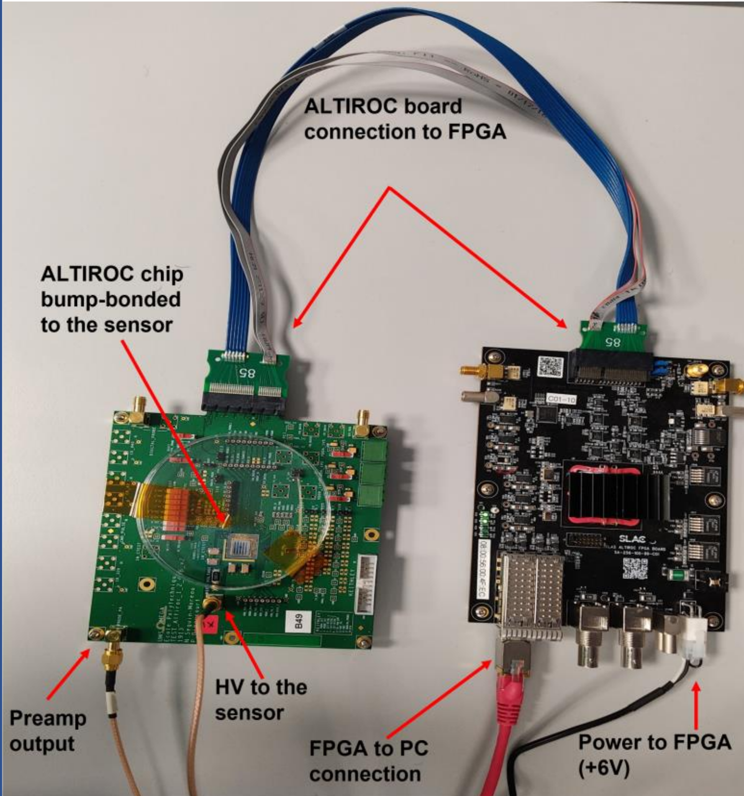


Test Method:

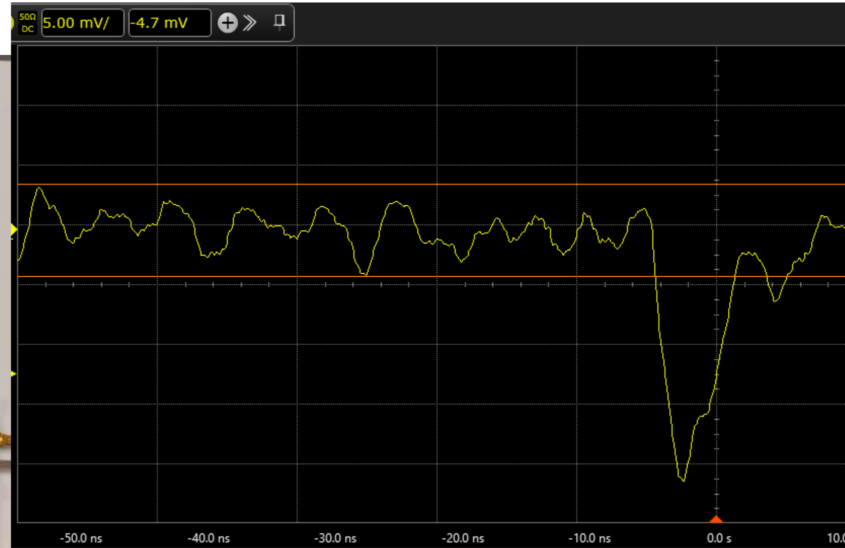
- Bump balls of 80 μm diameter were deposited on two ALTIROC1 ASICs (X1), while 115 μm diameter balls were deposited on another two (X3) (3 times the volume of the 80 μm diameter balls)
- Different bump sizes are significantly clear on X-rays
- Noise measurements using the altiroc-daq software with the charge scan as well as with an oscilloscope

Tests with early module for bump size effect

Setup

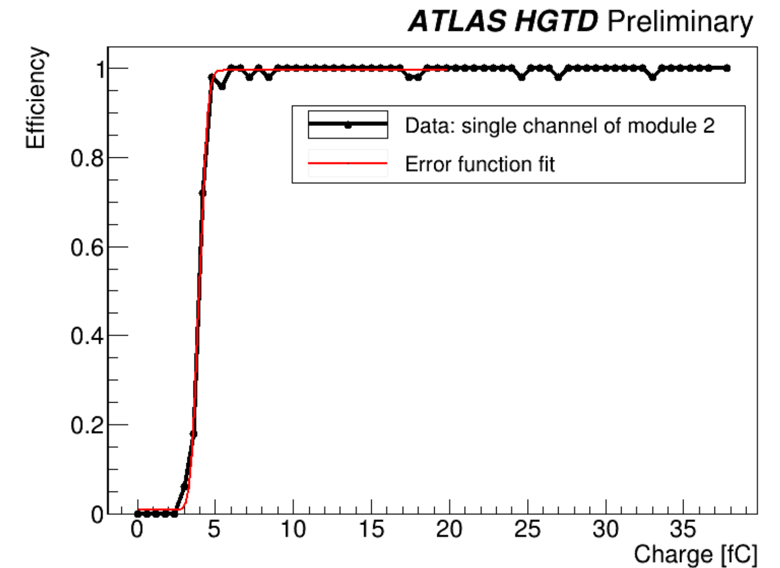


Early module prototype:
5×5 HPK sensor + ALTIROC1



Noise measurements from Oscilloscope:

- First, the preamplifier probe is turned on from the altiroc-daq-software for the pixel to be tested
- Preamp output signal from PCB is then fed to oscilloscope
- R.m.s of the signal within orange lines defined as the noise of the pixel



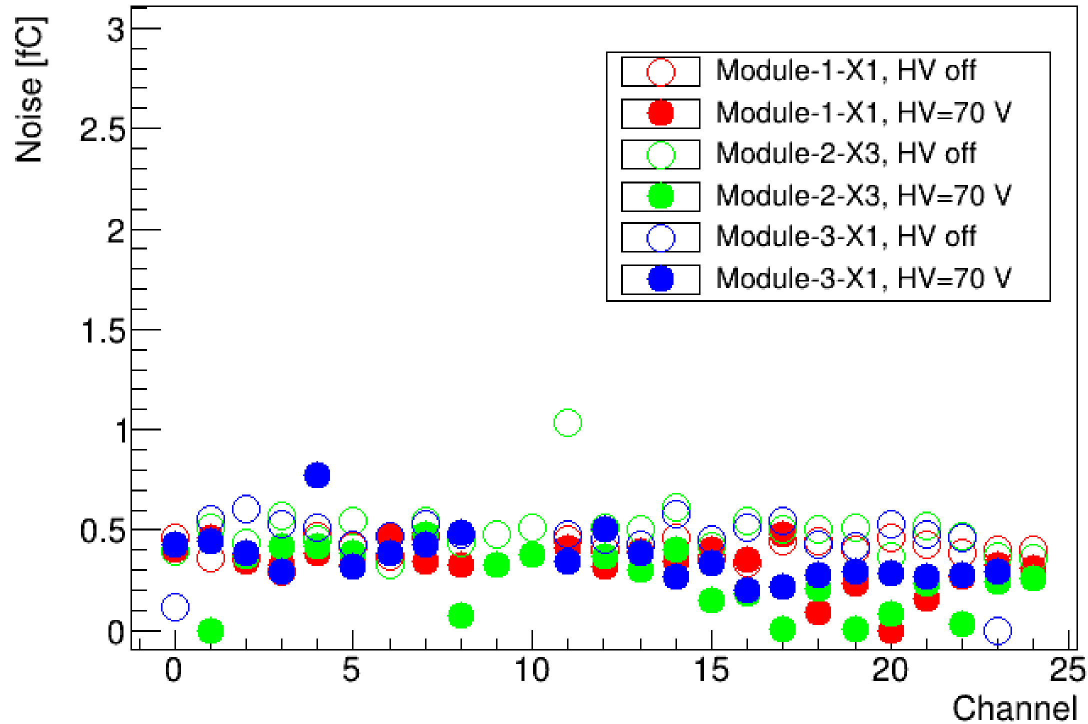
Noise measurements from charge scan:

- Charge vs Efficiency is plotted at particular threshold
- The S-curve obtained from the scan is fitted with an error function:

$$d + \frac{1}{2}\left(c \times \frac{(1 - Erf(x-a))}{\sqrt{2b}}\right)$$

- The parameter a is defined as the threshold and parameter b of the fit is defined as the noise of the pixel

Results: Effect of bump size on noise



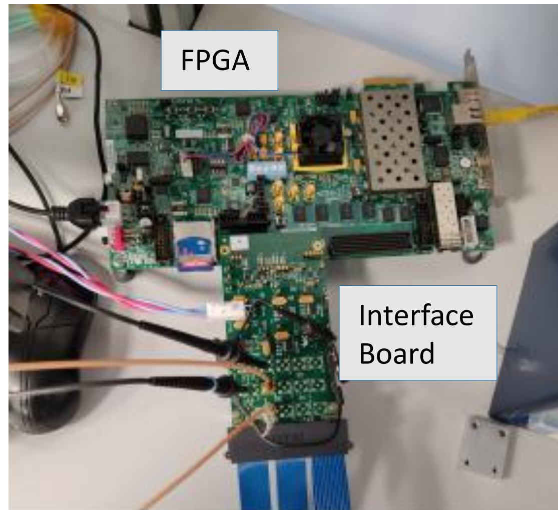
Noise measurements from S-curves

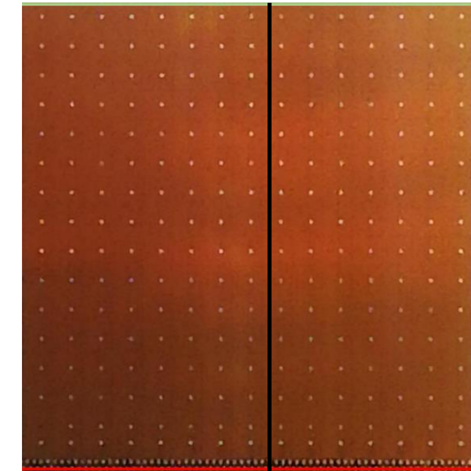
Conclusion:

- No significant affect of the bump size was observed on the noise of the module
- Hybridisation process doesn't effect the noise in the ALTIROC modules
- 80 µm bump size was decided for rest of the assembly process

Measurements on full size hybrids after assembly

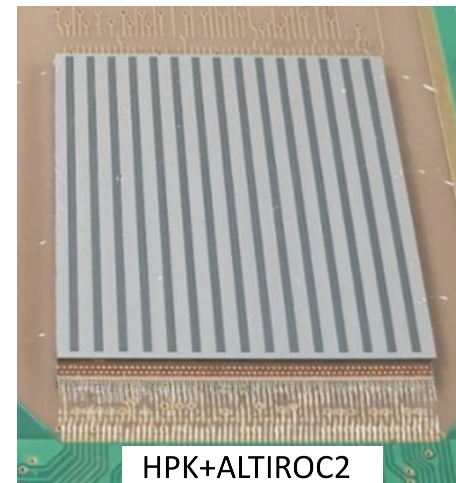
Setup

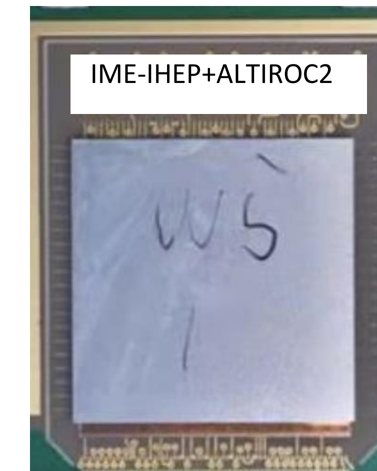




- Full size module contains 15×15 matrix of sensor bump-bonded to the ASIC
- Col 0 to Col 7 consists of VPA (voltage pre-amplifier) and Col 7 to Col 14 consist of TZ (Transimpedance amplifier)

- Firmware and the Software (Alvin) system developed for HGTD.
- The ALTIROC discriminator has been designed to have a threshold of about 2 fC



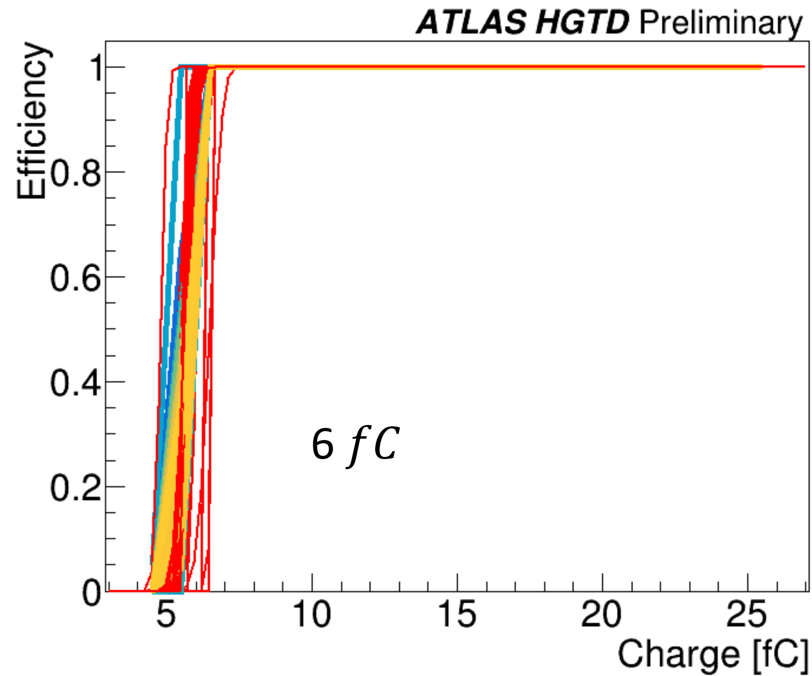


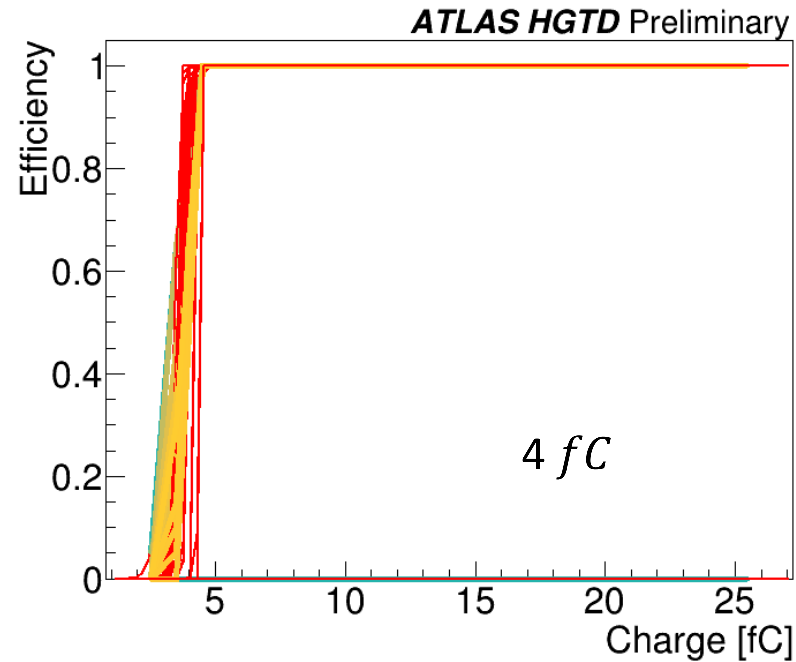
Full size modules produced in Spain (IFAE) and China (NCAP/IHEP)

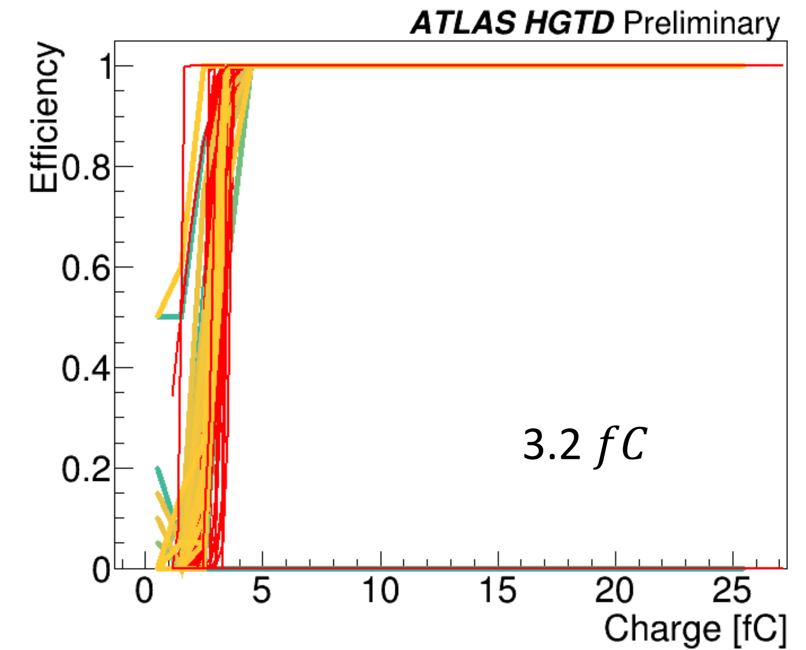
Lowest threshold achievable for full size modules

Measurements Steps:

- First, the configuration of registers are done
- Then the ASIC threshold is set to target. (First global and then in pixel correction)
- Then, a charge scan is performed. The efficiency as a function of charge is obtained and fitted with S-curves. The threshold corresponds to the value at 50% efficiency

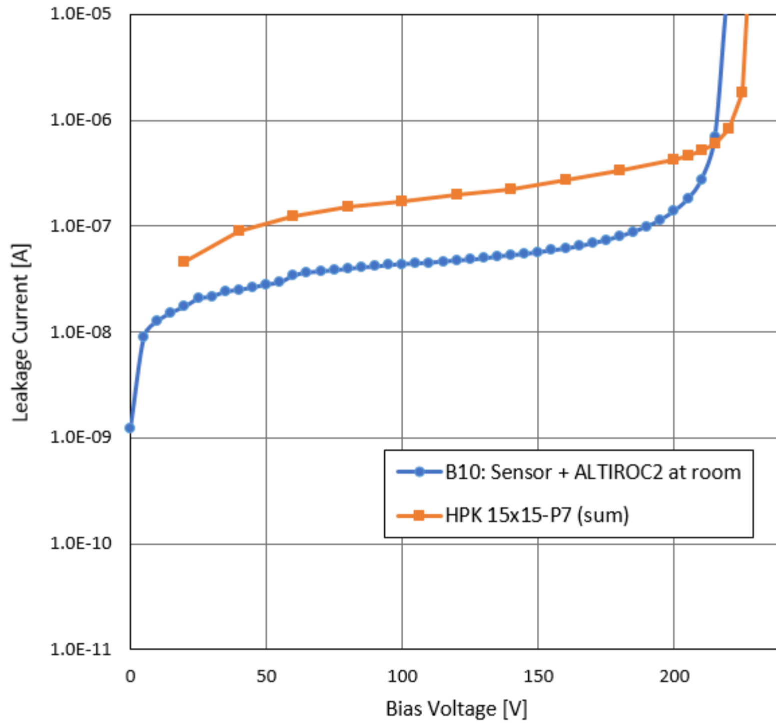




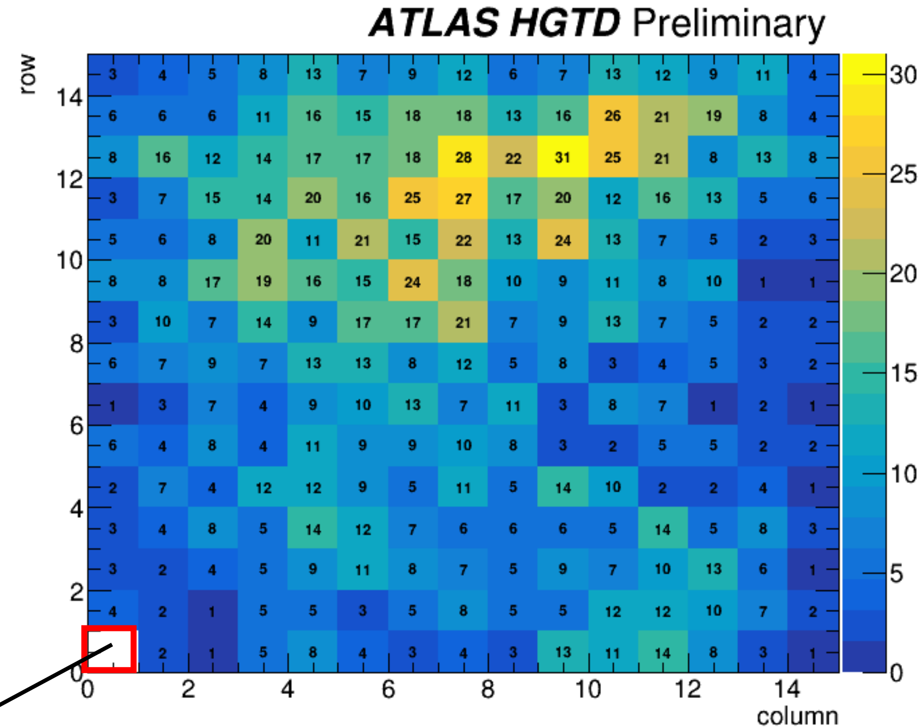


- The module can be tuned till 4 fC without any noise
- The module is well tuned till 3.2 fC with few noisy pixels (No tuning of clock delays implemented)

Bump-bond connectivity verification of full size modules



IV for HPK sensor



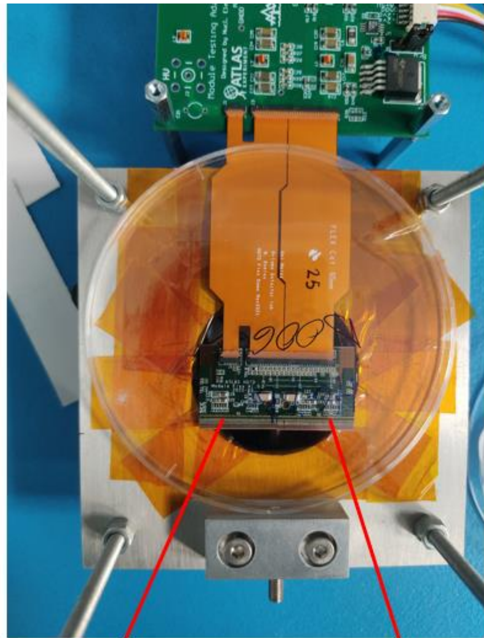
Pixel 0 not bump-bonded for other studies

Occupancy map with Sr-90 source. Sensor biased at = HV 90 V.

Threshold = 8 fC

- Sr-90 source scan shows 100% bump connectivity.
- Similar tests were done on other 8 modules. All of them resulted in 100% bump-bond connectivity!

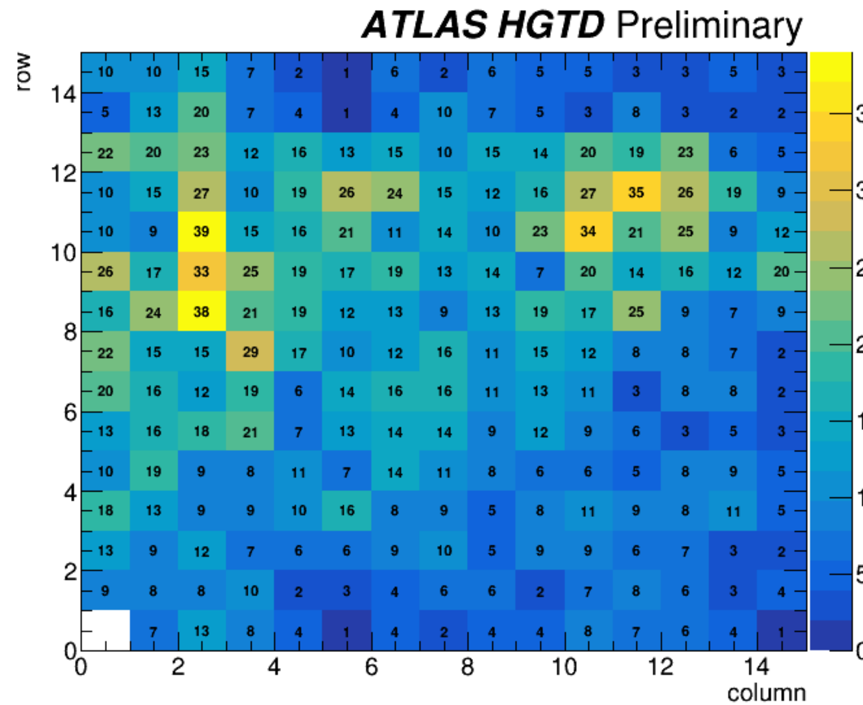
Bump-bond connectivity verification of full HGTD modules at IFAE



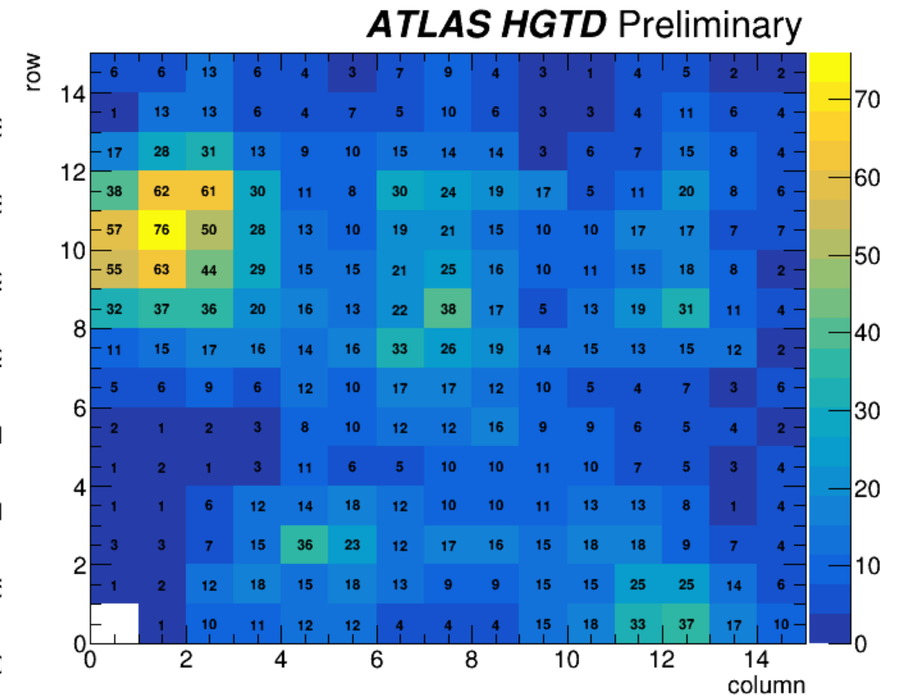
Chip 0 | Chip 1

HV = 150 V

Threshold = 10 fC



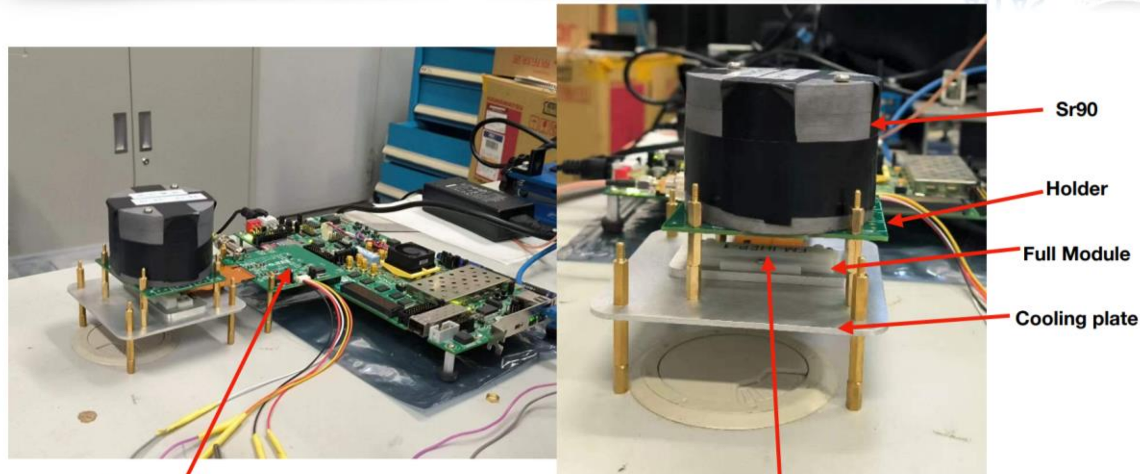
Chip 0



Chip 1

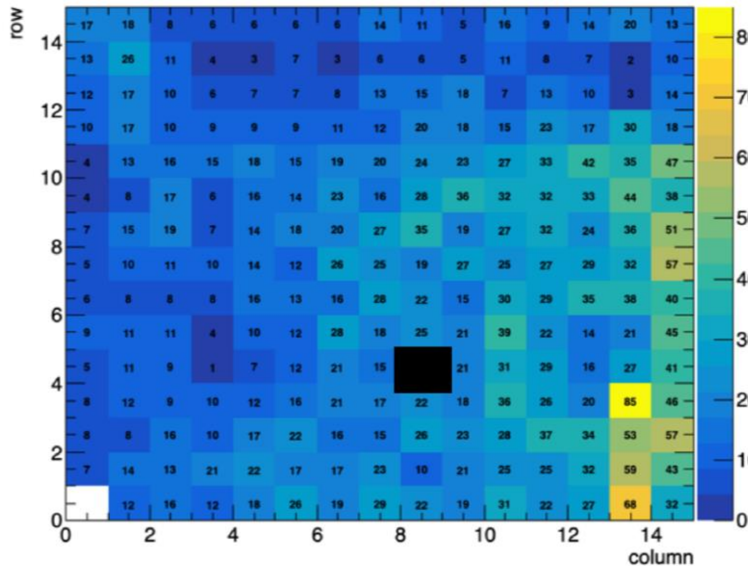
- Full HGTD modules with the flex assembled for demonstrator tests
- Sr-90 source scan shows 100% bump connectivity

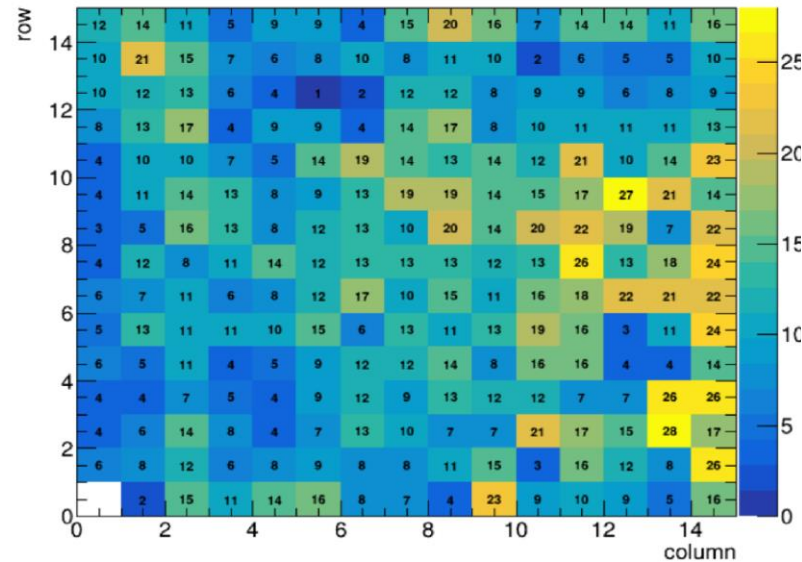
Bump-bond connectivity verification of full HGTD modules at IHEP



HV= 150 V

Threshold = 8 fC



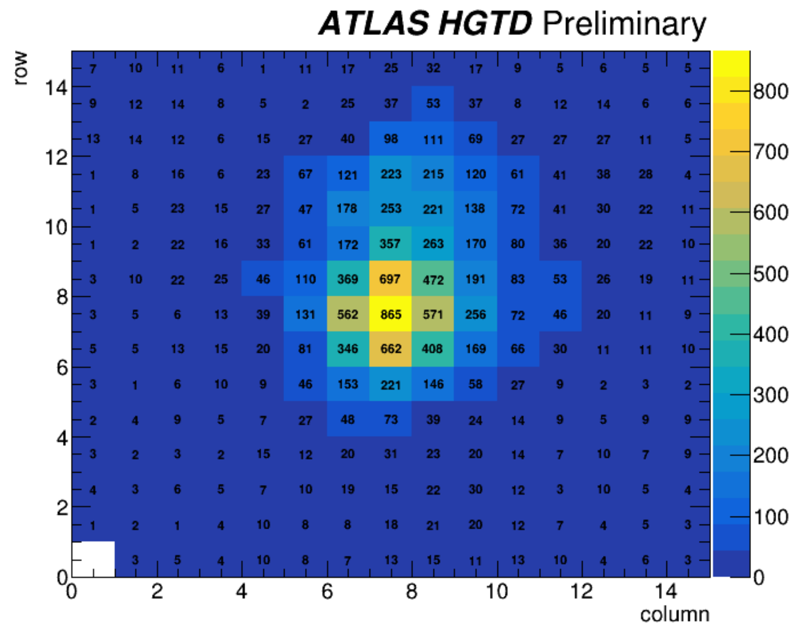


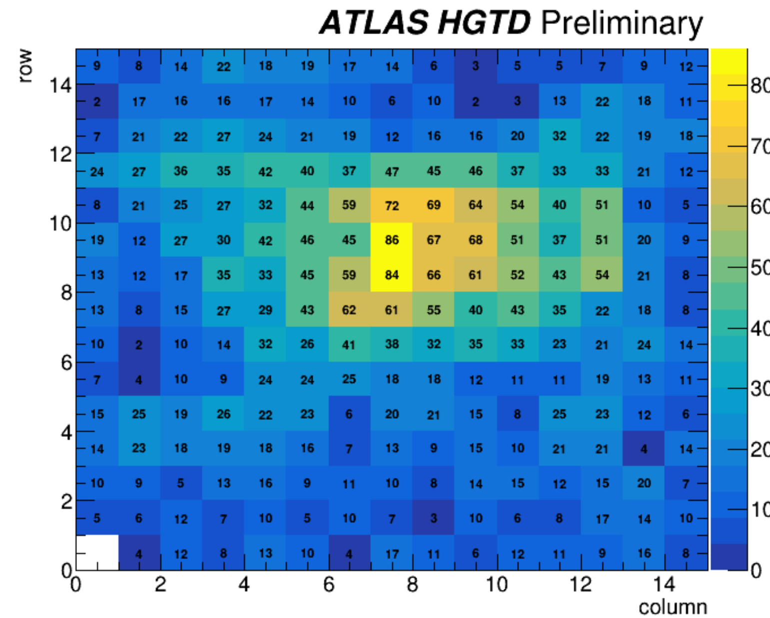
- One masked pixel due to noise issues at lower threshold tuning
- Sr-90 source scan with full modules at IHEP shows 100% bump connectivity
- Tests at both IHEP and IFAE shows 100% bump-bond connectivity in the hybridisation process at both institutes

Thermal stress tests

Motivation for this study:

- The operating temperature for the modules in HGTD is -30°C
- The hermetic vessels which provide a robust support structure to the detector instrumented disks has a safe operational temperature range from -45 °C to 40 °C
- Necessary to verify that modules can sustain thermal cycles (no delamination or bump failures)





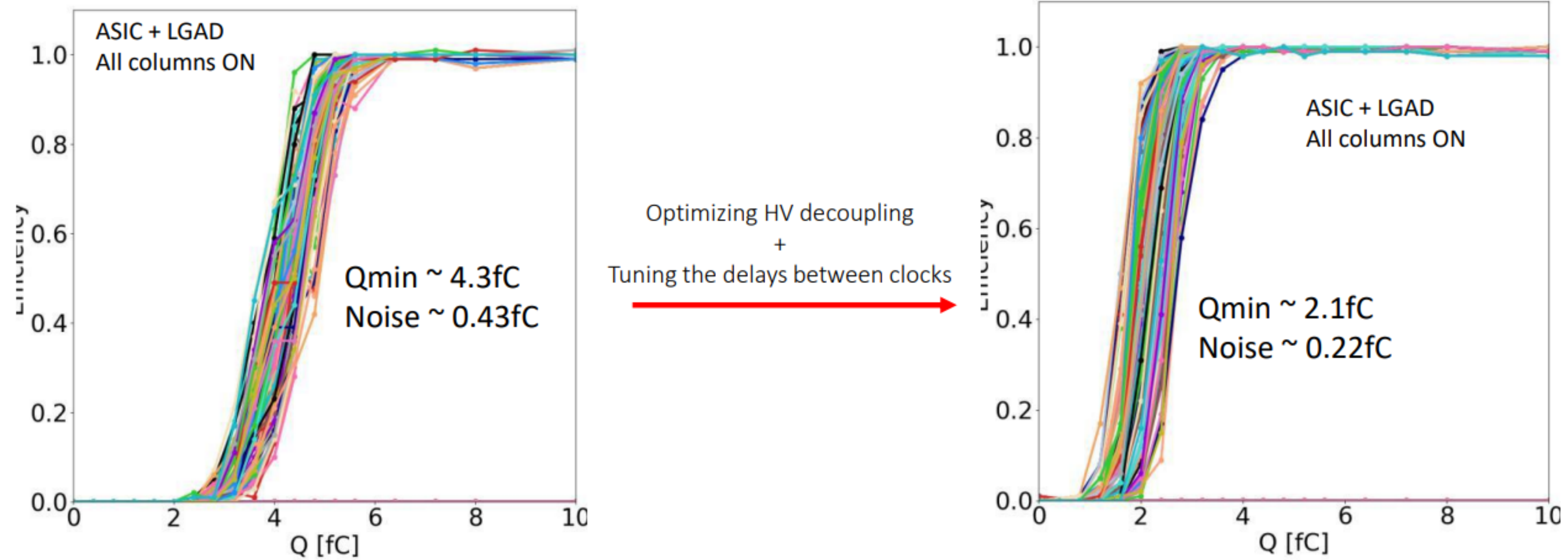
- We verified the operation range from -30 °C to +40 °C
- All the bumps show connectivity in the range of -30 °C to +40 °C
- Safe operational temperature range to be studied

Conclusions

- HGTD modules were hybridized and assembled successfully
- The effect of bump size on the noise was studied with early module prototypes. We conclude that there is no significant effect of the bump size (from 80 μm to 115 μm) on noise
- Full firmware and software (AlVin) developed for the characterisation of full size modules
- The studies done for full module on test PCB show that the module can reach down to 3.2 fC of threshold (without implementing clock delay tuning)
- Full HGTD modules with flex were also hybridized and assembled
- The Sr-90 source scan tests show all the bumps are connected in the modules assembled at HGTD assembly sites at IFAE and IHEP
- Overall, the hybridisation process for HGTD resulted in modules that satisfy the initial requirements with a 100% yield of working channels

Backup Slides

WBS 8.2.1: Altiroc2 performance - Qmin (ASIC + LGAD sensor)



Limitation for minimum achievable charge (Qmin) is due to digital noise injected through the ground of the preamp

Further improvements are implemented in ALTIROC3 to reduce this noise issue