WG5 - Electronics for Gaseous Detectors

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Tasks of WG5 described in chapter 4.5 of the extended DRD1 proposal (p.63-74):
https://indico.cern.ch/event/1273991/attachments/2668256/4624404/RD_EXTENDED-PROPOSAL__DRD1.pdf

Task1: Front-End ASICs

Reference	Description	Deliverable Nature
D5.1.1	High-rate RPC electronics	Survey on low-threshold discriminators
D5.1.2	Front-end ASIC for TPCs - WP4	Description of parameters
D5.1.3	Front-end ASIC for straw chambers - WP3	Description of VMM3/3a
D5.1.4	Front-end ASIC for straw chambers - WP3	VMM3b or new ASIC design
D5.1.5	Front-end ASIC for MPGDs - WP1	Community survey on chip requirements

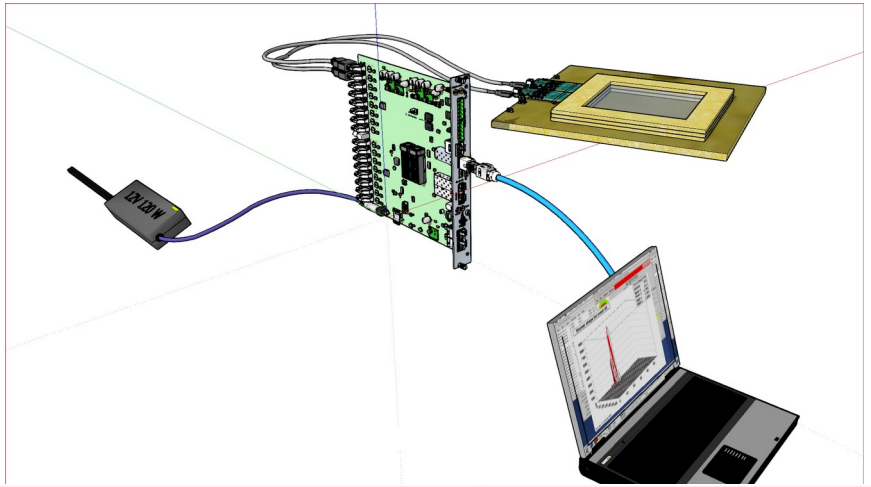
Table 15: WG5 - Objective 5.1: Front End Challenges

Task2: Modernized Readout System

Reference	Description	Deliverable Nature
D5.2.1	SRSe WP1-8	eFEC
D5.2.2	SRSe WP1-8	VMM software and firmware migration
D5.2.3	SRSe - WP1-8	DAQ and reconstruction software
D5.2.4	SRSe	Testing and integration
D5.2.5	Common DAQ/SRS WP1,4	SAMPA implementation
D5.2.6	Common DAQ/SRS - WP4	Timepix3 implementation
D5.2.7	Common DAQ/SRS	*RPC front-end implementation?*
D5.2.8	SRS upgrades	2.5 Gbit Ethernet and L0 trigger ß

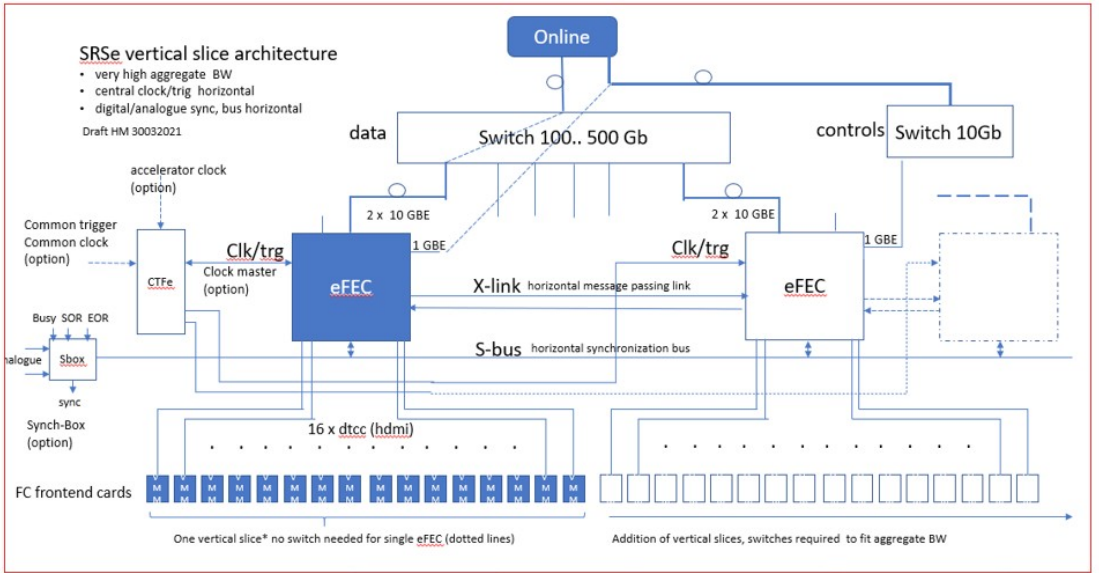
Table 16: WG5 - Objective 5.2: Modernised Readout System

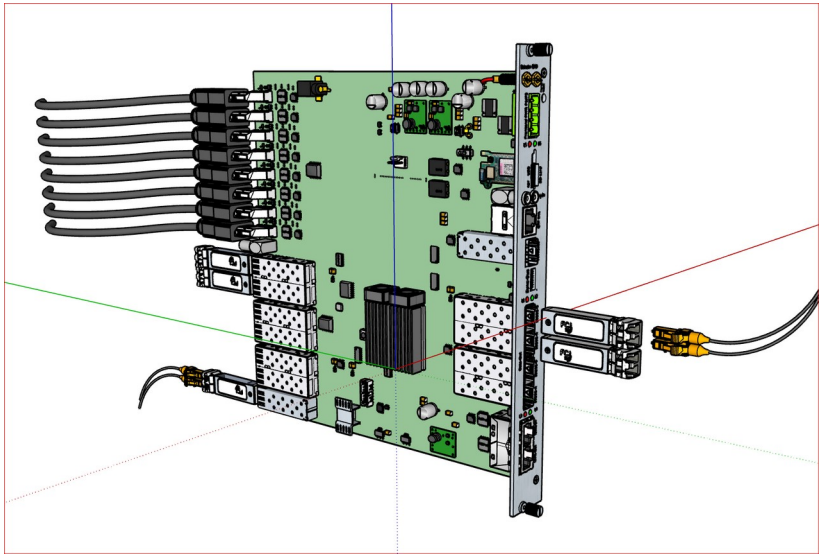
e Scalable Readout System



Status: planned

FPGA: Ultrascale+ with embedded Linux
Output links: 2 x 10 Gbps





Task 3: Beyond Readout

Reference	Description	Deliverable Nature
D5.3.1	MPGD HV - WP1	Stabilised voltage divider
D5.3.2	MPGD LV - WP1-8	PBX
D5.3.3	Monitoring - WP1-8	SoC investigation

Table 17: WG5 - Objective 5.3: Beyond Readout System

DRD1-WG5 ↔ DRD7

- Projects in DRD7 will target common generic developments, or exploration of cutting-edge technologies requiring negotiated access to frameworks and complex design flows. They may involve high costs, expert coordination or unique expertise, and can possibly only be effectively delivered as a common community effort. They will follow design practices enabling later volume production in industry and/or using COTS components.

- Projects in individual DRDs will target developments driven by DRD-specific requirements. They will typically be smaller-scale prototypes exploring or benchmarking novel concepts or technologies and delivering demonstrators. They will focus on diversity and originality, but will not necessarily be suitable for large-scale production.

→ We should try to identify if *common generic development* concerning ASIC and/or DAQ can be setup across our collaboration

CONTACT PERSONS: Sorin Martoiu, Marco Bregant

New ASICS

Status 27.5 : DRD7 is calling for projects in electronics, following the priorities established in the ECFA Detector R&D roadmap document **before 30 June 2023.**

Ideally a chip matrix created after the 2021 Topical Workshop on electronics for MPGDs

Name	Exp	Detectors	£Ch	Shaping	Noise	Range [ke]	Input signal	Pol.	ADC [#bits]	fs [MHz]	P/ch [mW]	Feature	Technology	Radhard
AFTER	T2K; T2K upgrade	TPC, micromegas end-plate	72	50-1000	(350-1800)e +(22-1.8)e/pF	4 ranges: 750/1500/2250/3800	current	both	external 12-bit ADC	1 to 50 SCA sampling	8	SCA	0.35 µm CMOS	N.D.
AGET	ACTAR, AT-TPC, SΠRIT	MGPD+DSSD	64	25-500	(435-34000)e +(19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	external 12-bit ADC	1 to 100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 µm CMOS	N.D.
DREAM	CLAS12	MGPD	64	25-450	(394-2140)e + (10-0.34)e/pF	4 ranges: 312/624/1248/3744	current	both	external 12-bit ADC	1 to 50 SCA sampling	10	SCA; Trigger	0.35 µm CMOS	N.D.
GEMROC	(Client under NDA)	GEMs	64	30-200	N.D.	1fC -> 500fC	charge	negative	N.D.	40MHz	1mW	//	0.35 SiGe	N.D.
HARDROC3	ILC CALICE sDHCAL	RPC	64	50-150 (Q) 20 (T)	N.D.	10fC -> 50pC	current	negative	N.D.	50MHz	1mW	Zero Suppression	0.35 SiGe	N.D.
PADI-X	CBM	RPC, Diamond, Straw Tubes, Silicon, Micro-Channel Plates, Channel Electron Multiplier, Scintilation, PMT	8	0	N.D.	1 fC - 2 pC	current	pos/neg	external	//	16.8	Setable Input impedance: 50 - 400 Ω	CMOS UMC-180 nm	2.4
PADI-XI	CBM	//	8	2.5-17	N.D.	1 fC - 2 pC	current	pos/neg	external	//	22	Setable Input impedance: 18 - 250 Ω	CMOS UMC-180 nm	2.4
PADI-XII	for future experiments	//	8 or 4 channels	2.5-17	N.D.	1 fC - 2 pC	current	pos/neg	external	//	24 for LED / 32 for PSA	Setable Input impedance: 18 - 250 Ω	CMOS UMC-180 nm	2.4
PETIROC2	CMS Muon	RPC (was designed for SiPM)	32	25-100 (Q)	N.D.	1mV (~1pe)	voltage	both	10 bits	N.D.	6mW	//	0.35 SiGe	N.D.
SAMPA_v4	ALICE	TPC-GEM / MCH-MWPC	32	160/320	550e+25e/pF	400/600 (@160ns) 3100 (@300ns)	charge	pos/neg	10 bits	10 MHz	20	Z.S. Baseline correction. Huffman.	130 nm	N.D.
SAMPA_V5	sPHENIX	TPC-GEM	32	80/160	550e+25e/pF	400/600	charge	pos/neg	10 bits	10/20 MHz	20	Z.S. Baseline correction. Huffman.	130 nm	N.D.
STAGE	HARPO	MGPD+DSSD	64	25-4000	(435-34000)e +(19-7.4)e/pF	4 ranges: 750/1500/6240/62400	current	both	external 12-bit ADC	1 to 100 SCA sampling	10	SCA; Triggerless; selective readout	0.35 µm CMOS	N.D.
STS/MUCH-XYTER2.2	CBM Experiment at FAIR	Microstrip silicon detectors at Silicon Tracking System, GEM detectors at Muon Chamber	128	90-260	550e+25e/pF	624ke with for GEM, 75ke for Silicon	charge	pos/neg	5	continuous-time	10	BaselineCorrection / PeakFinding	UMC 180 nm CMOS	N.D.
VMM3a	ATLAS	New small wheel, sTGC, Micromegas	64	25-200	depends configuration	2pC at 0.5mV/FC, in linear range	charge		3 ADCs per channel, 10b, 8b, 6b	200ns conv. time	~11mW	data driven, Baseline stabilization, neighbouring logic, fast digitisation, Peak Finding, timing information, and many more	130nm GF	>300kRad
WASA	CEPC	TPC, GEM	16	160	533e +9.1e/pF	748.8	charge	negative	10	100M max.	2.33	direct waveform output	65nm CMOS	N.D.

Certainly not possible, but any preliminary ideas/comments are welcome. Full community survey next year. See also presentation tomorrow by Sorin/Marco.