From “Organisation of the DRD7 collaboration” V6, 09/5/23:

- DRD7 is an R&D collaboration, and ***will not provide a design or fabrication service for ASICs or other components***; this is the role of engineering teams at institutes and laboratories participating in the various DRD projects.
- Where common developments across DRDs are agreed, either of IP, or of complete devices or subsystems, ***DRD7 is available to set up a review and coordination body***.
- ***Funding for specific electronic developments and prototypes in DRDs should be allocated to the relevant collaborations***, with prioritisation decisions made by the collaborations ***as part of their funding request and review***. In case of complex electronics developments (and in particular of ASICs), ***a review coordinated by DRD7*** will be instrumental in lowering the development risk and limiting duplication of effort.
- Funding for DRD7 R&D and coordination activities will be separately requested, including the costs of common tools, the costs of specialised personnel (for instance, verification experts), specific R&D developments at both device and system level, and the technical facilities necessary for R&D.
- **Proposals for R&D projects involving electronics and data-processing** can be included in either detector-related DRDs or in DRD7, taking into account the following guidelines:
  - ● Projects in DRD7 will target common generic developments, or exploration of cutting-edge technologies requiring negotiated access to frameworks and complex design flows. They may involve high costs, expert coordination or unique expertise, and can possibly only be effectively delivered as a common community effort. They will follow design practices enabling later volume production in industry and/or using COTS components.
  - ● Projects in individual DRDs will target developments driven by DRD-specific requirements. They will typically be smaller-scale prototypes exploring or benchmarking novel concepts or technologies and delivering demonstrators. They will focus on diversity and originality, but will not necessarily be suitable for large-scale production.

- We should try to identify if *common generic development* concerning ASIC and/or DAQ can be setup across our collaboration
- The targets of tasks in DRD1 WPs (see next slides) are overlapping in many aspects, but still they may require separate developments
- Building blocks and IPs (ASIC sub-blocks, FPGA IPs or software components) may be exchanged within the DRD1 and DRD7 communities, with coordination from relevant bodies.

T3	New front-end electronics	- 1 fC threshold - High-sensitivity electronics to help achieving stable and efficient operation up to ≈MHz/cm^2	WG5, WG7 (7.1,2)	1.1	- Integration of FEE in the detector Faraday cage - Integration of electronics and readout PCB	- Conceptual electronics design based on gas detector simulation and experimental measurements - Development and test of a front-end prototype - High throughput multichannel FE (peak time/amplitude based VMM3a): performance studies and optimization.	IFIN-HH, INFN-FE, INFN-BA, INFN-BO, INFN-TO, IRFU/CEA, IPPLM, INFN-RM2, U Cambridge, CERN
T4	Optimization of scalable multichannel readout systems	- Front-end link concentrator to a powerful FPGA with possibilities of triggering and ≈20 GBit/s to DAQ	WG5	1.1, 1.2	- FPGA-based architecture - FPGA with embedded processing for triggering and ML - Basic firmware and software can be bootstrapped from existing readout system	- First prototype by the end of 2024 for commissioning at test beam - SRS/VMM3a Readout: Continuous and trigger mode, distributed systems, synchronization with other DAQs.	IFIN-HH, INFN-BO, U Bonn, IPPLM, CIEMAT, CERN
T1	Development of front-end ASICs for cluster counting	- High bandwidth - High gain - Low power - Low mass	WG5, WG7 (7.2)	1.1, 1.2	- Achieve efficient cluster counting and cluster timing performances	- Full design, construction and test of the first prototype of the front-end ASIC for cluster counting	IHEP CAS, CNRS-LSBB, INFN-RM1, INFN-LE, INFN-PD, INFN-BA, INFN-TO, SBU, IPPLM
T2	Develop scalable multichannel DAQ board	- High sampling rate - Dead-time-less - DSP + filtering - Time stamping - Track triggering	WG5, WG7 (7.2)	1.1, 1.2	- FPGA-based architecture - ML algorithms-based firmware	- A working prototype of a scalable multichannel DAQ board	IHEP CAS, INFN-LE, INFN-BA, UW–Madison, IPPLM, INFN-BO
T4	Optimization of electronic readout and ASIC development	- Time readout with sub-ns precision - Leading and trailing edge time readout	WG5, WG7 (7.1-2)	1.1	- Dedicated R&D on ASIC	- ASIC development - Development of readout system	INFN-PV, MPP, HUJI, JU-Krakow, AGH-Krakow, CERN, U Bursa, U Manchester, U South Carolina, INP-Almaty

#	Task	Performance Goal	DRD1 WGs	ECFA DRDT	Comments	Deliv. next 3y	Interested Institutes
T4	Low-power FEE	- <5 mW/ch for >10^6 pad TPC - ASIC development in 65 nm CMOS	WG5	1.3	- Continuous vs. pulsed	- Present stable operation of a multi-channel TPC prototype with a low-power ASIC	IHEP CAS
T1	Development of high-granularity demonstrators	- Cell size ≈1 cm^2 - Channel count ≈10k per m^2	WG5, WG7 (7.2)	1.1	- Innovative signal-induction structures to balance readout cost and performance - Front-end electronics	- Performance validation of a technology demonstrator in-beam	VUB and UGent, IP2I, MPP, WIS, INFN-RM2, CERN, INFN-NA, INFN-RM3, INFN-BA, INFN-LNF, CIEMAT, Istinye U, U Cambridge
T4	FEE	- Stability at high input capacitance - Low noise - Large dynamic range	WG5	1.2		- Present an ASIC concept/prototype	IFUSP, NISER Bhubaneswar, INFN-PD, INFN-TS, AGH-Krakow, IPPLM, U Manchester, MSU, SBU, JLab, DIPC
T5	Low-noise FEE	- High input capacitance - Large dynamic range - Fast rise time - Sensitivity to small charges - Low noise	WG5	1.2		- ASIC design - Full readout-chain for multichannel readout solutions for timing ≈10 ps (discrete and ASICs)	USTC, IP2I, IRFU/CEA, GSI, MPP, INFN-PD, INFN-PV, LIP-Coimbra, CERN, U Manchester, MSU, SBU, JLab, INFN-TO, RBI, U Tsinghua, INFN-RM2
T2	Enhanced operation of charge readout across gas densities	- Achieve an ionization-energy threshold of at least ≈keV in the range 10 mbar to 10 bar (and, in the case of noble gases, to saturated vapours and even to the liquid state) with a scalable concept. - Reconstruction of MeV-nuclei of variable stopping power, with mm and sub-mm sampling.	WG1, WG5, WG6, WG7	1.2, 1.4	- High avalanche gain across gas densities in CF_4, H_2, He, Ar, Xe -based TPCs with keV-sensitivity. - Fine track sampling capabilities in the range of 10's of µm to few mm. - High-density and low-power electronics, with the ability to self-trigger. - TimePix-based charge readouts.	- Low-pressure nuclear track reconstruction at ≈10 keV. - 1 keV ionization-energy threshold at high pressure. - Few MeV's-proton tracking at 10 bar in argon-based gas. - Reconstruction of MeV-nuclei with mm and sub-mm sampling at varying pressure and gas conditions. - Stability of reconstruction of nuclear-reaction byproducts over a large range of primary ionizations.	IRFU/CEA, GANIL, U Bonn, ANU, U Zaragoza, U Colorado, Fermilab, UH Manoa, MSU, RWTH Aachen, HUJI, U Bursa, U Bolu-Abant, U Warwick, WIS, CNRS-IN2P3/UGA, ISNAP, U Coimbra, INFN-LNS, SINP Kolkata, U Hamburg, U Aveiro, U New Mexico, AUTH , U Kobe

- Front-end ASIC development mentioned 8 times -> is there potential for common developments?
- DAQ development mentioned 3 times

Electronics wish-list in DRD1

- High performance charge-sensitive front-end circuit specific for medium and large volume gaseous detectors (MPGD, TPC, drift chambers, straw tubes, RPC, …)
  - High input capacitance (2-2000 pF)
  - Low noise/high sensitivity (eg. ~100e@2pF)
  - Low power (~ mW/ch)
  - High dynamic range (12-14bits, 1:50000)
  - Precise timing (10-100ps)
  - High event-rate (1MHz/cm2 -> @1m x 1mm sensitive area/ch -> 10MHz/channel)
- Architectural innovations R&D
  - Versatile front-end circuitry (variable parametric front-end and shaping circuit, variable resource distribution,…)
  - Cluster-counting (continuous readout, 1GHz analog bandwidth front-end, 2GSps high-sampling rate, on-line processing with direct mathematical algorithms or Machine Learning)
  - Deadtime-less readout, self-trigger vs continuous sampling with digital data compression
  - High-rate data-acquisition (> 1MHz/ch, up to Tb/s total DAQ bandwidth – scalable systems mapped on switched networks)
  - Signal/Event Processing on- or off-chip (eg. peak finding, baseline restoration, feature extraction, … - reusable IP library for online use in FPGA/ASIC or offline in software)
- Technological developments
  - High-voltage tolerance/spark protection
  - Detector biasing via ASIC (eg TSV for HV)
  - Combined detector & electronics assembly technology, cooling & services integration (integration of the FE electronics in the detector Faraday cage)

DRD7 Working Groups

High-rate scalable DAQ

Versatile front-end

Precise timing, ADC & TDC

Signal/event processing IPs

WG 7.1: Data density and power efficiency
- Szymon Kulis (CERN), Jeffrey Prinzie (KU Leuven), Jan Troska (CERN)
- High data-rate ASICs and systems
- New link technologies, including silicon photonics technology
- Power conversion and efficiency optimisation

WG 7.2: Intelligence on the detector
- Davide Ceresa (CERN), Francesco Crescioli (IN2P3-LPNHE), Frédéric Magniette (IN2P3-LLR)
- Front-end programmability and modular design
- Intelligent power management
- Advanced data reduction techniques

WG 7.3: 4D and 5D techniques
- Sophie Baron (CERN), Marek Idzik (AGH-Kracow), Adriano Lai (INFN-Cagliari)
- High-performance sampling
- High-precision timing distribution
- Novel on-chip architectures

WG 7.4: Extreme environments
- Giulio Borghello (CERN), Oscar Francisco (Uni-Manchester), Manuel Rolo (INFN-Torino)
- Cryogenic technology and operation
- Thermal management of ASICs
- Radiation hardness

WG 7.5: Backend systems and COTS
- Conor Fitzpatrick (Uni Manchester), Niko Neufeld (CERN), NN
- Use and adaptation of advanced COTS technologies
- Real-time software and firmware development
- System-level control and readout

WG 7.6: Complex imaging ASICs and technologies
- Marlon Barbero (IN2P3-CPPM), Michele Caselle (KIT), Iain Sedgwick (RAL), Walter Snoeys (CERN)
- Common access framework to selected imaging technologies
- Common IP for imaging ASICs
- 3D integration and interconnects

WG 7.7: Tools and technologies
- Kostas Kloukinas (CERN), Xavi Llopart (CERN), Mark Willoughby (RAL)
- Access and support to qualified technologies and tools
- Investigation of emerging microelectronics technologies
- Support and training for device and systems development and verification
- Common IP and design reuse

- Gaseous detector type front-end does not seem to be represented. Perhaps we can propose a sub-task (eg. in WG 7.6)
- Common developments focusing on a smaller number of optimisation directions which could satisfy requirements of more detector technologies and applications would bring more visibility and support
- Exchange and/or common development of building blocks and IPs (ASIC sub-blocks, FPGA IPs or software components) should be encouraged

Backup slides

Task	Performance goal	Comments	Possible deliverables next 3-5 y
(Muon systems) New front end electronics	- 1 fC threshold - Geometrical avalanche quenching - High sensitivity electronics and new detector structures to achieve stable and efficient operation (rate, occupancy) up to O(MHz/cm2)	- Study of the integration of the FE electronics in the detector Faraday cage - Study of the integration of electronics and readout PCB	- Conceptual electronics design based on gas detector simulation and experimental measurements - Development and test of a front-end prototype
(Large-volume drift chambers) Front-end ASIC for cluster counting	- High bandwidth - High gain - Low power - Low mass	achieve efficient cluster counting and cluster timing performances	full design, construction and test of a first prototype of the front-end ASIC for cluster counting
(Straw chamber) Electronic readout, ASIC	- Time readout with sub-ns precision - Leading edge and trailing edge time readout	- Dedicated R&D on ASIC	- ASIC - Readout system
(Time Projection Chambers) Low-power FEE	•< 5 mW/ch for >1e6 pad TPC - ASIC development in 65 nm CMOS	•continuous vs. pulsed	- Present stable operation of a multi-channel TPC prototype with a low-power ASIC
(Gaseous photon detectors) FEE	- High input C - Low noise - large dynamic range	•	- present an ASIC concept/prototype
(Gaseous timing detectors) Low-noise FEE	- High input C - large dynamic range - Fast rise time - sensitivity to small charge - Low noise	•	Define an ASIC

Task	Performance goal	Comments	Possible deliverables next 3-5 y
(Muon systems) Scalable multichannel readout system	•Front-end link concentrator to a powerful FPGA with possibilities of triggering an O(20GBit/s) to DAQ	- FPGA based architecture - FPGA with embedded processing for triggering and ML - Basic firmware and software can be bootstrapped from existing readout system	First prototype by end of 2024 for commissioning at test beams
(Large-volume drift chambers) Scalable multichannel DAQ board	- High sampling rate - Dead-time-less - DSP and filtering - Event time stamping - Track triggering	- FPGA based architecture - ML algorithms-based firmware	working prototype of a scalable multichannel DAQ board
(Straw chamber) Electronic readout, ASIC	- Time readout with sub-ns precision - Leading edge and trailing edge time readout	- Dedicated R&D on ASIC	- ASIC - Readout system