Subject: Interplay between DRD1 and DRD7 Collaborations
Date: Friday 30 June 2023 at 22:32:00 Central European Summer Time
From: Sorin Martoiu
To: Francois Vasey, Dave Newbold
CC: Marco Bregant, Sorin Martoiu, Jochen Kaminski, Hans Muller, Maxime Gouzevitch, Michael Lupberger, Eraldo Oliveri, Anna Colaleo, Leszek Ropelewski
Attachments: drd1_electronics_tables.pdf, RD_EXTENDED-PROPOSAL__DRD1 - WG5-Electronics.pdf

Dear Francois, Dave, and colleagues,

We contact you as representatives of DRD1 Collaboration appointed for the relation with DRD7. Following an internal review of scientific projects proposed in DRD1 we identified a number of R&D tasks listed in the DRD1 Work Packages aimed to deliver specific ASIC front-ends or Data Acquisition Systems which are supported by a large number of institutes. An attempt to summarize the research directions and deliverables is given in the itemized list below.

Several of the topics listed potentially map with activities of the DRD7 Working Groups (eg. Precise timing and ADC/TDC blocks in WG 7.3; High-rate scalable DAQ in WG 7.5 or Versatile front-end in WG 7.2), but generally the subject of *high-performance charge sensitive front-end and readout circuits optimized for larger capacitance detectors specific for medium and large volume gaseous detectors*, we don't find covered in the DRD7 theme list. Following discussion in the recent DRD1 Collaboration meeting, we would like to propose the addition of this task as a research theme in the DRD7 organigram. We believe this would bring more visibility and expand the funding possibilities of interested institutes, also allowing for a more efficient collaboration for researchers involved across DRD7 Collaboration. We wonder if an additional Working Group devoted to this is needed, or this theme can be accommodated in the existing structure.

In addition to the aspects related to ASIC design of this research theme, there are also a number of technological aspects that need to be addressed as the high-voltage tolerance, integrated discharge protection or assembly developments in relation to the effort of bringing the front-end electronics inside or closer to the gaseous detector pressure vessel, which will imply more advanced packaging and cooling technologies. Access to these special technologies will be very difficult for individual institutes or project collaborations if not backed by DRD7.

Last but not least, the DRD1 community has strong interest in sharing and co-designing front-end building blocks, complete ASICs or processing IPs with research teams across other DRD Collaborations, with proper protection of Intellectual Property and authorship recognition, where DRD7 Collaboration may play a coordinating role.

We would be happy to discuss further in a zoom meeting in the following days. Regarding the quantitative information about institutes involved and research teams, this information is being collected inside DRD1 as well, as part of the proposal definition phase. This process will require time and further interactions but we are clearly interested in consolidating the interplay between DRD1 and DRD7 as much as we can identify what is better to do in DRD1 and what is better to have in DRD7. Attached is the list of electronics related tasks in the present DRD1 Work Packages draft. The institute list related to each task is not yet definitive. In addition, we attach the electronics related chapter of the current DRD1 proposal draft.

Electronics "wish-list" in DRD1:

- High performance charge-sensitive front-end circuit specific for medium and large volume gaseous detectors (MPGD, TPC, drift chambers, straw tubes, RPC, …)
    - High input capacitance (2-2000 pF)
    - Low noise/high sensitivity (eg. ~100e@2pF; 50mV/fC)
    - Low power (~ few mW/ch)
    - High dynamic range (12-14bits, 1:50000, several strategies)
    - Precise timing (10-100ps - linked to Ion tail processing and extraction of electron

charge peaks)
    - High event-rate (1MHz/cm2 -> several MHz/channel)
- Pixelated readouts (charge- or photon-sensitive detectors with high timing resolution)
    - Optimization of pixel size (>200 μm)
    - Provide a large-area pixel-based readout
- Architectural innovations R&D
    - Versatile front-end circuitry (variable parametric front-end and shaping circuit, variable resource distribution,…)
    - Cluster-counting (continuous readout, 1GHz analog bandwidth front-end, 2GSps high-sampling rate, on-line processing with direct mathematical algorithms or Machine Learning)
    - Deadtime-less readout, self-trigger vs continuous sampling with digital data compression
    - High-rate data-acquisition (> 1MHz/ch, up to Tb/s total DAQ bandwidth – scalable systems mapped on switched networks, generic DAQ for different Front-Ends)
- Platform for sharing and collaborative development of Processing IPs and building blocks
    - Sharing and co-design of front-end building blocks.
    - Signal/Event Processing on- or off-chip (eg. peak finding, baseline restoration, feature extraction, etc.… - reusable IP library for online use in FPGA/ASIC or offline in software)
    - Proper mechanism for open access, end user agreement, protection of Intellectual Property and authorship recognition.
- Technological developments
    - High-voltage tolerance/spark protection
    - Detector biasing via ASIC (eg TSV for HV)
    - Combined detector & electronics assembly technology, cooling & services integration (integration of the FE electronics in the detector Faraday cage)

Sincerely,
Marco Bregant and Sorin Martoiu, on behalf of the Conveners of DRD1 Working Group 5 (Electronics for Gaseous Detectors)