Task	Performance Goal	DRD1 WGs	ECFA DRDT	Comments	Deliv. next 3 y	Interested Institutes
New front-end electronics (WP1 - Muon Systems)	- 1 fC threshold - High-sensitivity electronics to help achieving stable and efficient operation up to ≈MHz/cm^2	WG5, WG7 (7.1,2)	1.1	- Integration of FEE in the detector Faraday cage - Integration of electronics and readout PCB	- Conceptual electronics design based on gas detector simulation and experimental measurements - Development and test of a front-end prototype - High throughput multichannel FE (peak time/amplitude based VMM3a): performance studies and optimization.	IFIN-HH, INFN-FE, INFN-BA, INFN-BO, INFN-TO, IRFU/CEA, IPPLM, INFN-RM2, U Cambridge, CERN, MPP.
Development of front-end ASICs for cluster counting (WP2 - Drift Chambers)	- High bandwidth - High gain - Low power - Low mass	WG5, WG7 (7.2)	1.1, 1.2	- Achieve efficient cluster counting and cluster timing performances	- Full design, construction and test of the first prototype of the front-end ASIC for cluster counting	IHEP CAS, CNRS-LSBB, INFN-RM1, INFN-LE, INFN-PD, INFN-BA, INFN-TO, SBU, IPPLM
Optimization of electronic readout and ASIC development (WP3 - Straw Chambers)	- Time readout with sub-ns precision - Leading and trailing edge time readout	WG5, WG7 (7.1-2)	1.1	- Dedicated R&D on ASIC	- ASIC development - Development of readout system	INFN-PV, MPP, HUJI, JU-Krakow, AGH-Krakow, CERN, U Bursa, U Manchester, U South Carolina, INP-Almaty
Pixel-TPC development (WP4 - Time Projection Chambers)	- Produce 50000-60000 GridPixes to read out a full TPC - Achieve dN/dx counting-resolution < 4%	WG5, WG7 (7.1-2,5)	1.1	- InGrids (grouping of channels) - Low-power FEE - Optimization of pixel size (>200 µm) or cost reduction	- Provide a large-area pixel-based (InGrid) readout module - Measuring IBF for GridPix. Reduction with double-mesh - Present dN/dx measurements in beam - Small area prototypes of MPGD/TimePix hybridisation.	U Bonn, U Carleton, WIS, CERN
Low-power FEE (WP4 - Time Projection Chambers)	- <5 mW/ch for >10^6 pad TPC - ASIC development in 65 nm CMOS	WG5	1.3	- Continuous vs. pulsed	- Present stable operation of a multi-channel TPC prototype with a low-power ASIC	IHEP CAS
FEE cooling (WP4 - Time Projection Chambers)	- Operate 10^6 channels per end-plate	WG5	1.2	- Two-phase CO_2 cooling - Micro-channel cooling with 300 µm pipes in carbon fiber tubes - 3D printing: complex structures, performance optimization, material selection	- Present a prototype of a cooling system for the 10^6 pad TPC option	IRFU/CEA, U Lund, INFN-PI, INFN-LE, INFN-PD
Development of high-granularity demonstrators (WP5 - Calorimetry)	- Cell size ≈1 cm^2 - Channel count ≈10k per m^2	WG5, WG7 (7.2)	1.1	- Innovative signal-induction structures to balance readout cost and performance - Front-end electronics	- Performance validation of a technology demonstrator in-beam	VUB and UGent, IP2I, MPP, WIS, INFN-RM2, CERN, INFN-NA, INFN-RM3, INFN-BA, INFN-LNF, CIEMAT, Istinye U, U Cambridge
FEE (WP6 - Gaseous Photon Detectors)	- Stability at high input capacitance - Low noise - Large dynamic range	WG5	1.2		- Present an ASIC concept/prototype	IFUSP, NISER Bhubaneswar, INFN-PD, INFN-TS, AGH-Krakow, IPPLM, U Manchester, MSU, SBU, JLab, DIPC
Low-noise FEE (WP7 - Gaseous Timing Detectors)	- High input capacitance - Large dynamic range - Fast rise time - Sensitivity to small charges - Low noise	WG5	1.2		- ASIC design - Full readout-chain for multichannel readout solutions for timing ≈10 ps (discrete and ASICs)	USTC, IP2I, IRFU/CEA, GSI, MPP, INFN-PD, INFN-PV, LIP-Coimbra, CERN, U Manchester, MSU, SBU, JLab, INFN-TO, RBI, U Tsinghua, INFN-RM2

Table 1: Tasks related to front-end electronics in DRD1 Work Packages. *The mentioning of Institutes in the draft should be considered exclusively as a preliminary expression of interest or as potential involvement given the role of the institute in the field.*

Task	Performance Goal	DRD1 WGs	ECFA DRDT	Comments	Deliv. next 3 y	Interested Institutes
Optimization of scalable multichannel readout systems (WP1 - Muon Systems)	- Front-end link concentrator to a powerful FPGA with possibilities of triggering and ≈20 GBit/s to DAQ	WG5	1.1, 1.2	- FPGA-based architecture - FPGA with embedded processing for triggering and ML - Basic firmware and software can be bootstrapped from existing readout system	- First prototype by the end of 2024 for commissioning at test beam - SRS/VMM3a Readout: Continuous and trigger mode, distributed systems, synchronization with other DAQs.	IFIN-HH, INFN-BO, U Bonn, IPPLM, CIEMAT, CERN
Develop robust, compact, and low power DAQ for low rates (WP1 - Muon Systems)	- 256 channel readout - 100 W or less - 1200 cc DAQ volume - Rugged design for remote (<1 km), e.g. underground operations	WG5		- Muon rates from few Hz to few events per day	- Deployed and tested at depth	OXY
Develop scalable multichannel DAQ board (WP2 - Drift Chambers)	- High sampling rate - Dead-time-less - DSP + filtering - Time stamping - Track triggering	WG5, WG7 (7.2)	1.1, 1.2	- FPGA-based architecture - ML algorithms-based firmware	- A working prototype of a scalable multichannel DAQ board	IHEP CAS, INFN-LE, INFN-BA, UW–Madison, IPPLM, INFN-BO

Table 2: Tasks related to Data Acquisition Systems in DRD1 Work Packages. *The mentioning of Institutes in the draft should be considered exclusively as a preliminary expression of interest or as potential involvement given the role of the institute in the field.*