DRD1

DRD1 EXTENDED R&D PROPOSAL
Development of Gaseous Detectors Technologies

Abstract

The document provides an overview of the state of the art and challenges for various detectors concepts and technologies, as well as a detailed list of R&D tasks grouped into Work Packages (WPs) that related to the strategic R&D programs to which funding agencies might commit, with related infrastructures and tools necessary to advance the technological goals, as outlined in the ECFA R&D roadmap. The main DRD1 document is structured into chapters, each describing the activity planned by the eight Working Groups (WG), which are the core of the future scientific organization. The current DRD1 proposal concentrates on the collaborative research program for the next 3 years.

On-line version: `https://cernbox.cern.ch/s/BKQsu6oiuhPWDaa`

Geneva, Switzerland
June 29, 2023

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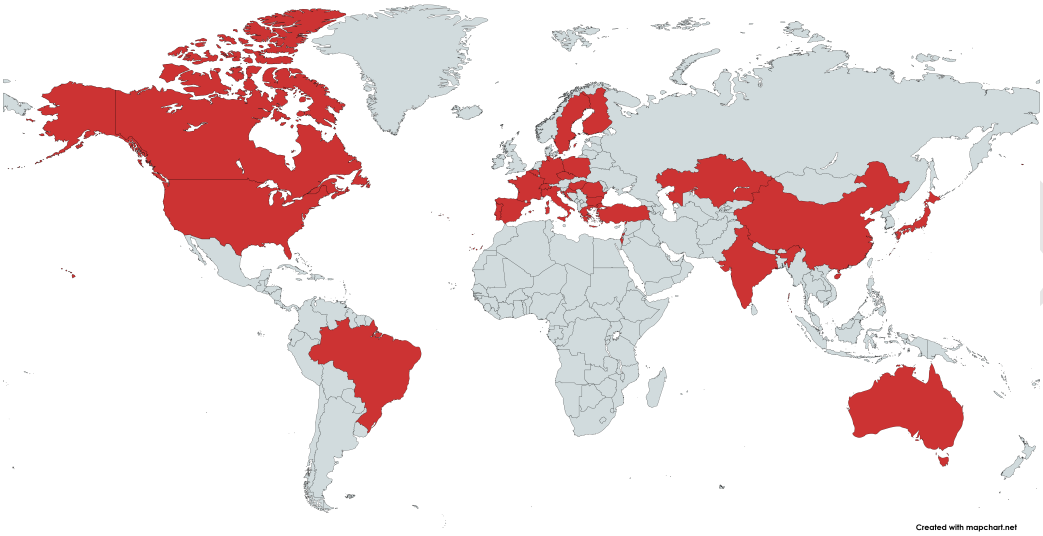

Figure 1: DRD1 Country Map (created with mapchart.net).

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4.5 Electronics for Gaseous Detectors [WG5]

The DRD1 Working Group 5 (WG5) takes responsibility for the development, application and dissemination of electronic components required to operate and further advance Gaseous Detectors (GDs). As an integral part of the detector system, the tools of WG5 are developed together with the e.g. detector amplification structures and enable their improvements. After the introduction in Section 4.5.1 and a summary of the state-of-the-art (Section 4.5.2) the major tasks are outlined in Sections 4.5.3 to 4.5.5 and summarised in Tables 16-18.

WG5 topically differentiates itself from ECFA DRD7 in the sense that it focuses on GDs and the electronics required for their R&D and application in small- to mid-size experiments. Methodologically, WG5 is based on the specific requirements of DRD1, developments by the community for the community and dissemination opportunities to future facilities and their experiments. Close exchange with DRD7 is achieved through the membership of electronic experts in both collaborations.

4.5.1 INTRODUCTION

The development of dedicated GD electronics is of major relevance for the advancement of detectors, their operation, qualification and application in experiments. This is recognised and fully supported by large experiments, which in the past often profited from merging R&D electronics into their final DAQs as for the DAQ of the European Spallation Source or the ATLAS New Small Wheel.

WG5 will, compared to DRD7, address the electronics need during the R&D phase, where e.g. radiation hardness, high-speed links, data reduction, dense integration and experiment-specific front-end ASICs with the highest performance play a subordinate role. The aims are to develop and provide well-suited service electronics in smaller quantities such as high- and low-voltage systems, monitoring equipment (Section 4.5.5) and in particular DAQs (Section 4.5.4) that are well-supported, can be maintained by the community with limited manpower and require a short training period until efficient use is reached. In a similar effort, the development of front-end ASICs for the specific needs of the different GD technologies (Section 4.5.3) could be supported. This working group, therefore, is concentrating on developing a platform for R&D detectors and introductory test systems for large experiments. A community survey has shown that the Scalable Readout System (SRS) [68] developed by the RD51 Collaboration was a huge success, and many groups familiar with the system have mentioned that continued support and development of new features are among the most important tasks of DRD1. The requests for additions reflect the increased diversity of the community and range from analogue and discrete readouts to multichannel integrated ASICs for multi-purpose data acquisition. Also, the application requirements mentioned in the survey show a large almost uniform distribution of pixel readout, strip readout and waveform digitization. Also, non-conventional features like high time resolutions (sub ns), FPGA-based pre-reconstruction and wide dynamic ranges are of interest for many groups. Finally, support for noise reduction, grounding, shielding and spark protection was mentioned with similarly high numbers as other future challenges.

4.5.2 STATUS OF READOUT SYSTEMS FOR GASEOUS DETECTORS

The readout of multichannel gas detectors starts with a Front-End (FE) layer on the detectors, typically implemented as an array of plugin carrier cards (hybrids) with a number n_{chip} of ASICs. These integrate each a number n_{ch} of readout channels and, depending on technology and detector type, convert the primary charge into voltage signals that can be transmitted over front-end links to a Front-End Concentrator (FEC) layer, normally located in a crate-powered readout back-end. Software control, associated with DAQ online software, is responsible for transmitting user-defined commands and configuration data together with common clocks and optional triggers and to all ASICs on the front-end. In return, the ASICs send triggered or untriggered serial channel data over front-end links to the FECs. A scalable system transmits and receives over one single front-end link per hybrid to make it a completely independent vertical readout slice with $n_{chip} \times n_{ch}$ channels connected to one of n_{link} link-ports of a FEC. In order to avoid a bandwidth limit in the front-end, the link bandwidth must be higher than the maximum output bandwidth that the ASIC output can provide. A single FEC can then seamlessly concentrate the stream of event fragments from all connected ASICs in a single transit buffer integrated inside an FPGA. Single FEC readout systems hence consist of n_{link} non-saturating, vertical slices with n_{link} front-end links, concentrating $n_{chip} \times n_{ch} \times n_{link}$ channels with transit lifetimes up to tens of microseconds before being transmitted to a very high-bandwidth network link connecting the online system. In general, an array of n_{FEC} FECs transmits over n_{FEC} network links to a non-blocking network switch to the network port(s) of the Online system. Small systems with typically a single FEC however can make use of a Laptop with 1 Gbit network ports controlled by standard DAQ and Control and data analysis software. Large systems require an online system running on computers with hundreds of Gigabit I/O capacity and disk arrays to cope with the incoming bandwidth. Scalable systems can use the same DAQ and control software both on large or small systems, starting with a single hybrid up to a number of hybrids at which the I/O capabilities of the connected Online system start to limit the scalability. Higher scalability can be reached by adding links, disks, switches and computers to the online system. On the FEC level, the scaling limit can also be reduced by implementing user-defined real-time triggers in the firmware in the FPGAs, to remove insignificant subevents from the transmission to the online links. Algorithms are detector specific and must be completed within the lifetime of the subevents in the FPGA-embedded buffers. The use of state-of-the-art FPGAs in the next generation of FECs is intended to concentrate an even higher number of channels to increase both the effective detector regions and trigger efficiencies.

Readout System for MPGDs: Within the RD51 collaboration, the community has agreed on a common effort to develop a central readout system: the SRS (Fig. 5 [69]). It is developed by the community for the community, which also maintains and further develops it as a system directly usable or adaptable to the needs of the R&D groups. Improvements and extensions by single or several groups together are fed back to the whole community. The success of SRS allows the R&D groups to focus primarily on detector developments. SRS is a scalable readout concept for MPGD detectors, consisting of a crate-resident SRS backend and a detector-resident front-end. The SRS paradigm splits the SRS backend and front-end into fully functional, vertical DAQ slices allowing to start with a single, 128-channel front-end card (= hybrid, n_{ch} = 128) connected over an HDMI cable to a Front-End Concentrator Card (FEC) with link adapter for analogue or digital front-ends. Small systems can get aggregated in units of 128 channels and operated with the same DAQ software as required for large systems. The addition of more 128-channel slices is native to SRS and the reason for the name “scalable”. By 2023, the MPGD community deployed more than 100 small and large SRS systems internationally for different research purposes. At CERN, SRS helped to bootstrap readout and test of detectors of e.g. for ATLAS, ALICE and CMS.
SRS is designed to work with different front-end ASIC technologies, initially implemented with the analogue APV-25, followed by Timepix and since 2019 via the digital VMM3a ASIC, allowing for higher rates, zero-suppression and a wide range of configuration settings to match a wider range of detectors. Further SRS front-ends in preparation are SAMPA and Timepix3. SRS hybrids plug directly onto detectors via connectors standardized for MPGDs. The VMM hybrid is by default equipped with general-purpose coolers, dissipating up to 4 Watts per 128 channel hybrid. The readout links are HDMI A-D cables, used for transmission of very high bandwidth, LVDS-encoded data, configuration, clock and trigger and, optionally power. With externally supplied power and a small Powerbox, HDMI links can be as long as 30 m. VMM hybrids transmit 2x 400 Mbps per HDMI cable, resulting in self-triggered hit rates of up to 8.9 Mhit/s per hybrid. With 8 connected hybrids per FEC, up to 1k channels can be read out per FEC. SRS Mini-crates can house 2 FEC/DVMM for up to 2k channels. Euro-crates provide slots and power for up to 8 FEC/DVMM slots for up to 8 k channels. SRS hardware is

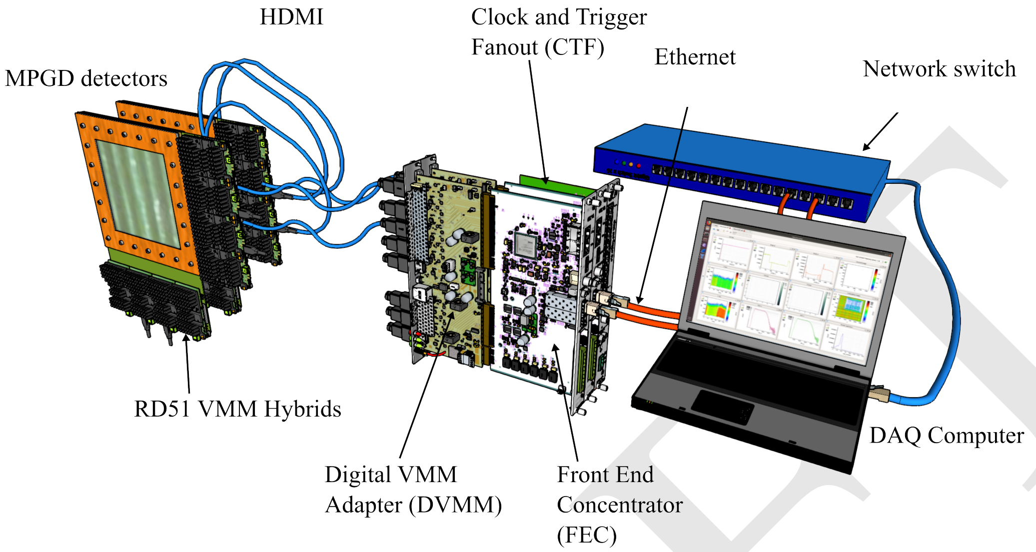

Figure 5: Schematic display of the SRS in the flavour with the VMM as front-end chip. Each of the two exemplary MPGD detectors is read out by eight VMM hybrids (each hybrid: $n_{ch} = 128$, $n_{chip} = 1$). All VMM hybrids of one detector can be connected with each one HDMI cable to the DVMM adapter card of one FEC ($n_{link} = 8$). Several FECs can be connected to a DAQ computer by an Ethernet network switch.

available for CERN users via the CERN store, or alternatively commercially from two producers. Detailed SRS documentation on HW, SW and FW with user FAQ is available on public drives and GitHub. SRS with the VMM comes with software for mid-size systems, data acquisition, online monitoring and data reconstruction as input to dedicated analysis. The FEC-to-online links are so far implemented via 1 Gbit Ethernet UDP standard via copper or fibre, with a planned firmware upgrade for 2.5 Gbit Ethernet. Another firmware project plans to implement the ATLAS L0 trigger mode for the VMM front-end to complement the triggerless readout mode preferred by most users.

Readout System for RPCs: The main feature of an RPC detector is a high timing precision related to the fast rise time of the signal. The time resolution can go from a few ns for a large gas gap detector down to a few 10s of ps for a multi-gap detector. The charge produced in avalanche mode fluctuates from a few pC up to $\approx$100 pC). The pickup charge is significantly smaller than the avalanche charge and stays within a few 100 fC. The size of the pick-up strips or pads is kept at the centimetric range. Reducing it may improve the spatial resolution, but would reduce the charge amount per strip/pad. This feature defines the typical properties of RPC electronics:

- A pre-amplifier that can be coupled with a shaper
- A fast discriminator in a range from 1 to hundreds of fC. In some cases, like calorimetry applications, multiple discriminator levels can be used for a semi-digital readout.
- A TDC to tag the rising (*Tr*) (and possibly falling edge - *Tf*) with a precision significantly better than the time resolution of the detector to read. The Time-Over-Threshold (*TOT* = *Tf* - *Tr*) can be subsequently used to estimate the deposit charge by the particle.

As of today, there are numerous readout ASICs, discrete readout systems pairing a pre-amplifier and a discriminator, and Front-End-Boards in the RPC community tailored to particular needs. The way the electronics are connected to the pickup system is also peculiar to each system: soldered coaxial or twisted-pair cables, commercial connectors, and direct bonding, among others. Most of the RPCs target a 2D readout. This can be achieved either using pads or using specific geometries of strips: partitions with short strips, x and y strips or long strips with double-sided readout, where the relative time of transition of the signal is used to define the position. Each strategy has its advantages and disadvantages, but it strongly impacts the design of the electronics.

Readout System for TPCs: Signals in TPCs often have a larger time elongation because of the longer drift distances and thus larger longitudinal diffusion of the signals as compared to planar tracking detectors. Therefore, signals have a higher probability of overlapping. To be able to identify and reconstruct correctly two overlapping events, the signal is sampled with a Fast Analogue to Digital Converter (FADC). Pixel-TPCs, due to their low occupancy, are less affected. In general, TPCs require a trigger signal which starts the time measurement until the charges arrive at the readout for the correct reconstruction of the third coordinate of the track position. Currently, only very few ASICs fulfil the fast sampling requirements of traditional TPC readout, most of which have been developed exclusively for large experiments like ALICE. The backend electronics necessary to operate these chips is complicated and tailored for the corresponding experiments. Besides, the availability of ASICs can be very limited. Many smaller experiments cannot find well-suited electronics and are required to either operate ASICs with inadequate timing properties or have to resort to using electronics designed for planar tracking detectors. Pixel-TPC developments employ the Timepix ASIC implemented in the SRS and recently Timepix3, for which the implementation in SRS is ongoing.

Readout System for Straw Detectors: For straw chambers, the main parameters to consider are the drift time and collected charge. The drift time t_d depends on straw diameter d_s and wire diameter d_w. For instance, d_s = 5 mm and d_w = 30 μm, results in a maximal drift time of $t_d \approx$ 50 ns. For such a configuration, the produced charge could reach up to 50 fC in Ar/CO2 mixture. To reduce the drift time, d_w should increase and d_s decrease, reducing the amplification field and collected charge. This can be compensated by a larger applied HV, with an increased risk of discharge. Optimal electronics for a straw tube requires a low threshold sensitivity of 5-20 fC and a good double pulse resolution, i.e. the ability to separate signals with a time difference of the order of t_d. This implies a dead time smaller than t_d of one given electronic channel. The electronic shall contain a TDC module to resolve the position of the fast signal with a resolution of 1 ns or better. This information is used to measure offline the impact parameter of the signal with respect to the wire (usually referred to as space resolution). A measurement of the position of the signal along the wire can be obtained in that case from a double-sided readout.

4.5.3 FRONT-END CHALLENGES FOR FUTURE FACILITIES, EXPERIMENTS AND APPLICATIONS

In future, the electronics for **RPC** detectors will meet the challenge of high rates and faster timing. The usage of RPCs in experiments with a high rate of particles per cm² is becoming more and more frequent. The development of thinner electrodes with lower bulk resistivity leads to a faster charge evacuation from inside the gap. It also reduces the screening effect and increases the pick-up charge. A smaller gas gap allows for the reduction of the produced charge. Consequently, the discriminator threshold will be reduced to keep the same efficiency. The typical target for high-rate application is 1-10 fC. It implies excellent control over the detector and electronic noise via innovative grounding schemes. The new electronics have to cope with much higher transmission rates and the usage of optical gigabit transmission would become more and more common. The timing challenge is motivated by the common usage of single-gap and multi-gap RPC detectors such as TOF or VETO. The increased number of electrodes and gas gaps in multi-gap RPCs leads to a significant improvement of the timing resolution. This requires the development or application of higher-precision TDCs, synchronization and high-precision clock distribution.

For the **TPC** community, a flexible ASIC not adapted to specific operating conditions of a large experiment, implemented in a flexible, well-supported backend is much sought after and is highly desirable for numerous small experiments and

R&D projects. For the Pixel-TPC with GridPix readout, Timepix3 with simultaneous charge and time measurement and an ASIC with optimised pixel size are key. In addition, TPCs for rare event searches have very diverging requirements. For example, some of these experiments have to run triggerless, while others need a continuous readout. For the latter, a trigger signal has to be synchronized to ASIC clocks. Negative ion TPCs have drift times in the order of milliseconds, with correspondingly long signal-shaping-time requirements.

Straw Chambers require a versatile ASIC including a TDC and an ADC for individual channels. It is also important to have at least one analogue multiplexed output channel for debugging and monitoring purposes. This condition implies two different frequencies to control the TDC ($\approx$ 1 GHz) and the ADC ($\approx$ 40 MHz). The TDC resolution sho be at least 1 ns and ADC few fC/mV and more.

uld In **general**, detector R&D programs require fast, low-noise, high-bandwidth and multi-channel ($\approx$100) front-end electronics, often including embedded digital online processing of data. Novel detector readout technologies, like cluster counting, may require the development of entirely novel front-end topologies as opposed to the classical charge-preamplifier-discriminator or ADC chain. In addition, gaseous detectors pose a specific set of challenges to the front-end electronics design than for other detector technologies, like high-current transient or spark tolerance, high dynamic range, high-rate capabilities or deadtime mitigation techniques. These requirements are often conflicting with each other, as emphasized previously, making the technological and architectural choices very difficult. As an example, the ADC design performance benefited greatly from technology scaling, while, on the other hand, the dynamic range capability of analog circuits has inherently suffered with scaling. Additionally, it was also observed that architectural innovation has played a significant role in the performance evolution of mixed-mode circuits like ADCs, thus signifying that more mature technological nodes may still benefit from this evolution. This entails a specific front-end electronics R&D effort tailored to the requirements of GDs, while, nevertheless, in line with the technological developments the broader high-energy physics scientific community is targeting. Historically, this effort was predominantly conducted on a project basis with the effort distributed among the community but essentially uncorrelated, supported mainly by the large research communities of large-scale high-energy physics experiments. Given the costs of such enterprises, smaller, blue-sky R&D developments on the other hand, which could not afford the expense of dedicated electronics development were left often to search for available ASICs, many times only loosely adapted to their requirements, adding significant delays and overheads to their projects. As new large-scale experimental collaborations are yet to be formed, this effort may be conducted on a more general basis, directed towards a set of collaborative directions that can bring together a number of research teams with different targets, but with similar technological requirements. Modern design practices and tools favour the exchange of architectural blocks in a more collaborative design approach, also as a method to mitigate risks and, thus, reduce the costs of complex designs. In this way, a generic MPGD, TPC or RPC-oriented front-end can be designed and assembled with the requirements of the gaseous detectors community itself, but also leveraging developments of the broader high-energy physics community. Another important aspect is that a successful detector R&D is only possible while accompanied by adequate electronics able to demonstrate the performance evolution. This makes the electronics R&D for gaseous detectors a rather short- or medium-term target, but also implies that resources need to be allocated accordingly.

Reference	Description	Deliverable Nature
D5.1.1	High-rate RPC electronics	Survey on low-threshold discriminators
D5.1.2	Front-end ASIC for TPCs - WP4	Description of parameters
D5.1.3	Front-end ASIC for straw chambers - WP3	Description of VMM3/3a
D5.1.4	Front-end ASIC for straw chambers - WP3	VMM3b or new ASIC design
D5.1.5	Front-end ASIC for MPGDs - WP1	Community survey on chip requirements

Table 16: WG5 - Objective 5.1: Front End Challenges

4.5.4 PLAN FOR MODERNIZED READOUT SYSTEMS

Front-End: As described earlier, various technologies and applications have a wide range of specifications for front-end circuits. Some circuits like VMM3a or a future potential successor may serve the purpose of many MPGD applications, other ASIC front-ends may work better for different applications, from the point of view of input coupling or dynamic range, whether they require triggerless, data-driven, continuous or triggered readout architectures. As the sensitivity and rate capability increase, the data bandwidth of the front-end links increases accordingly. In this respect, copper links are only usable up to a rather short distance, even with the use of state-of-the-art equalisation techniques. Therefore, optical links remain the best choice. In addition to the increased data-rate capability, they also realise an electrical separation between the detector-coupled front-end and the readout system, which helps to reduce spurious system effects and simplifies the grounding scheme of the experimental apparatus. On the other hand, optical links bring several challenges to the front-end design, one is the increased power required, but also the real estate at the level of the detector front-end, where space is usually limited. Radiation hardness may also be a concern in many cases. Several developments are underway in the community to address these issues, with products already designed and used in the LHC experiments. In some cases, industrial partners are developing products tailored for specific scientific use together with the scientific community. This opens up opportunities for bidirectional technology transfer or common developments.

Backend: SRSe is the planned extension of SRS, providing significantly higher readout bandwidth with up to 20 Gbit per eFEC to the online computing system and adding FPGA-embedded trigger processing in the new extended FEC card, named e-FEC. This unified SRS backend card can be housed/powered in the existing SRS crates and combines a FEC and link adapter on a single card. For backward compatibility, the eFEC has 8 configurable HDMI ports, allowing to connect VMM hybrids. For upgrades, 12 new SFP link ports will connect new SRS hybrids, predominantly via optical fibres. Link protocols between the front-end and back-end will be implemented in firmware.

Firmware: While the dimensions and complexities of circuits have increased, programmable digital circuits have evolved a lot over the years, from relatively simple mesh-distributed computing elements to novel emerging architectures that employ more complex or specialized computing units linked by network backbones. This evolution was proven beneficial in many cases. This architectural evolution was accompanied by a hardware description language evolution, which almost aims for a unification of the hardware description language and the computer language paradigms. While this union is still not perfect in many aspects, it is of particular importance in our physics-driven scientific community. It allows applying computer programming skills to develop FPGA firmware. In the same optic, FPGA and CPUs are now more closely coupled together in local or remotely distributed acceleration systems. There are several ongoing efforts towards implementing common abstraction mechanisms or data transport technologies like Remote Direct Memory Access (RDMA) that may be successfully used in data acquisition systems and heterogeneous data processing systems that implement novel technologies as machine learning online processing with e.g. neural networks. Building on top of these developments in synergy with DRD7, the aim is to develop firmware packages for the future SRS system that offer interchangeable and scalable processing libraries including protocol encoding and decoding which are community driven and as much as possible application agnostic.

DAQ: In a first phase, the DAQ for SRSe needs to be bootstrapped from the existing DAQ software (including data acquisition, online monitoring and reconstruction), firmware and slow controls for FECs with and VMM front-end. A generalized front-end link interface and a high-bandwidth online link upgrade are to be added. Taking advantage of the recent Xilinx Ultrascale FPGAs with embedded processors, DDR4 memory can be added and interfaced to the Linux operating system on the FPGA or an embedded CPU.

Testing (Radiation Hardness, Rate Compatibility): Until now, the radiation hardness of electronics was a second-order concern in the electronics design of gasesous detectors. Either the fronend boards were localized far away from the colliding beams being used as muon detectors, or they were used in low rate/low radiation experiments such as TPCs or wire chambers at LEP or Dark Matter search physics. The increasing usage of gas detectors in proton collisions, heavy ions, sometimes very close to the beam axis for increased acceptance, for calorimetry, or tracking in high luminosity fixed target experiments requires particular care for the design of on-detector electronics. Depending on the application, radiation-tolerant design and commercial components can be sufficient, or radiation-hard custom components might be required. Irradiation facilities to test electronics are located all around the world, since they require secondary particle energies from a few keV to a few 100 MeV. Many of them (mainly in Europe) are clustered into the RADNEXT network (https://radnext.web.cern.ch/) pioneered by CERN, others such as CHARM are available at CERN. RADNEXT maintains a database of tested components. Many facilities designed for medical applications can also be used for electronics testing. Depending on the radiation environement of the experiment, gamma photons, thermal neutrons, or high-energy neutrons/hadrons can be required. For the high particle rate expected in muon detectors of future facilities, a dedicated irradiation infrastructure to test the detector itself and emulating the appropriate rate might be required. An example of such a facility is GIF++ [70] at CERN. In that case, the electronics are to be tested for deadtime generated by heavy data rates, and space-time resolution to separate Minimum Ionising Particles (MIPs) from background particles. Detector timing resolution can be tested in facilities with single particle guns and low jitter, such as HZDR [71] in Germany. Together with WG7, these new challenges and requirements for the electronics can be addressed.

Portable μSRS: There is interest (so far from the muography community) in small and portable frontend readout nodes for readout of small gas detectors from inaccessible confined spaces and over long distance. Limited numbers of channels ($<$1k) per μSRS node eliminate the need for crate-based frontend concentrators if the bandwidth of a common network switch is sufficient to transfer the data from all connected nodes to the DAQ. Individual uSRS nodes can transmit self-triggered event data at high rates (>1MHz). The optional fibre interconnection between nodes provides clock synchronization and common control from a single, SoC-controlled master node. A first implementation is the uROC with two HDMI ports for readout of 256 VMM3a channels with 1Gbit/s ethernet uplink and 30 Watt USB-C power delivery.

Reference	Description	Deliverable Nature
D5.2.1	SRSe WP1-8	eFEC
D5.2.2	SRSe WP1-8	VMM software and firmware migration
D5.2.3	SRSe - WP1-8	DAQ and reconstruction software
D5.2.4	SRSe	Testing and integration
D5.2.5	Common DAQ/SRS WP1,4	SAMPA implementation
D5.2.6	Common DAQ/SRS - WP4	Timepix3 implementation
D5.2.7	Common DAQ/SRS	*RPC front-end implementation(tbd)*
D5.2.8	SRS upgrades	2.5 Gbit Ethernet and L0 trigger ß
D5.2.9	Portable, Connected μSRS nodes	readout of distributed, small detectors over long distance

Table 17: WG5 - Objective 5.2: Modernised Readout System

4.5.5 TOPICS BEYOND THE READOUT SYSTEMS

In addition to the readout electronics described in the previous sections, many additional electronics devices are needed to operate a particle detector successfully. In particular, gaseous detectors require several high voltage stages, for which a fine current monitoring system is necessary to detect discharges and prevent any damage to the detector caused by increased currents. To protect the readout electronics in case of discharges spark protection for each channel should be included to save the ASIC, which is generally laid out for much lower voltages than the gas amplification stage. Another large area of expertise necessary for operating gaseous detectors is noise reduction, which is based on correct grounding, shielding and low-noise power supplies. This requires a lot of experience and knowledge, which has to be passed on to younger generations of researchers and extended with new techniques and materials available today. The working group's tasks would also include the dissemination of these concepts and introducing everyone interested in the art of a good experimental setup in synergy with WG8. Finally, gaseous detectors also require a good knowledge of the environmental parameters, which have a significant impact on the performance of the detectors. Therefore, monitoring systems to record a variety of parameters are needed to provide the data for corrections studied in WG3 and allow offline or potentially even online calibration of detector parameters. A new and interesting approach is the use of CPU within a System on Chip (Soc) device to measure and correct for such comparably slowly changing parameters.

Reference	Description	Deliverable Nature
D5.3.1	MPGD HV - WP1	Stabilised voltage divider
D5.3.2	MPGD LV - WP1-8	PBX
D5.3.3	Monitoring - WP1-8	SoC investigation

Table 18: WG5 - Objective 5.3: Beyond Readout System

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