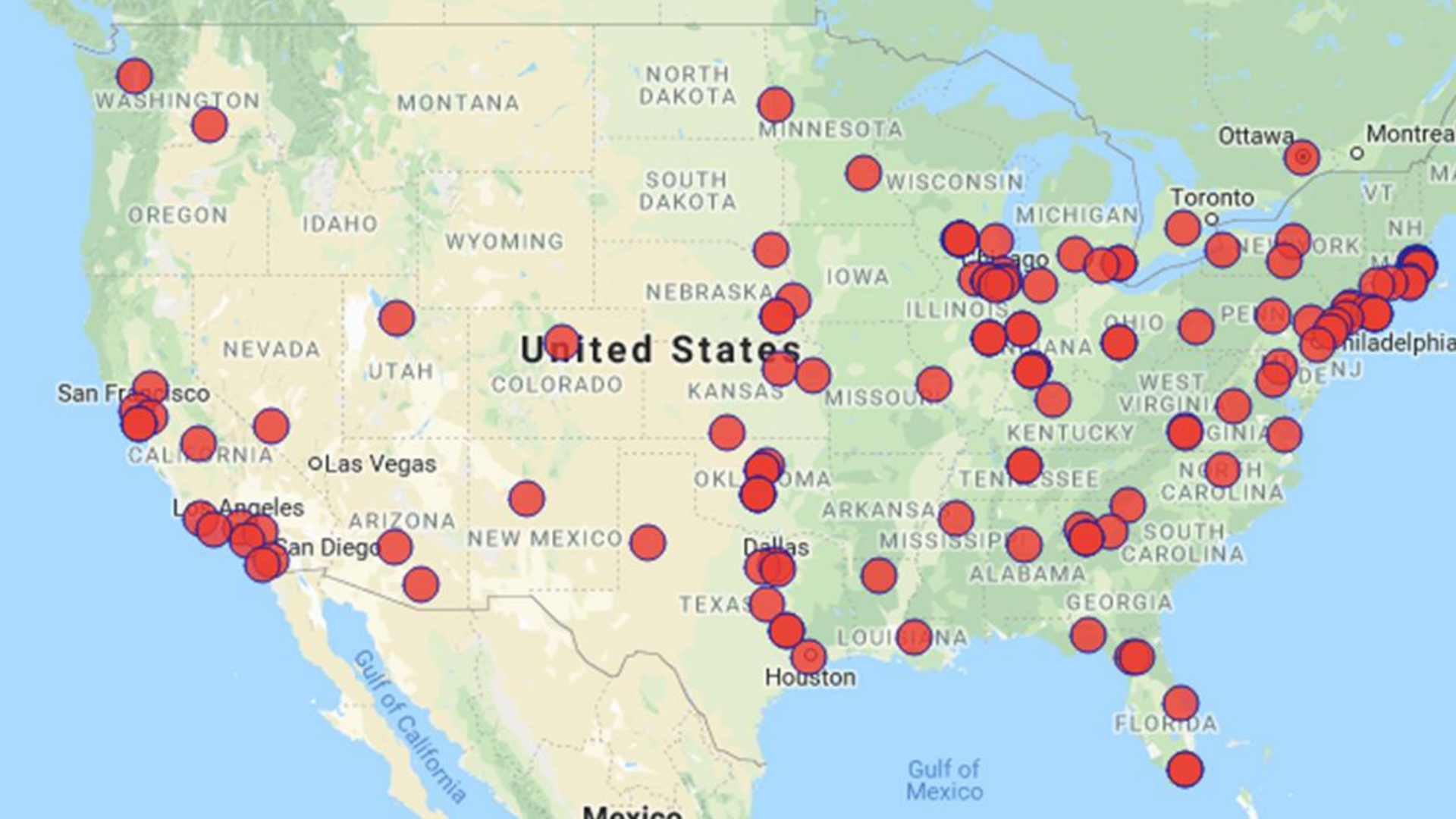
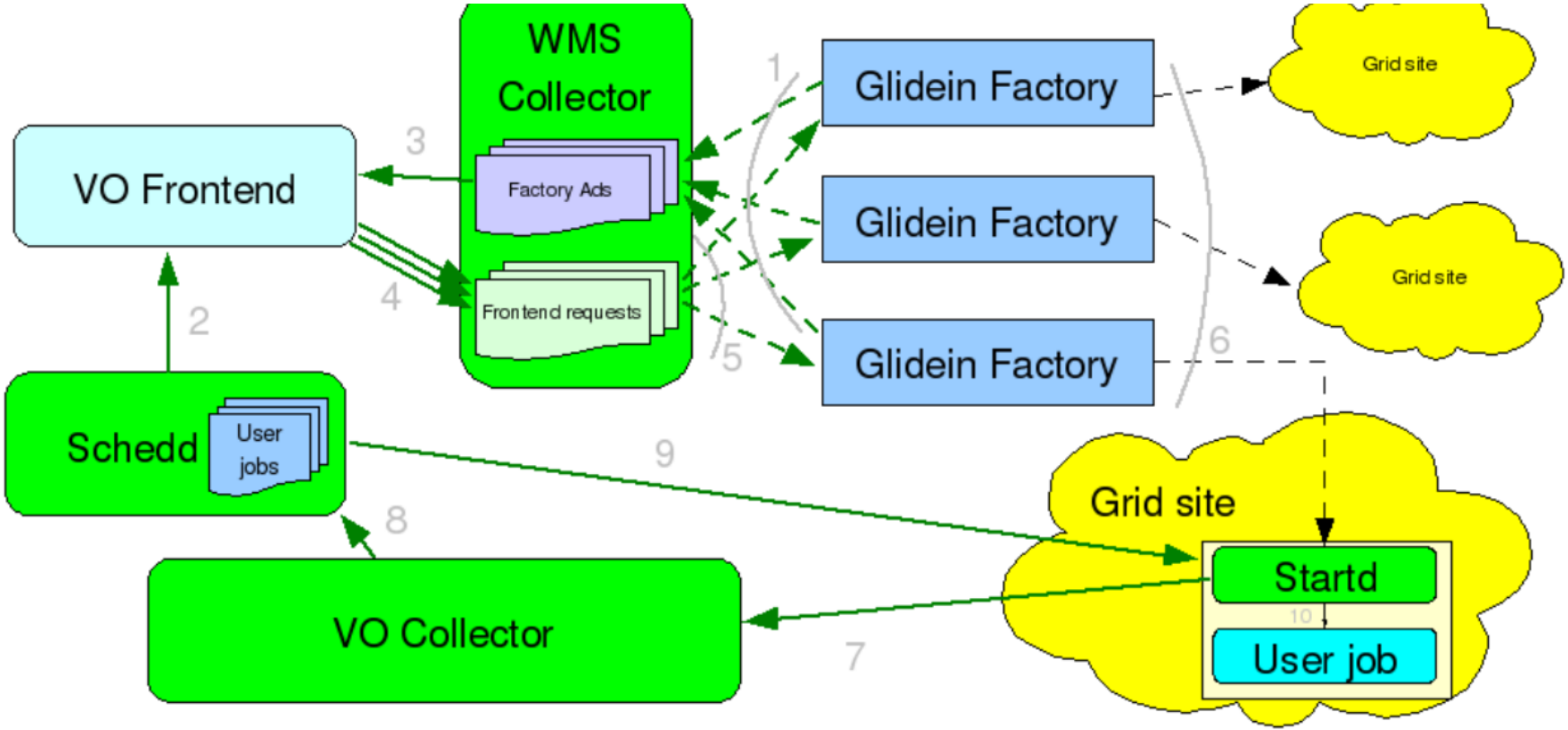
MicroArch

Nomen Numen

Greg Thain

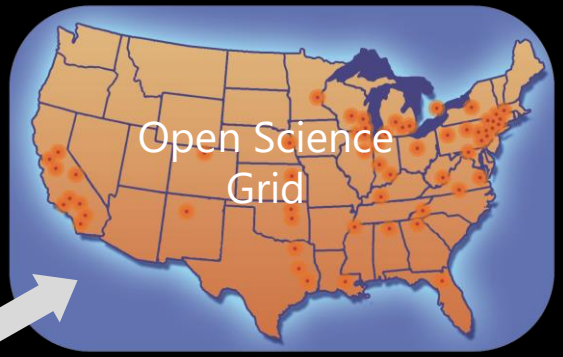
OS Pool

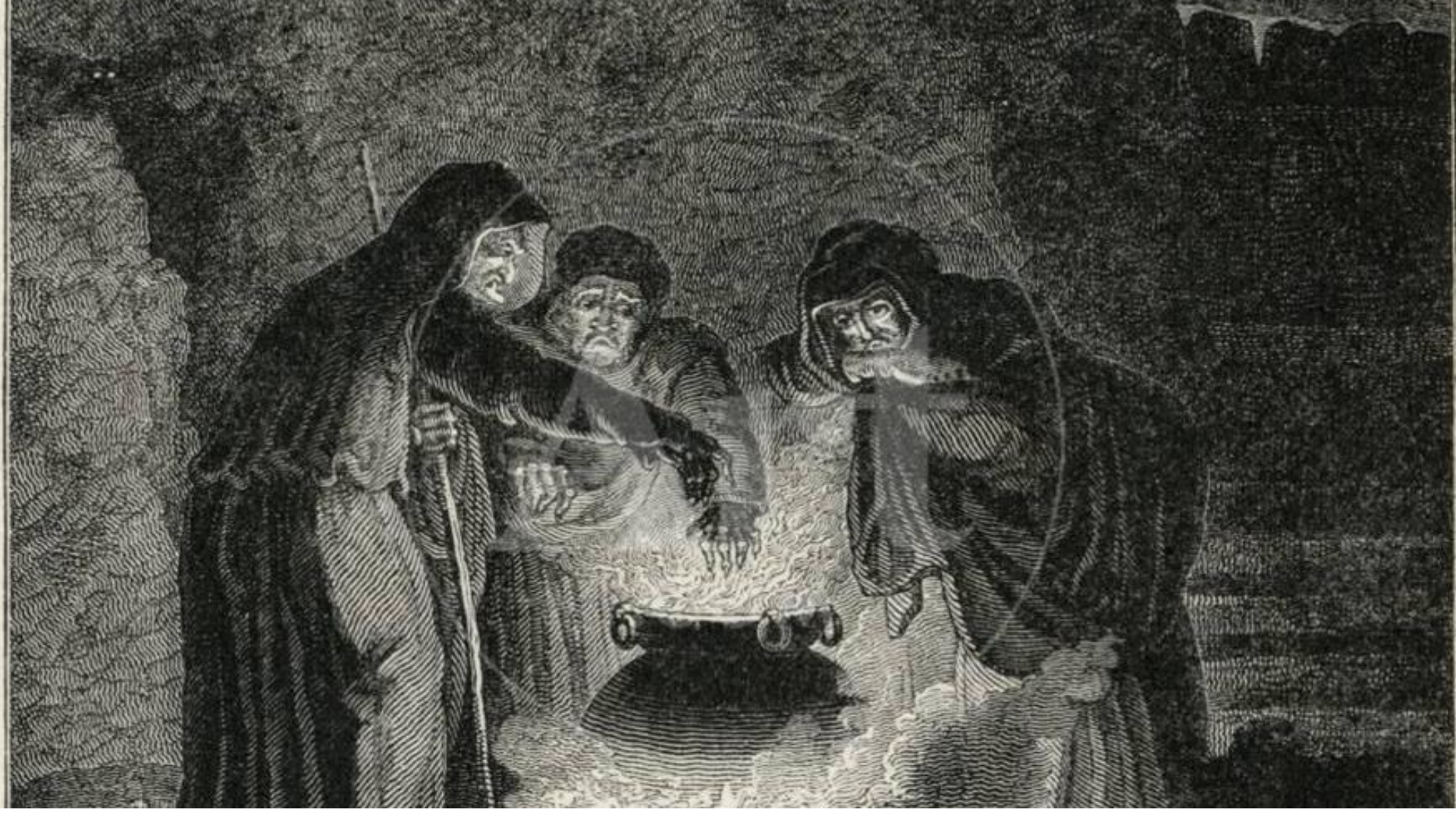

WASHINGTON
MONTANA
NORTH DAKOTA
MINNESOTA
Ottawa
Montrea
SOUTH DAKOTA
WISCONSIN
Toronto
OREGON
IDAHO
WYOMING
MICHIGAN
VT
NH
IOWA
NEBRASKA
ILLINOIS
OHIO
NEVADA
UTAH
United States
COLORADO
KANSAS
MISSOURI
WEST VIRGINIA
KENTUCKY
San Francisco
CALIFORNIA
Las Vegas
OKLAHOMA
TENNESSEE
NORTH CAROLINA
Los Angeles
ARIZONA
ARKANSAS
San Diego
NEW MEXICO
Dallas
MISSISSIPPI
SOUTH CAROLINA
ALABAMA
TEXAS
GEORGIA
LOUISIANA
Houston
Gulf of California
FLORIDA
Gulf of Mexico
Mexico


WMS
Collector
Factory Ads
Frontend requests
VO Frontend
Schedd
User
jobs
VO Collector
Glidein Factory
Glidein Factory
Glidein Factory
Grid site
Grid site
Grid site
Startd
User job
1
2
3
4
5
6
7
8
9
10

Campus Clusters

Local
pool

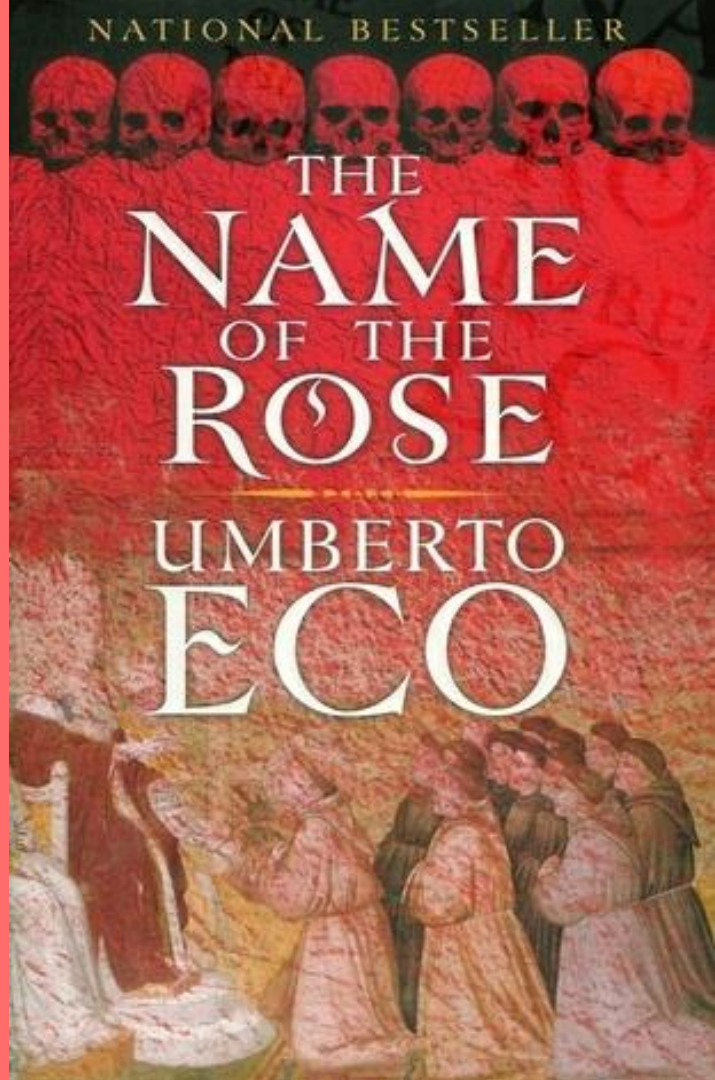


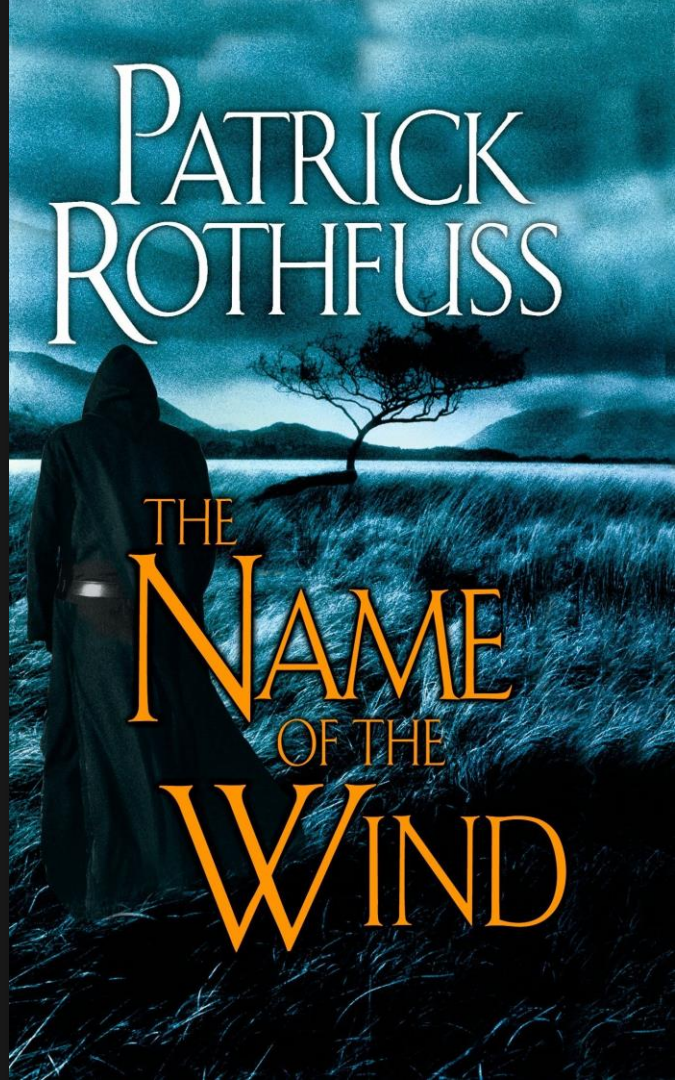



Speak friend and enter

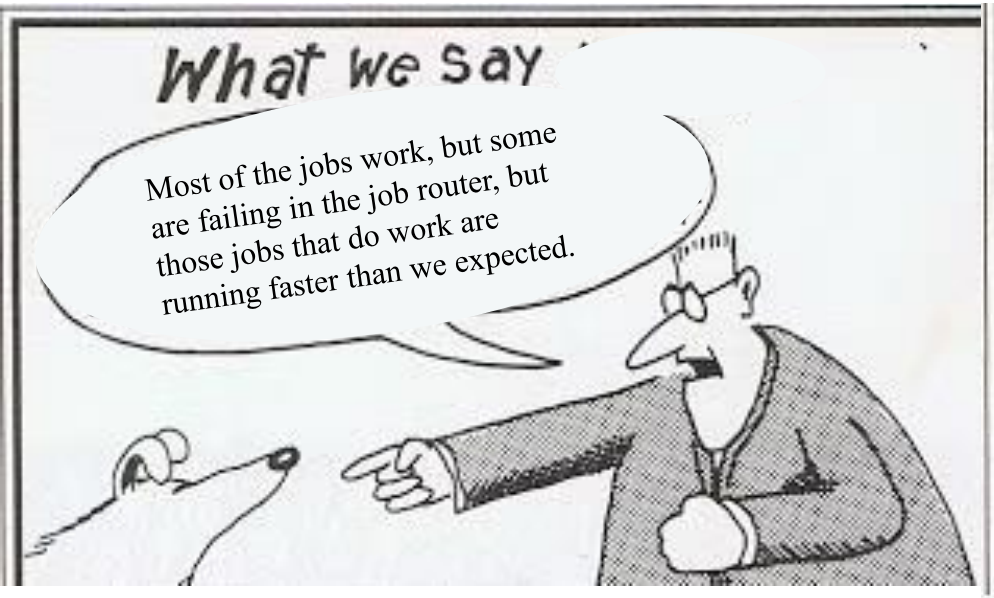
The
beginning of
Wisdom
is to call things by their proper
name.

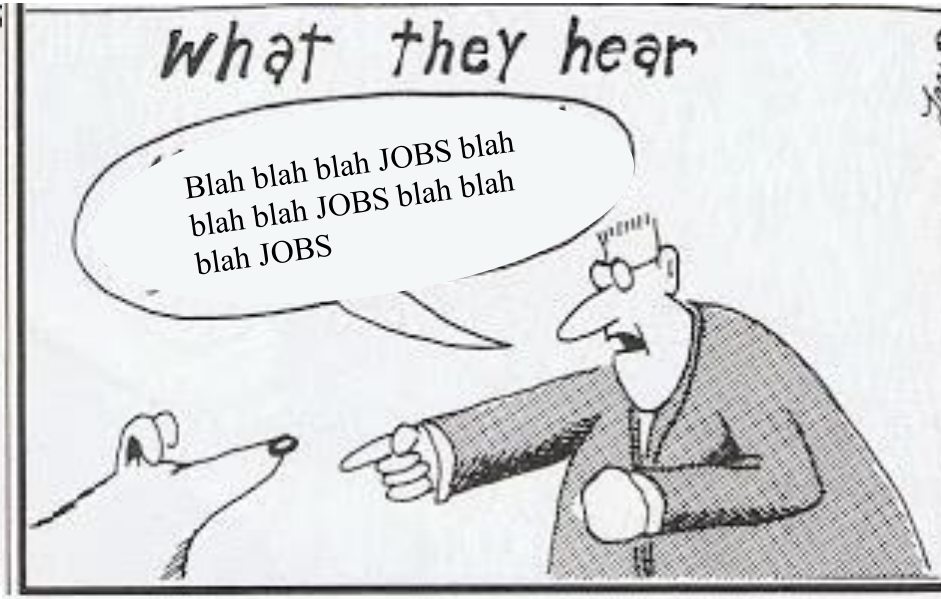
-- Confucius


NATIONAL BESTSELLER
THE
NAME
OF THE
ROSE
UMBERTO
ECO


PATRICK
ROTHFUSS
THE
NAME
OF THE
WIND

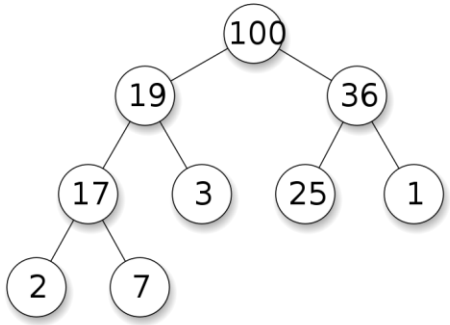
The Power of Clarity



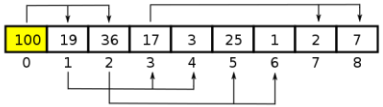


The Power of Metaphor

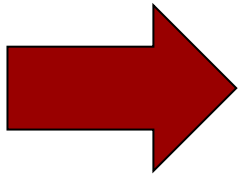
Tree representation



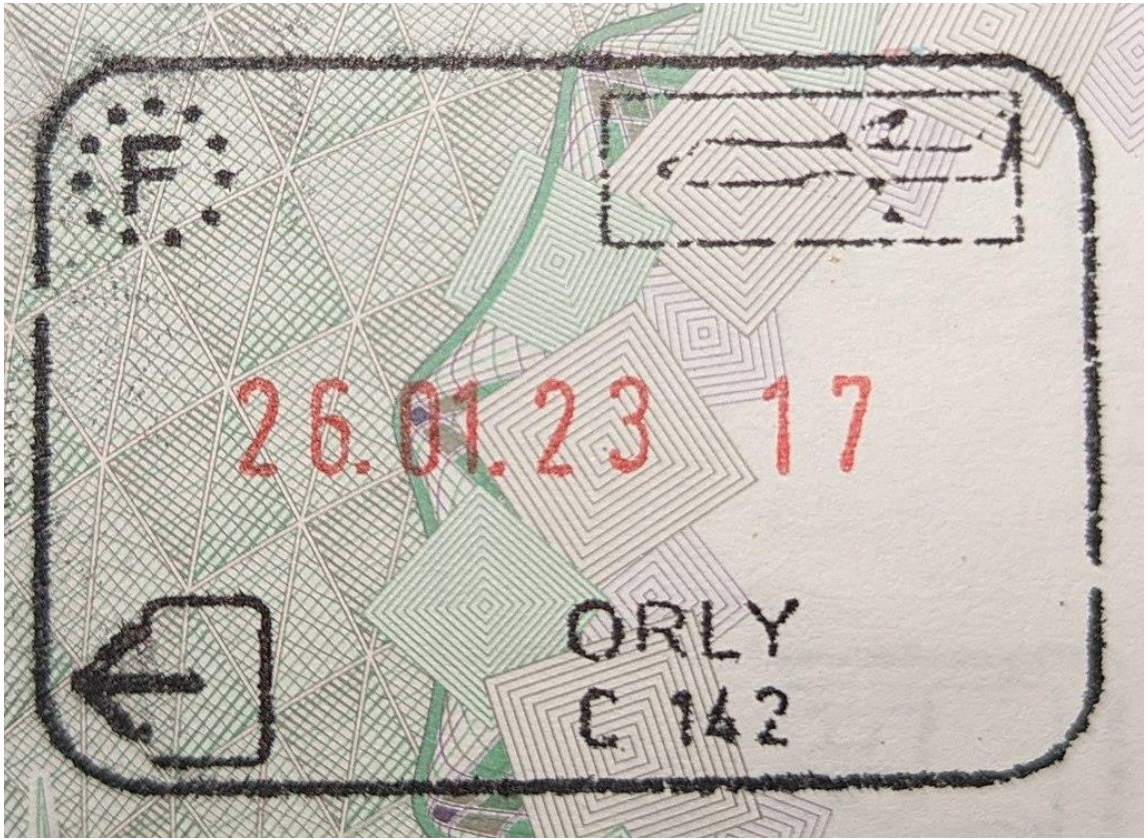
Array representation



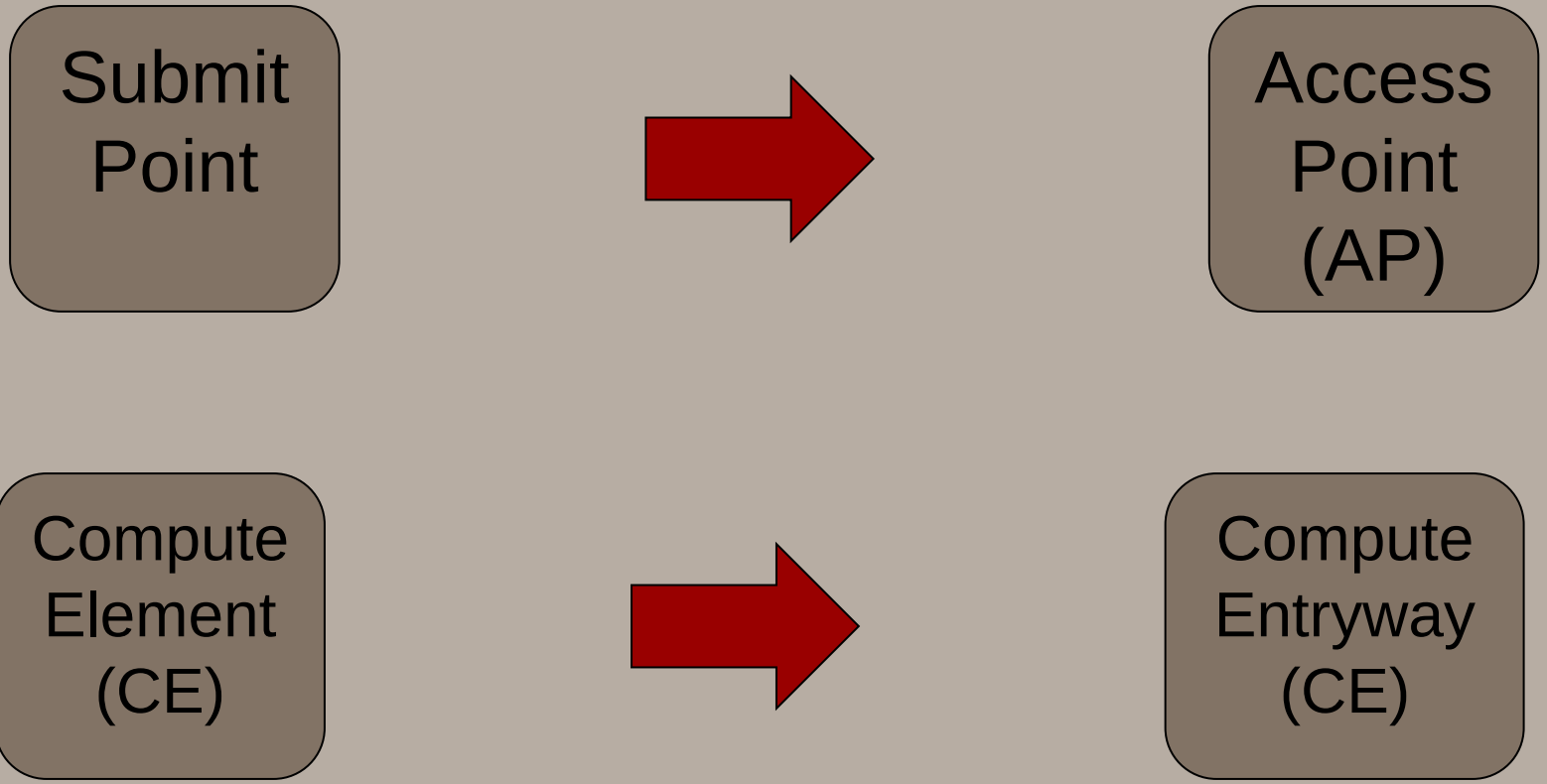
Heap

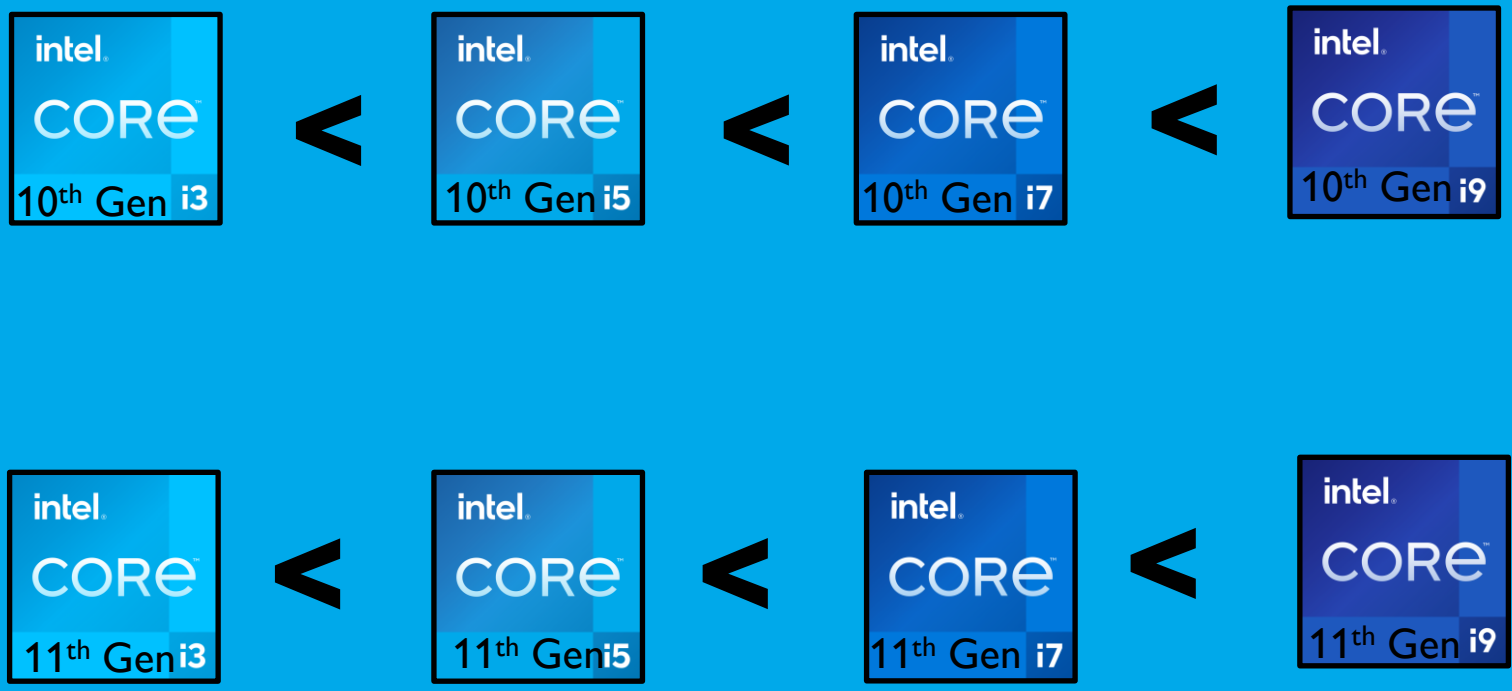


The Power of Generation



The Best Time to Plant a Tree




intel CORE 10th Gen i3
<
intel CORE 10th Gen i5
<
intel CORE 10th Gen i7
<
intel CORE 10th Gen i9
intel CORE 11th Gen i3
<
intel CORE 11th Gen i5
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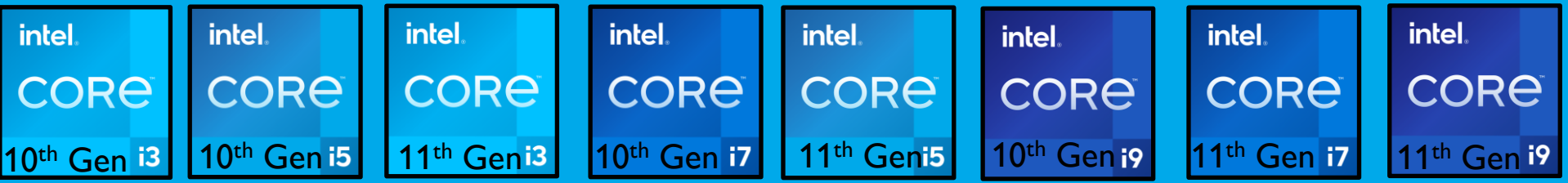
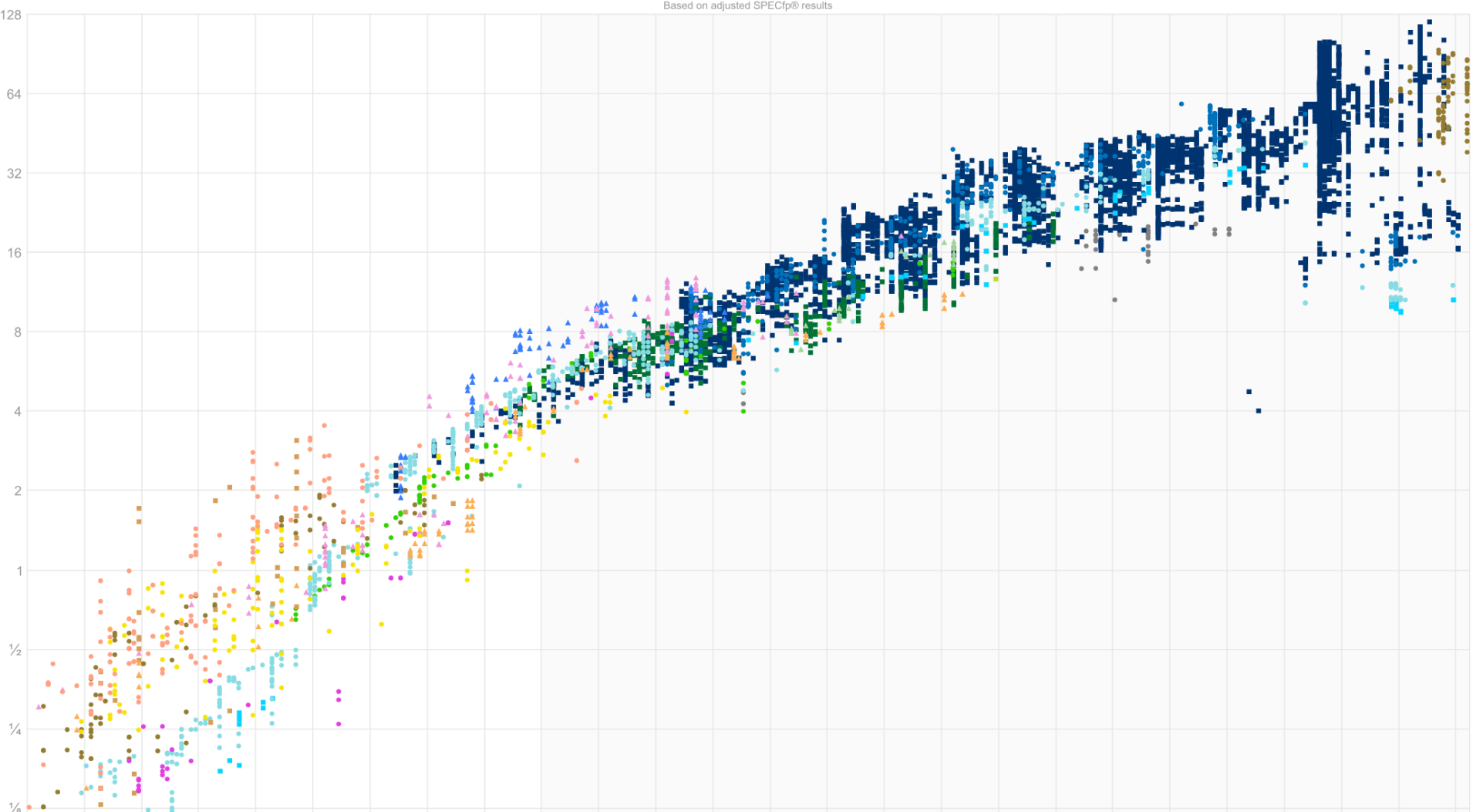
intel CORE 11th Gen i7
<
intel CORE 11th Gen i9


intel
CORE
10th Gen i3
intel
CORE
10th Gen i5
intel
CORE
11th Gen i3
intel
CORE
10th Gen i7
intel
CORE
11th Gen i5
intel
CORE
10th Gen i9
intel
CORE
11th Gen i7
intel
CORE
11th Gen i9

Single-Threaded Floating-Point Performance

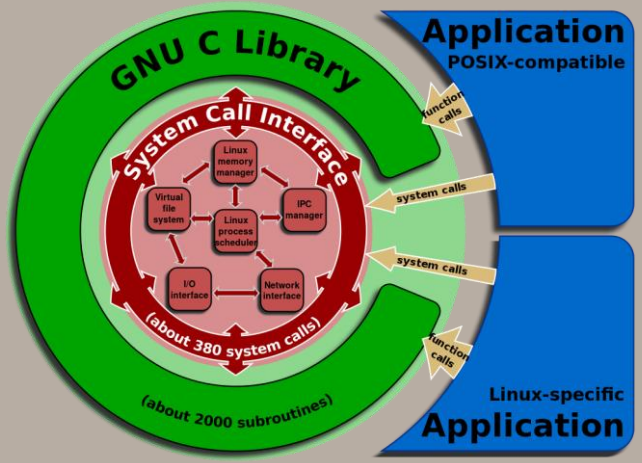
Based on adjusted SPECfp® results

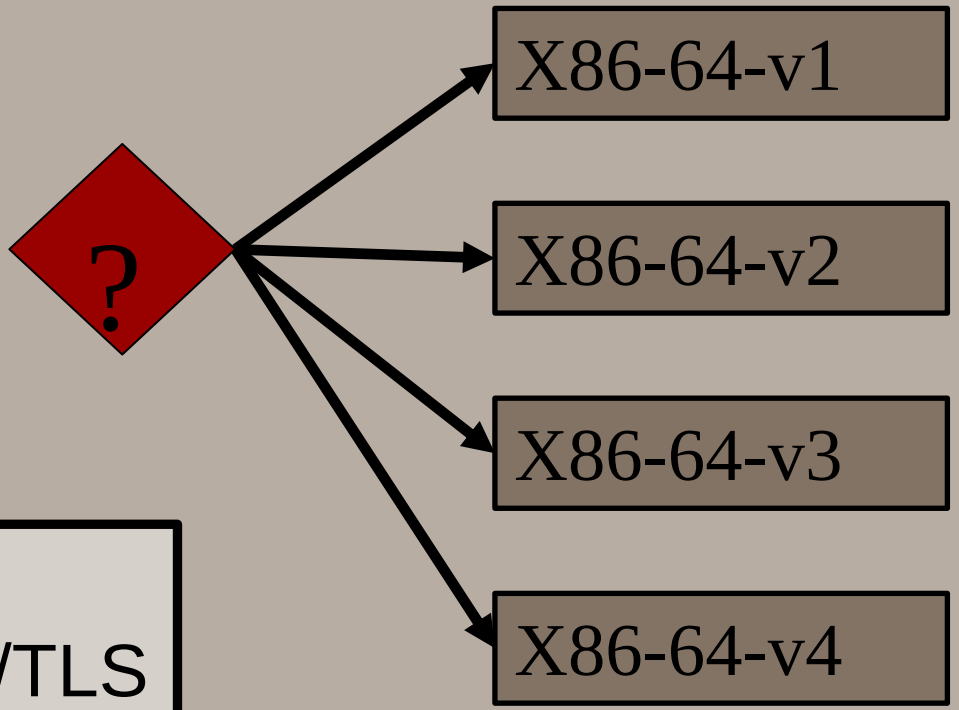


Year	Insn	Family	Description
2001	SSE2	P6	Attempt to replace the original MMX instructions; wider XMM registers offer better performance
2004	SSE3	Core	Streaming SIMD Extensions 3; new instructions to operate on multiple values in the same register
2006	SSSE3	Core	Supplemental Streaming SIMD Extensions 3; additional instructions for working with packed integers
2007	SSE4.1	Penryn	Streaming SIMD Extensions 4.1; initial set of instructions for manipulating media data
2007	SSE4a	K10	4 SIMD instructions, not related to 4.1/4.2
2007	ABM	K10	Advanced Bit Manipulation; bit counting instructions
2008	SSE4.2	Nehalem	Streaming SIMD Extensions 4.2; second set of instructions for manipulating media data
2007	SSE5		Proposed by AMD in 2007 but was never implemented
2008	SSE4		Streaming SIMD Extensions 4; Another name for SSE4.1 + SSE4.2

2013	FMA3	Haswell	3-operands fused multiply-add
2013	TSX	Haswell	Transactional Synchronization Extensions; adds transactional memory support
2013	AVX2	Haswell	Advanced Vector Extensions; additional instructions
2014	ADX	Broadwell	Multi-Precision Add-Carry Instruction extension
2014	RdRand	Broadwell	Part of Secure Key Technology extension (RdRand, RDSEED)
2014	PREFETCH	Broadwell	PREFETCH instructions (previously part of 3DNow!)
2015	AVX-512	Airmont	512 bit register operations
2015	MPX	Skylake	Memory Protection Extensions
2015	SGX	Skylake	Software Guard Extensions
2016	SHA	Goldmont	SHA Extensions
2017	SME	Zen	Secure Memory Extensions
2019	TME	Ice Lake	Total Memory Encryption

The hard way…

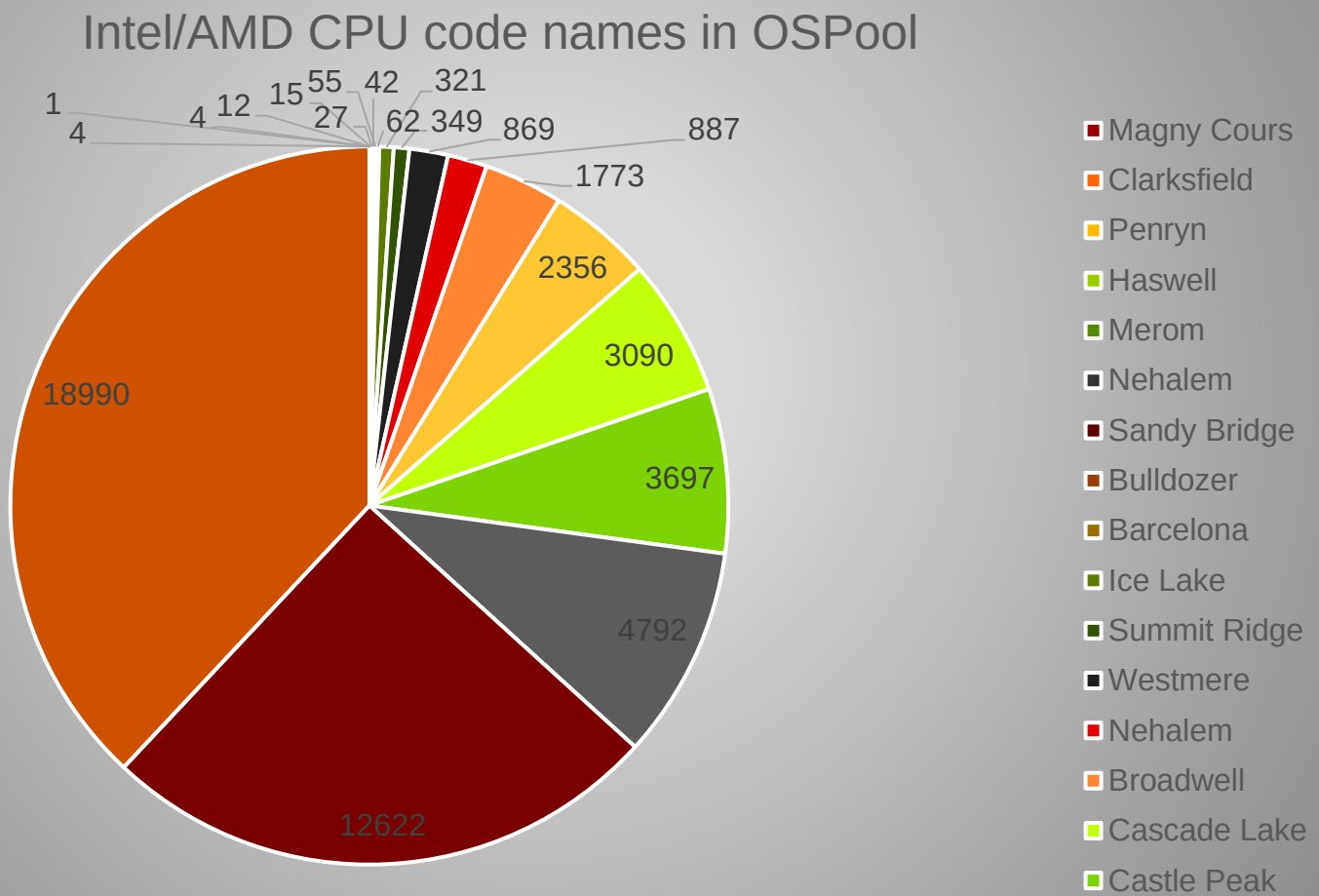




OpenSSL

Cryptography and SSL/TLS Toolkit

Cores in OSPool by codename



Why is this a problem?

1) If (CPU job built for) > CPU

→ Crash with SIGILL

2) if (CPU job built for) < CPU

→ Run slower than possible

Intel + RedHat to the rescue!

[llvm-dev] New x86-64 micro-architecture levels

Florian Weimer via llvm-dev llvm-dev at lists.llvm.org
Fri Jul 10 10:30:09 PDT 2020

- Previous message: [llvm-dev] [LNT] Build bot problems due to Python dependencies
- Next message: [llvm-dev] New x86-64 micro-architecture levels
- **Messages sorted by:** [date] [thread] [subject] [author]

```
Most Linux distributions still compile against the original x86-64
baseline that was based on the AMD K8 (minus the 3DNow! parts, for Intel
EM64T compatibility).

There has been an attempt to use the existing AT_PLATFORM-based loading
mechanism in the glibc dynamic linker to enable a selection of optimized
libraries.  But the general selection mechanism in glibc is problematic:

  hwcaps subdirectory selection in the dynamic loader
  <https://sourceware.org/pipermail/libc-alpha/2020-May/113757.html>

We also have the problem that the glibc version of "haswell" is distinct
from GCC's -march=haswell (and presumably other compilers):

  Definition of "haswell" platform is inconsistent with GCC
  <https://sourceware.org/bugzilla/show_bug.cgi?id=24080>

And that the selection criteria are not what people expect:
```

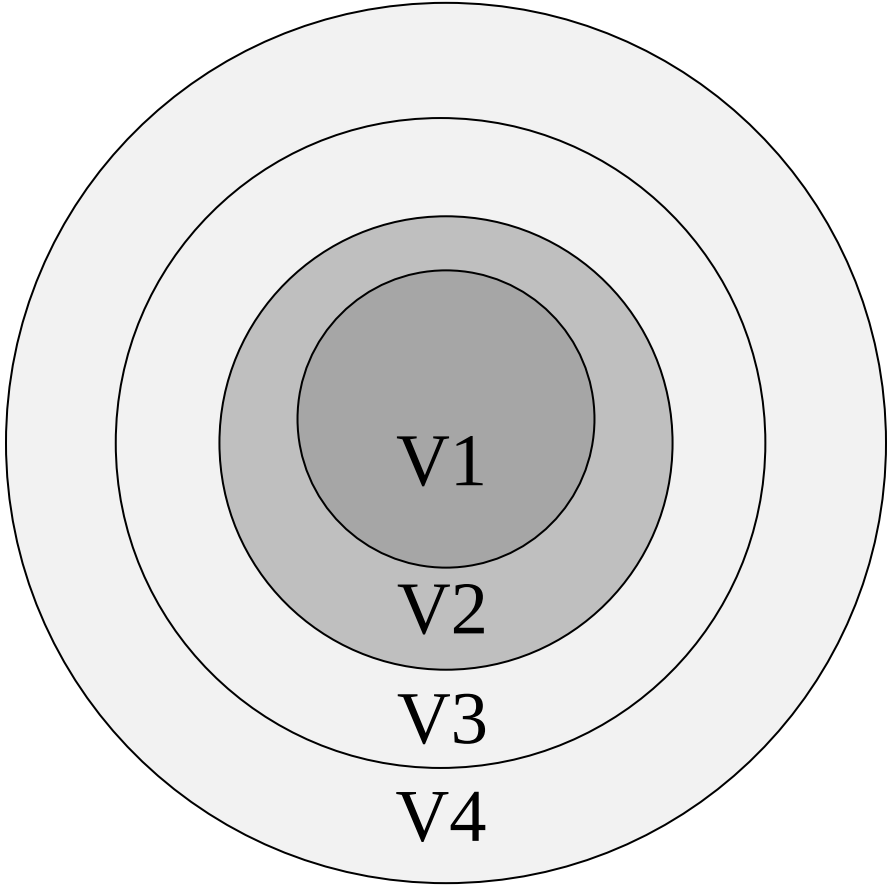
Microarch: four levels

Haswell	Core	Saphire Rapids	Nehalem
Broadwell	Core 2	Rapids Lake	Westmere
Skylake	Penryn	Granite Rapids	Sandy Bridge
Cascade Lake	Wolfdale	Willow Cove	Ivy Bridge
…	…	…	…

Microarch: four levels

x86_64-v1	x86_64-v2	x86_64-v3	x86_64-v4
Core	Nehalem	Haswell	Saphire Rapids
Core 2	Westmere	Broadwell	Rapids Lake
Penryn	Sandy Bridge	Skylake	Granite Rapids
Wolfdale	Ivy Bridge	Cascade Lake	Willow Cove
…	…	…	…

Microarch: strict hierarchy



Compilers and microarch

```
$ gcc -march=x86-64-v3 source.cpp


$ file a.out
a.out: ELF 64-bit LSB shared object, x86-64, version 1
(SYSV), dynamically linked, interpreter /lib64/ld-
linux-x86-64.so.2, for GNU/Linux 3.2.0
```

HTCSS Support for microarch

```
$ condor_status -af Name MicroArch
slot3@build4000.chtc.wisc.edu x86_64-v3
slot1@e2007.chtc.wisc.edu x86_64-v4
slot1@e2008.chtc.wisc.edu x86_64-v4
slot1@e3001.chtc.wisc.edu x86_64-v1
```

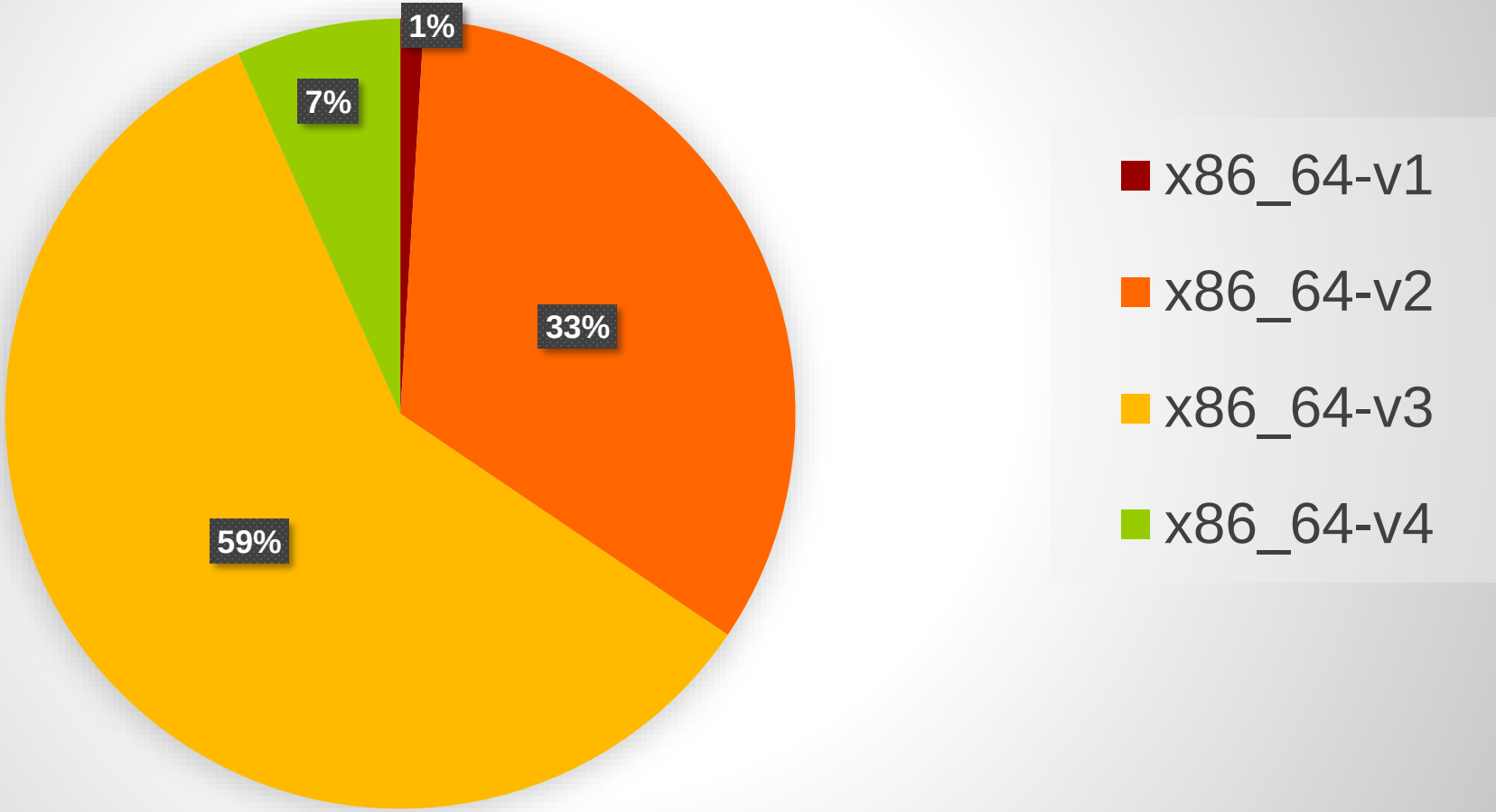
HTCSS Support for microarch

```
$ condor_status -const \
    'microarch > "x86_64-v2" '
slot3@build4000.chtc.wisc.edu x86_64-v3
slot1@e2007.chtc.wisc.edu x86_64-v4
slot1@e2008.chtc.wisc.edu x86_64-v4
```

HTCSS Support for microarch

```
Executable = calculate.exe
Requirements = microarch > "x86_64-v2"
Request_memory = 1Gb
Request_disk   = 100Mb
Request_cpus   = 2
queue
```

Microarch in OSPool



More uArch problems

AES acceleration in HTCondor v10.0

Encryption FREE for "modern CPUs"…

Future Wishlist

Automatic detection of microarch in binaries

Microarch specific packaging?

Recap

- Names have power
- MicroArch
  - Learn it
  - Use it
  - Teach it
- Invest in good naming