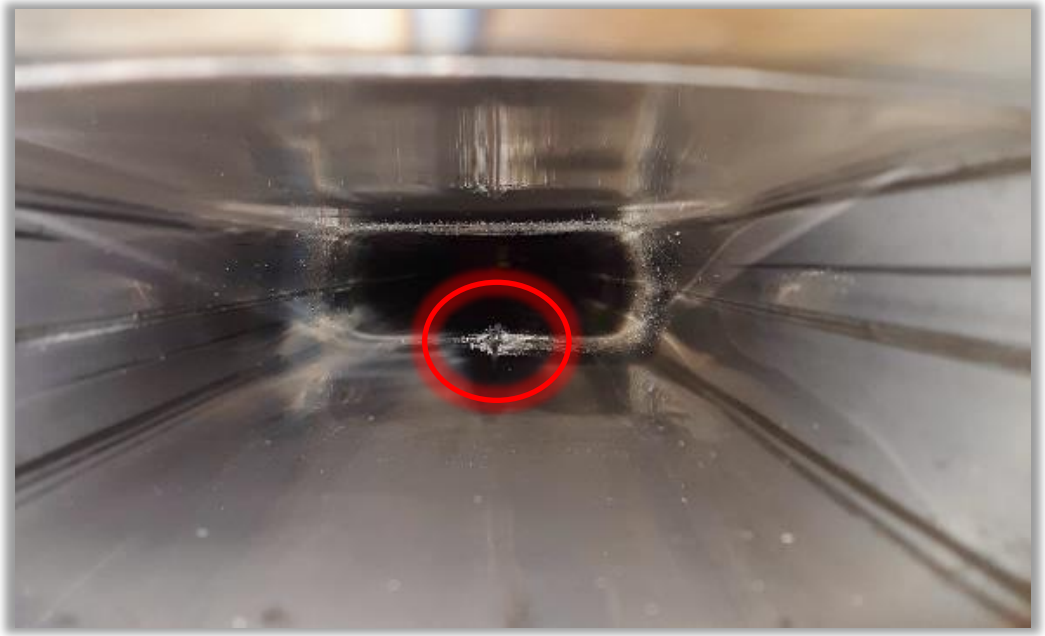
SPS dI/dt update & initial experience

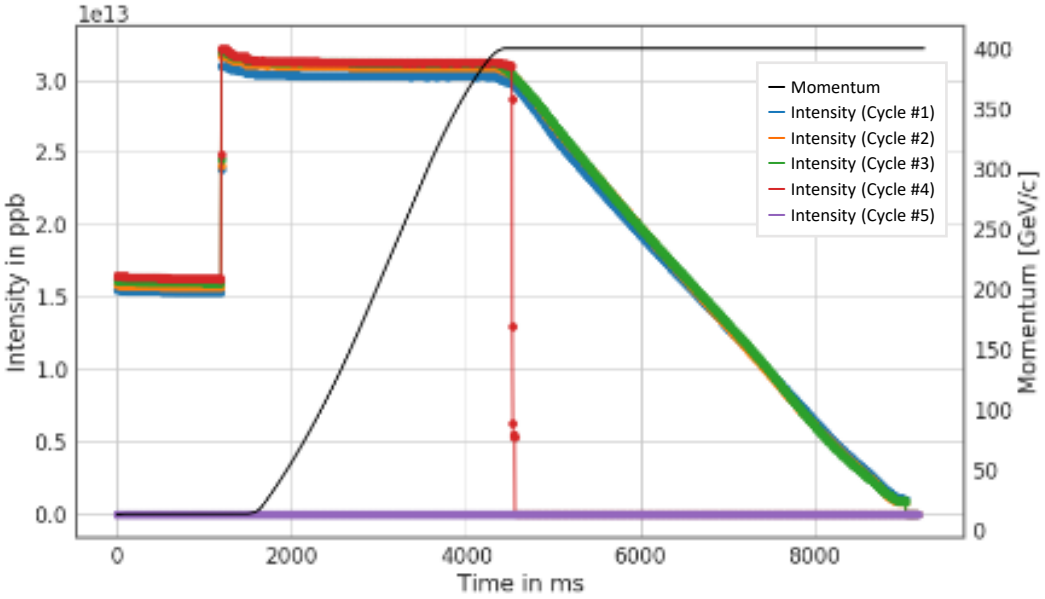
T. Levens, K. Li, S. Thoulet, S. Bart Pedersen

Introduction

- Incident in August 2018:
  - Fast beam loss during slow extraction due to tune crossing ½ integer resonance.
  - Resulting in leak in MBB in 331.
    - 48 hours downtime due to magnet exchange + dose to personnel.



- Following this incident, and other "near misses", request from OP for additional interlocks to protect against fast losses:
  - ALPS BPM interlocks.
  - BLM software upgrade (faster response).
  - **dI/dt interlock.**



- Document SPS-B-ES-0005 describing the requirements.

Requirements (from SPS-B-ES-0005)

2.3 Resulting specifications for dI/dT interlock

The system should interlock on fast changes of the stored intensity in the ring. As such, the system will be rather robust and global; it will be independent of the location of losses in the machine, any specific optics or beam types.

From the past events, the minimum speed needed to resolve the above events is < 1ms! Ideally, different "integration times", i.e. <1ms and 10ms, are available. For each of the integration times, programmable "maximum intensity change" thresholds should be provided. Adequate settings to protect against the events above:

2 integration windows

Integration time	Total loss threshold	Average loss rate	Comments
1 ms	-3e11 p+	-3e11 p+/ms	ppm
10 ms	-1e12 p+	-1e11 p+/ms	ppm

The interlock should have one input to the BIS, which will be maskable. The interlock should trigger whenever the programmed thresholds are crossed.

As means of post-mortem diagnostics, a dedicated buffer should record and be used to publish the last ~10000 turns (~230 ms) in case of an interlock before the beam dump.

BCTDC specifications

BCTDC

BCTDC 51454 & BCTDC 51456

Range	SF [mA/V]	FS [mA]	SF [charges/V]	FS [charges]
1	139	695	2.00E+13	1.00E+14
2	13.9	69.5	2.00E+12	1.00E+13
3	1.39	6.95	2.00E+11	1.00E+12
4	0.139	0.695	2.00E+10	1.00E+11

Band width: full BW: 10kHz (range 1 and 2)
FESA aqn: 200Hz

Noise peak-peak: FESA –Timber: 2E9 ch
full BW: 1 to 2E11 ch (estimation)

The noise level will be revaluated after monitors relocation

dI/dt

thresholds:

1. 3E11 ch in 1ms
2. 1E12 ch in 10ms

Range 1 to cover the whole dynamic

3E11 ch/ms measured on range 1, 0.3% FS !

Corresponds to 15mV with a BW > 1kHz
Quite challenging to measure on surface !

P.Odier

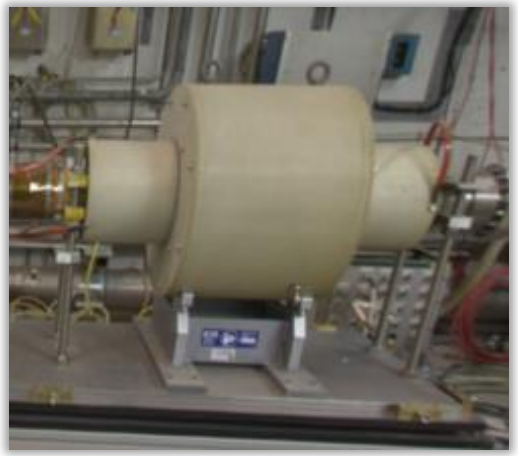
SPS dI/dt interlock

…as presented at 203rd MPP

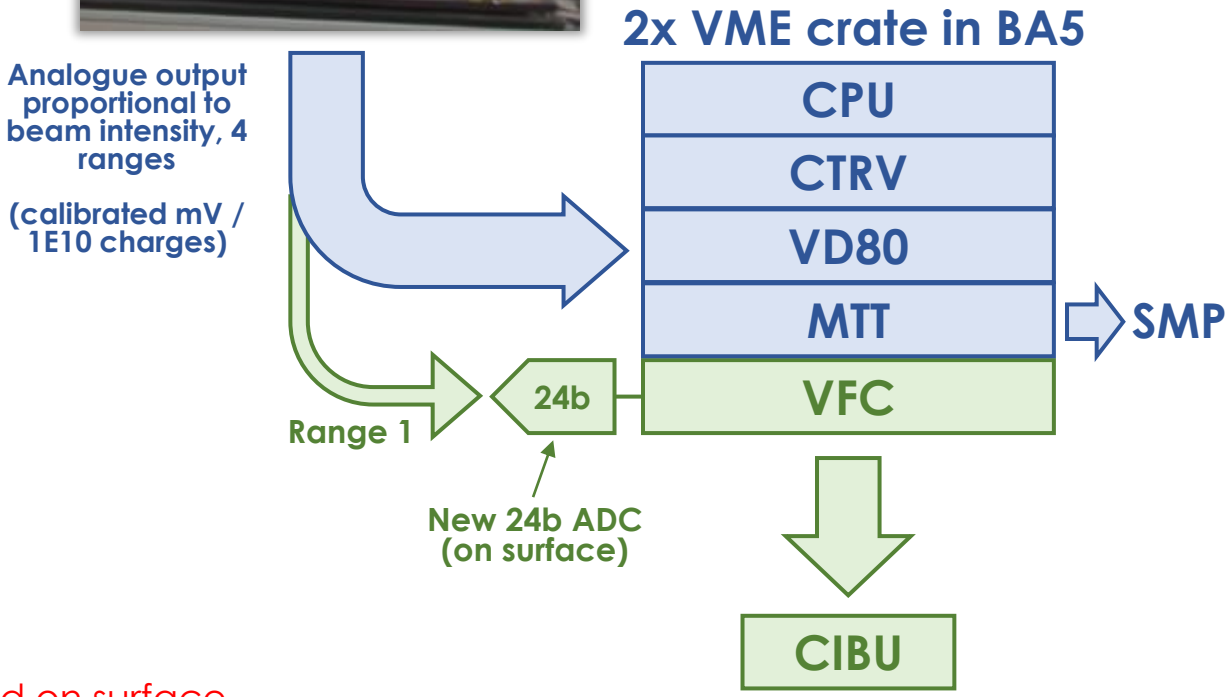
Integration time	Total loss threshold	Average loss rate
~~1 ms~~ 2 ms	3e11 to 5e11 p+	3e11 to 5e11 p+/ms
10 ms	1e12 p+	1e11 p+/ms

- Note: must be able to detect losses during slow extraction (unbunched beam) → DCBCTs
- Propose to use LSS5 DCBCT system
  - Used for NA ions personnel protection
  - Redundant detectors & acquisition chain
- Existing VME acquisition is too slow (200sps)
- New development using BI-standard VFC
  - Can reuse many parts of LHC DIDT (HW+FW)
- Requested 3e11 p+ in 1 ms is at the limit of the detector analogue performance
  - Relaxed specification to be finalised
- Plan to install first prototype during LS2
  - Need some commissioning time afterwards!
  - ~~Longer term: looking into~~ 24-bit system (as in LHC) located on surface

2x DCBCT detector in LSS5

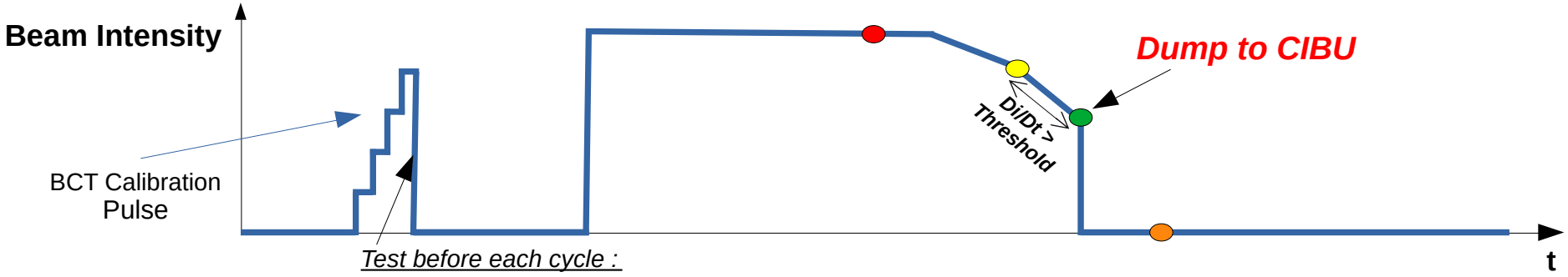


2x VME crate in BA5



dI/dt principle

* T1 = 0.1 ms, 24 Bits ADC Acquisition (10 kHz)
* T2 = 1 ms
* T3 = 10 ms

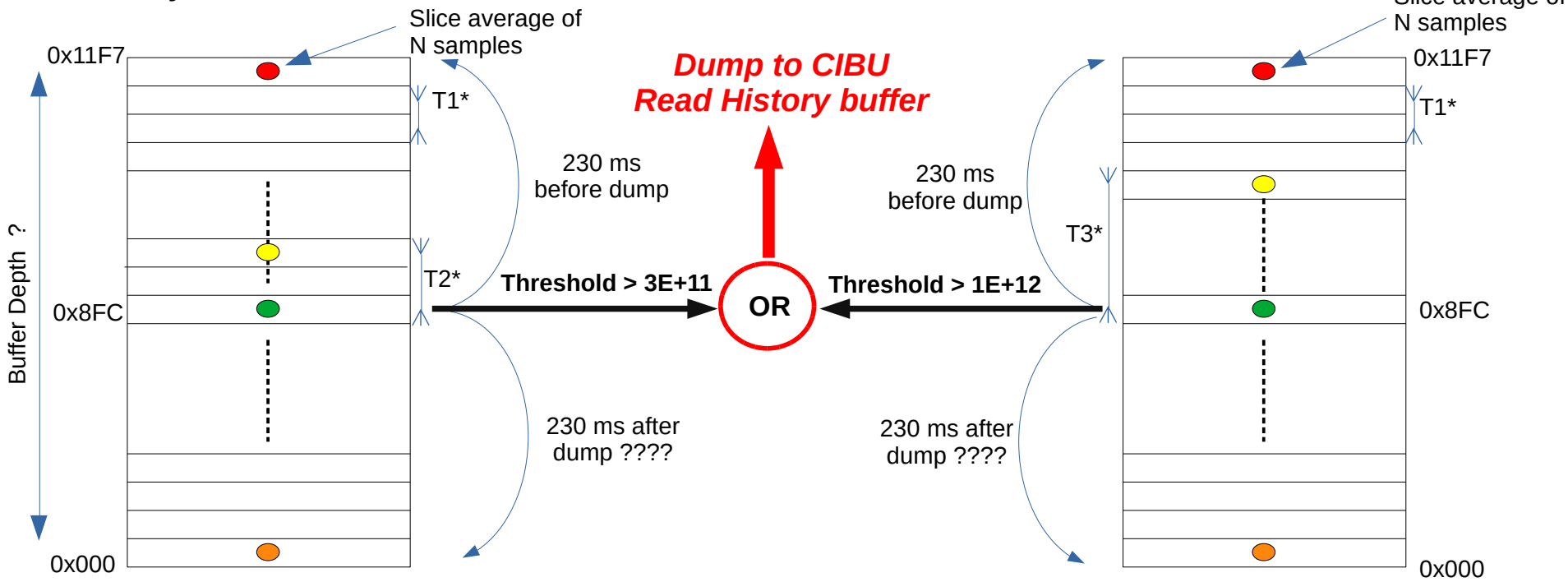


Set Threshold OK & Di/Dt > Threshold & … = NOT Dump to CIBU

Others cases = Dump to CIBU

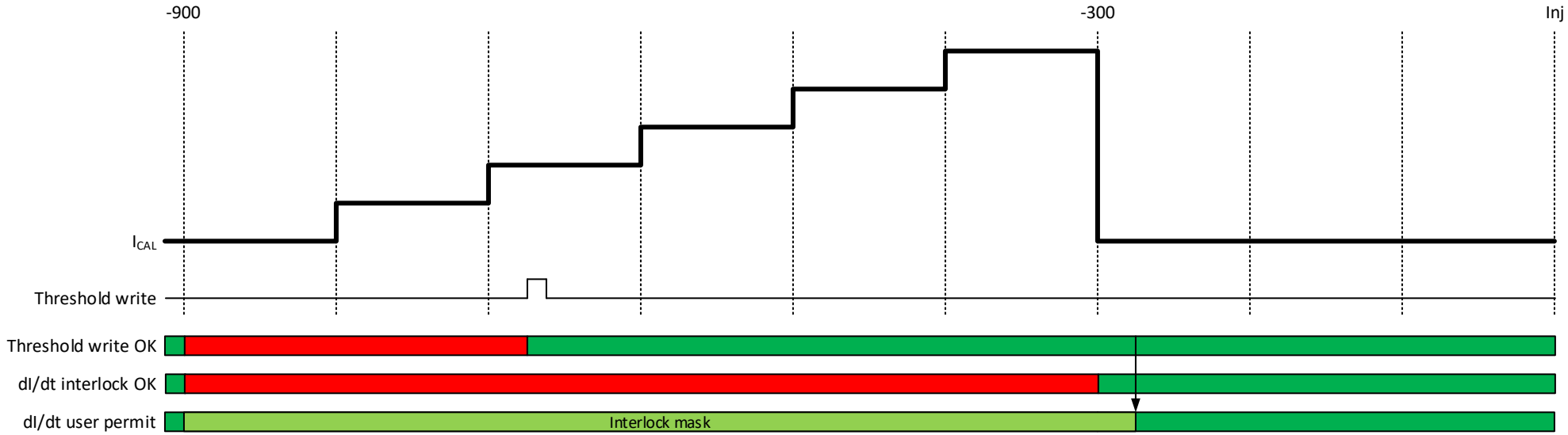
History buffer for Di/Dt 1ms

History buffer for Di/Dt 10ms



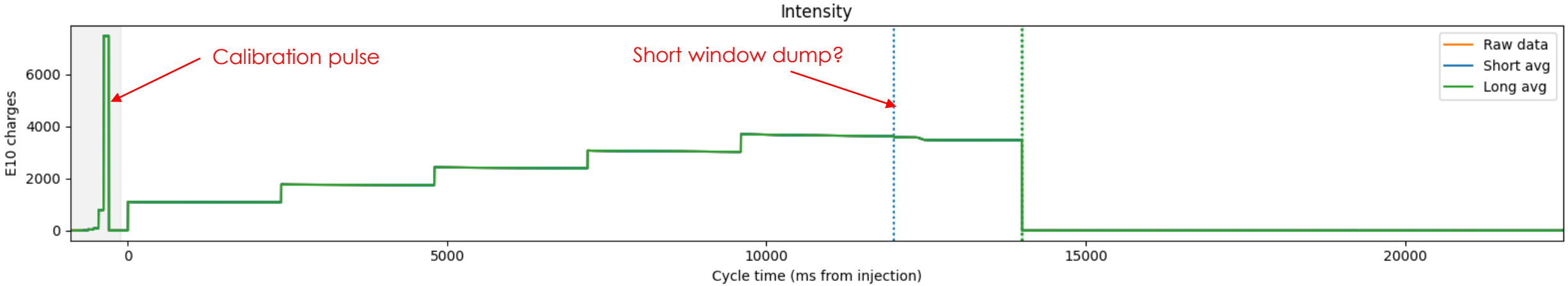
Self check principle

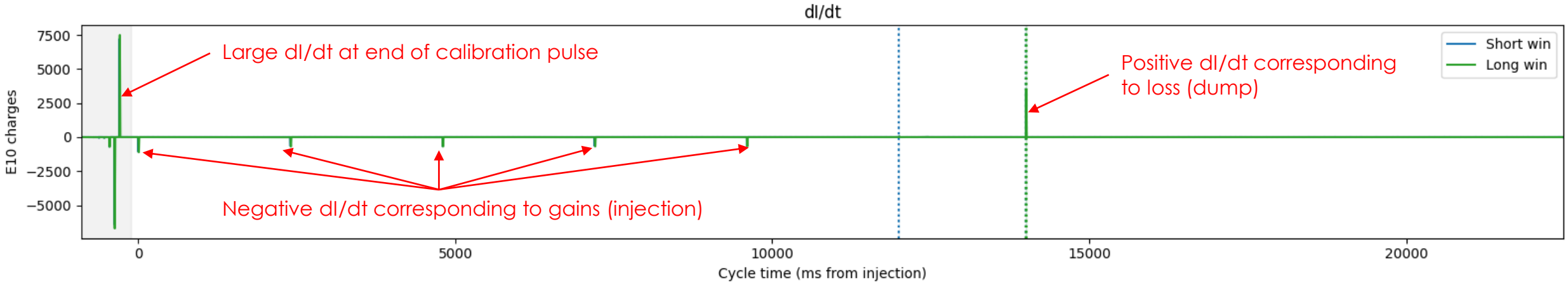
- BCTs have a self-check procedure launched 900ms before injection.
  - A multi-level current pulse is sent to the calibration winding of the BCT
  - At the end of the pulse there is a large dI/dt (~8e13)
- The dI/dt logic checks at the end of the 645ms interlock mask:
  - That both windows correctly dump on this large dI/dt
  - That the thresholds for both windows have been written
- If not the user permit will be removed before injection.
  - Avoids injection if there is an issue with the BCT or FESA has crashed.

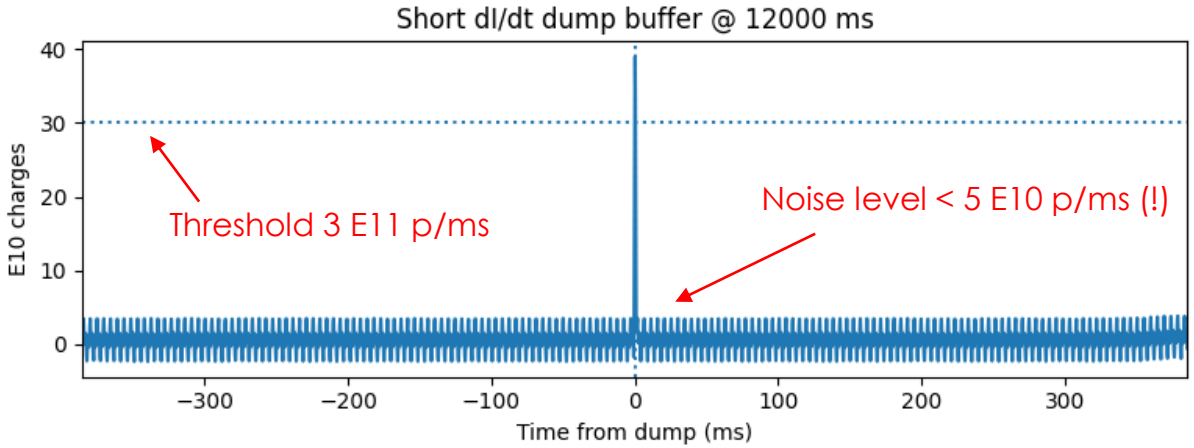


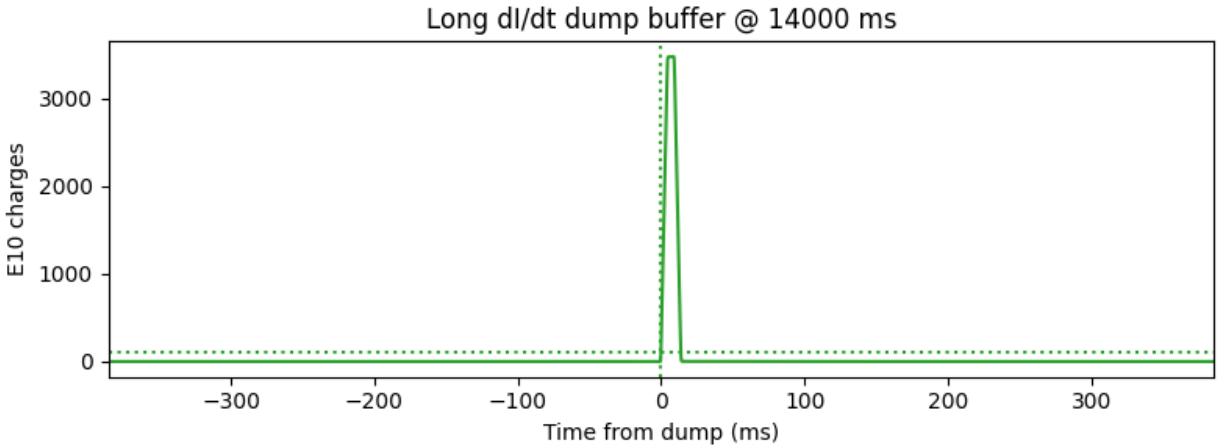
SPS dI/dt status

- 24-bit acquisition installed on BCTs in BA5 during LS2 for dI/dt with prototype gateware.
  - Due to other commissioning activities across all machines little time to test it during 2021.
- As presented at the 231st MPP meeting, new requirements added to send intensity to SMP.
  - Priority for development in 2022.
- New gateware with general acquisition, dI/dt and SMP features was deployed and tested by BI during second half of 2022.
- As of 2023 start-up this is considered as an operational system!
  - FESA class deployed and running.
  - Integration with LSA, PM, logging, etc.
  - Connected to SMP.
  - Connected to the BIS for dI/dt (but so far disabled).

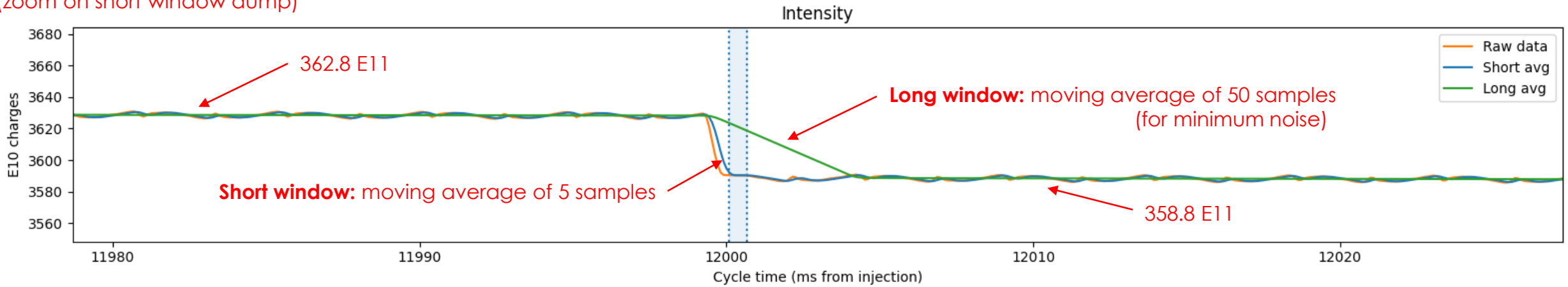

Intensity
Calibration pulse
Short window dump?
Raw data
Short avg
Long avg
E10 charges
Cycle time (ms from injection)

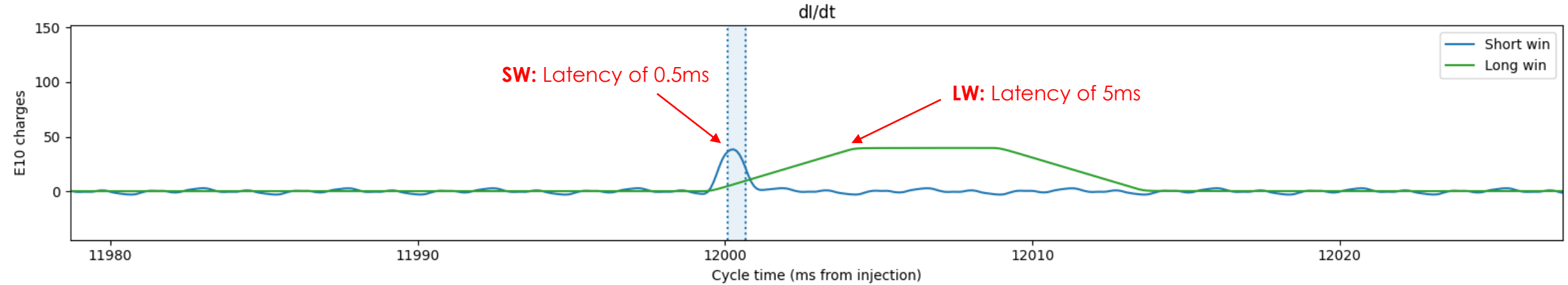

dI/dt
Large dI/dt at end of calibration pulse
Positive dI/dt corresponding to loss (dump)
Negative dI/dt corresponding to gains (injection)
Short win
Long win
E10 charges
Cycle time (ms from injection)

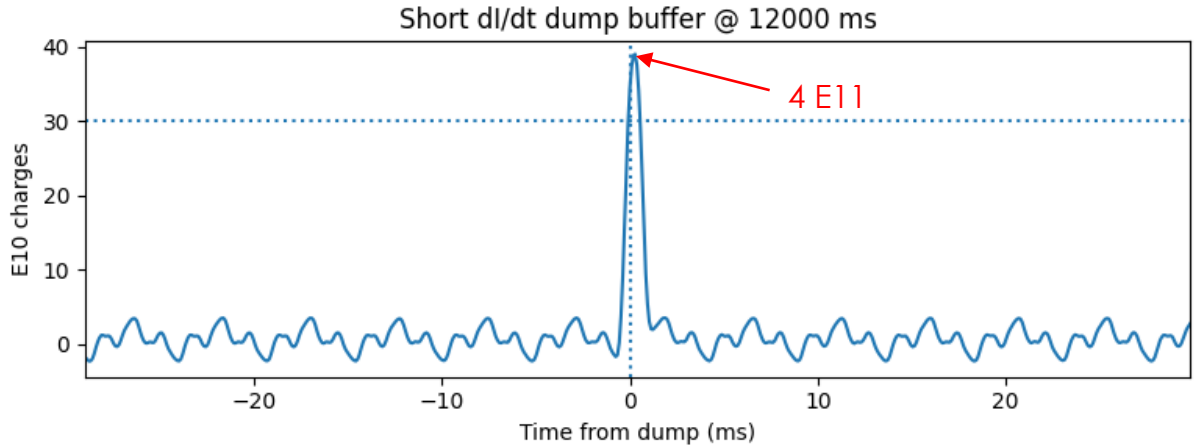

Short dI/dt dump buffer @ 12000 ms
Threshold 3 E11 p/ms
Noise level < 5 E10 p/ms (!)
E10 charges
Time from dump (ms)

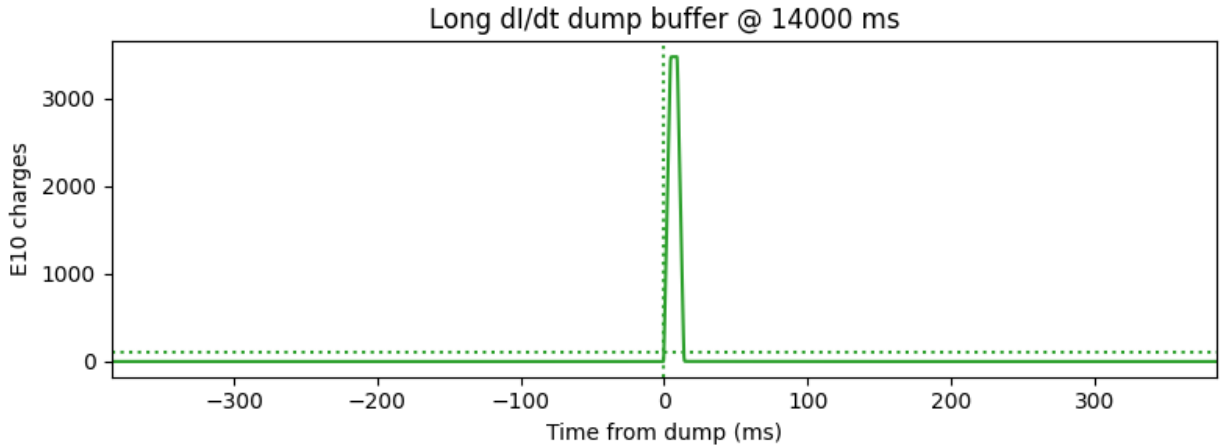

Long dI/dt dump buffer @ 14000 ms
E10 charges
Time from dump (ms)

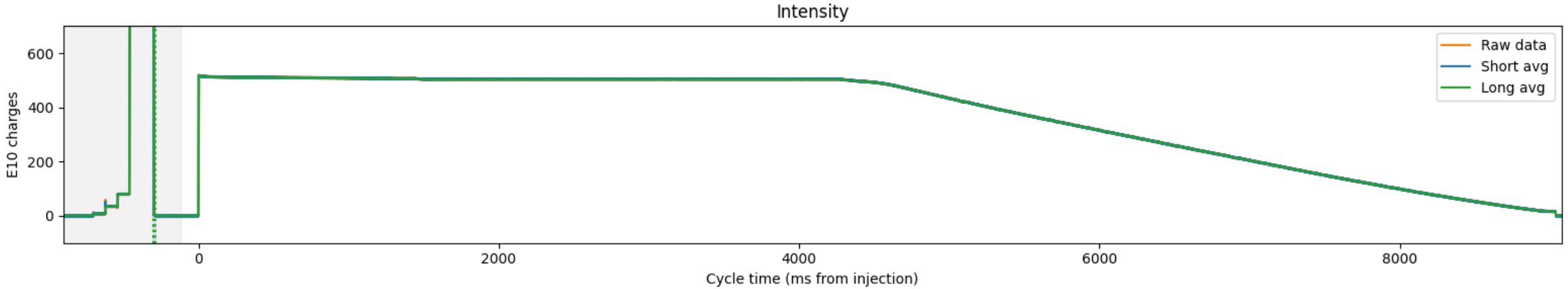
(zoom on short window dump)

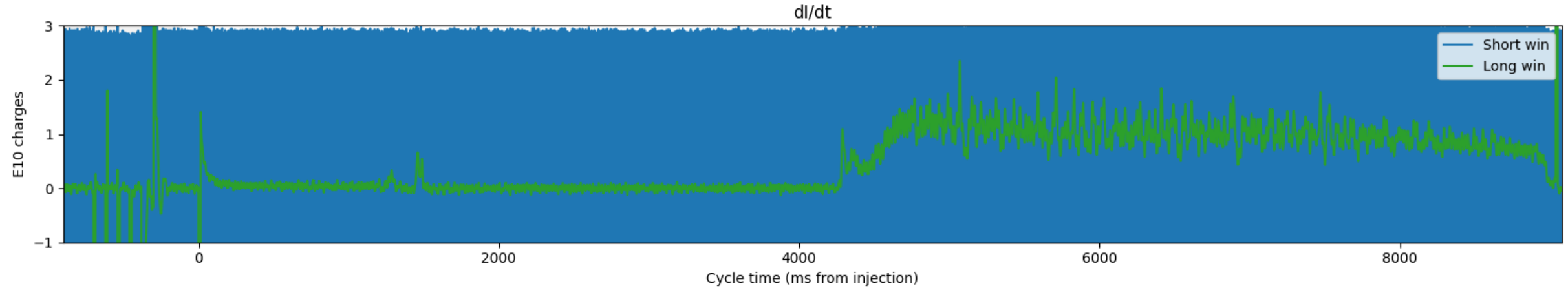


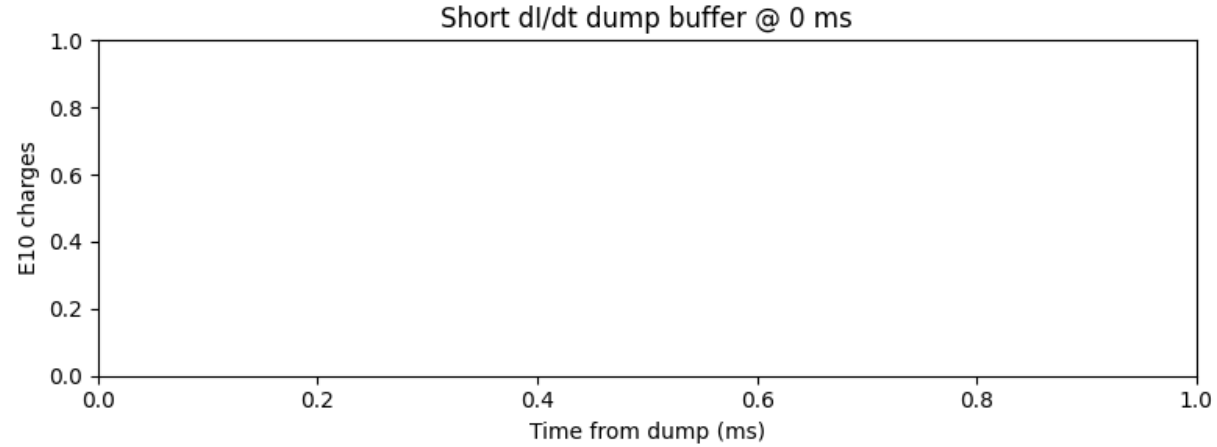


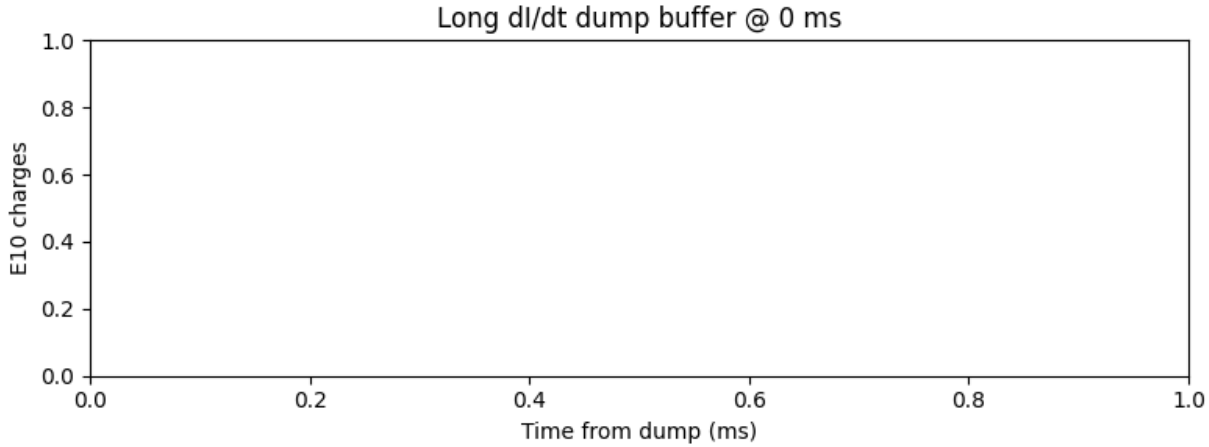





Intensity
Raw data
Short avg
Long avg
E10 charges
Cycle time (ms from injection)

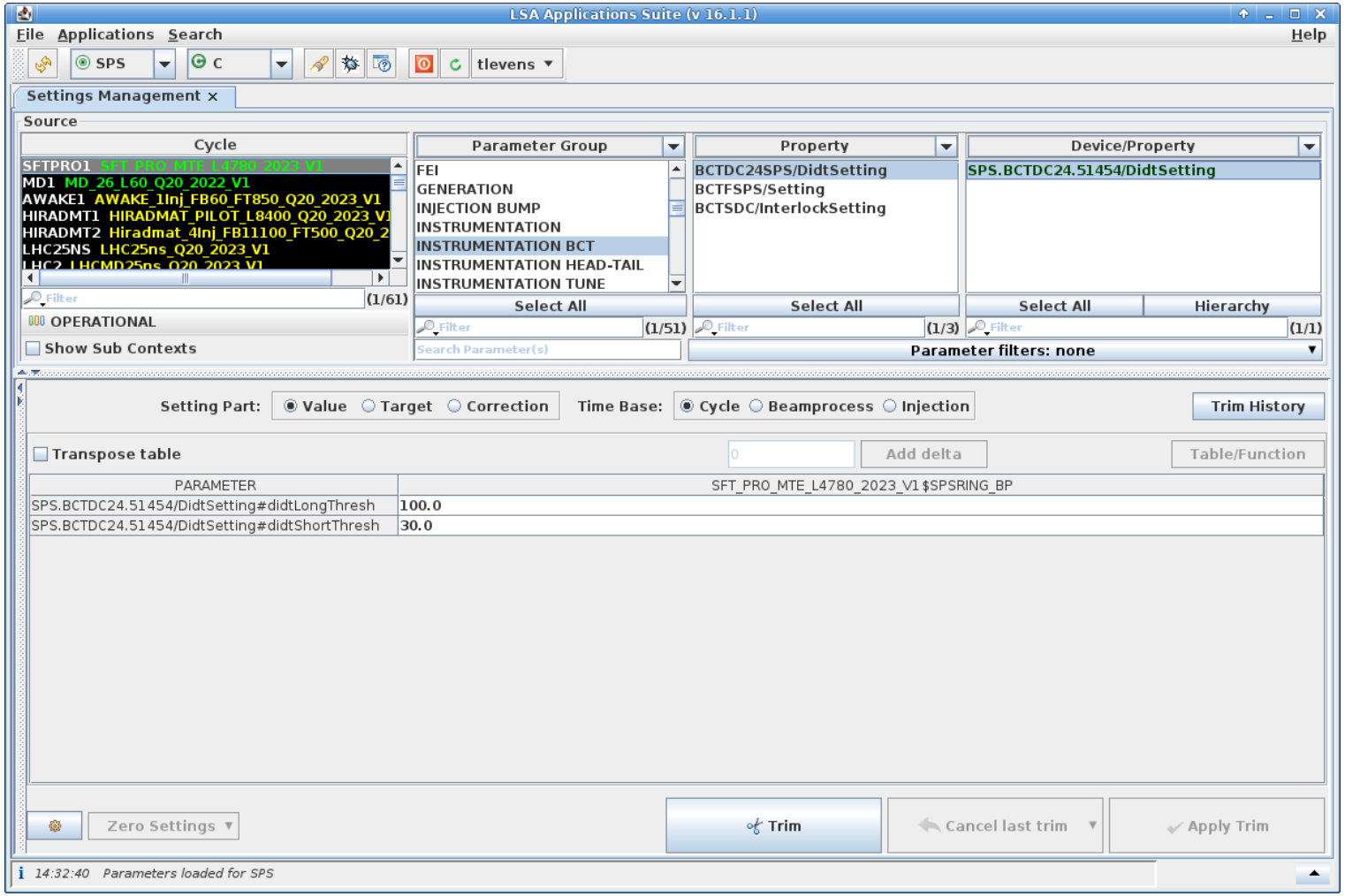

dI/dt
Short win
Long win
E10 charges
Cycle time (ms from injection)


Short dI/dt dump buffer @ 0 ms
E10 charges
Time from dump (ms)


Long dI/dt dump buffer @ 0 ms
E10 charges
Time from dump (ms)

SPS dI/dt settings

- Only OP settings exposed in LSA are the PPM thresholds for the dump level
- Expert settings for the window lengths and averaging factors (non-PPM)



SPS dI/dt logging

- dI/dt results are logged in NXCALS for every cycle

Variable Name	System	Description	Unit	Declared Type
SPS.BCTDC24.51454:DidtAcquisition:didtCalibDone	CMW	dI/dt calibration sequence was done	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtDumpStatus	CMW	dI/dt overall dump/permit status (0=PERMIT; 1=DUMP; -1=DISABLED)	Enum	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongAvg	CMW	dI/dt long window averaging nb. samples	Samples	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongCalibDumpOk	CMW	dI/dt long window dumped correctly during calibration pulse	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongCycleTime	CMW	dI/dt long window dump cycle time	Milliseconds from injection	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongDifference	CMW	dI/dt short dump buffer difference	Charges 1E10	VECTOR_NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongIntensity	CMW	dI/dt long dump buffer intensity	Charges 1E10	VECTOR_NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongLen	CMW	dI/dt long window length	Samples	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongThresh	CMW	dI/dt long window dump threshold	Charges 1E10	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongTriggered	CMW	dI/dt long window triggered dump	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtLongWrThreshOk	CMW	dI/dt long window thresholds were written	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtResultCalibOk	CMW	dI/dt overall result of calibration checks	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortAvg	CMW	dI/dt short window averaging nb. samples	Samples	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortCalibDumpOk	CMW	dI/dt short window dumped correctly during calibration pulse	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortCycleTime	CMW	dI/dt short window dump cycle time	Milliseconds from injection	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortDifference	CMW	dI/dt short dump buffer difference	Charges 1E10	VECTOR_NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortIntensity	CMW	dI/dt short dump buffer intensity	Charges 1E10	VECTOR_NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortLen	CMW	dI/dt long window length	Samples	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortThresh	CMW	dI/dt short window dump threshold	Charges 1E10	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortTriggered	CMW	dI/dt short window triggered dump	Boolean	NUMERIC
SPS.BCTDC24.51454:DidtAcquisition:didtShortWrThreshOk	CMW	dI/dt short window thresholds were written	Boolean	NUMERIC

Conclusion

- SPS dI/dt gateware and FESA implemented and working well
  - Operational since 2023

- In reality noise levels are much better than anticipated
  - < 5 E10 protons per 1ms in short window
  - < 0.2 E10 protons per 10ms in long window
- This gives us a comfortable margin to the requested thresholds

- First “commissioning” tests done with OP
  - With dumped beam ~1e11 lower dI/dt thresholds and check that the interlock activates when thresholds are below beam intensity – OK

- We request MPP approval to enable the BIS input so that OP can start gaining operational experience with the dI/dt

AOB: SPS intensity interlock

- SPS also has an "intensity interlock" available on both BCT3 and BCT4
  - Today is only used for AWAKE to avoid accidentally extracting multi-bunch beam
  - Has been used on other cycles in the past
- Intensity is checked 100ms after last injection, if it is above/below a set threshold then the beam is dumped
  - Comparison done in FESA RT action
  - FESA triggers an LTIM with a RDA set
  - LTIM output connected to CIBU input via special adapter module
- This comparison has also been implemented in the FPGA gateware of the 24-bit acquisition and a (second) direct output to a CIBU available
- Propose to connect this to a new CIBU channel in BA5 to replace the existing connections in BA3/BA4. Advantages:
  - Only one BCT for the entire intensity range
  - No software involvement apart from setting (PPM) thresholds
  - Significantly less complicated
  - Preparing for obsolescence of old BCT3/BCT4

www.cern.ch