Status of the DC-DC ASICs development

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Outline

- AMIS2
  - New TID tests with Low Dose Rate at -30°C
  - New Efficiency tests
  - Temperature Tests
- AMIS3
  - Description of the chip
- AMIS4
  - Description of the chip
  - Protection circuit
- IHP

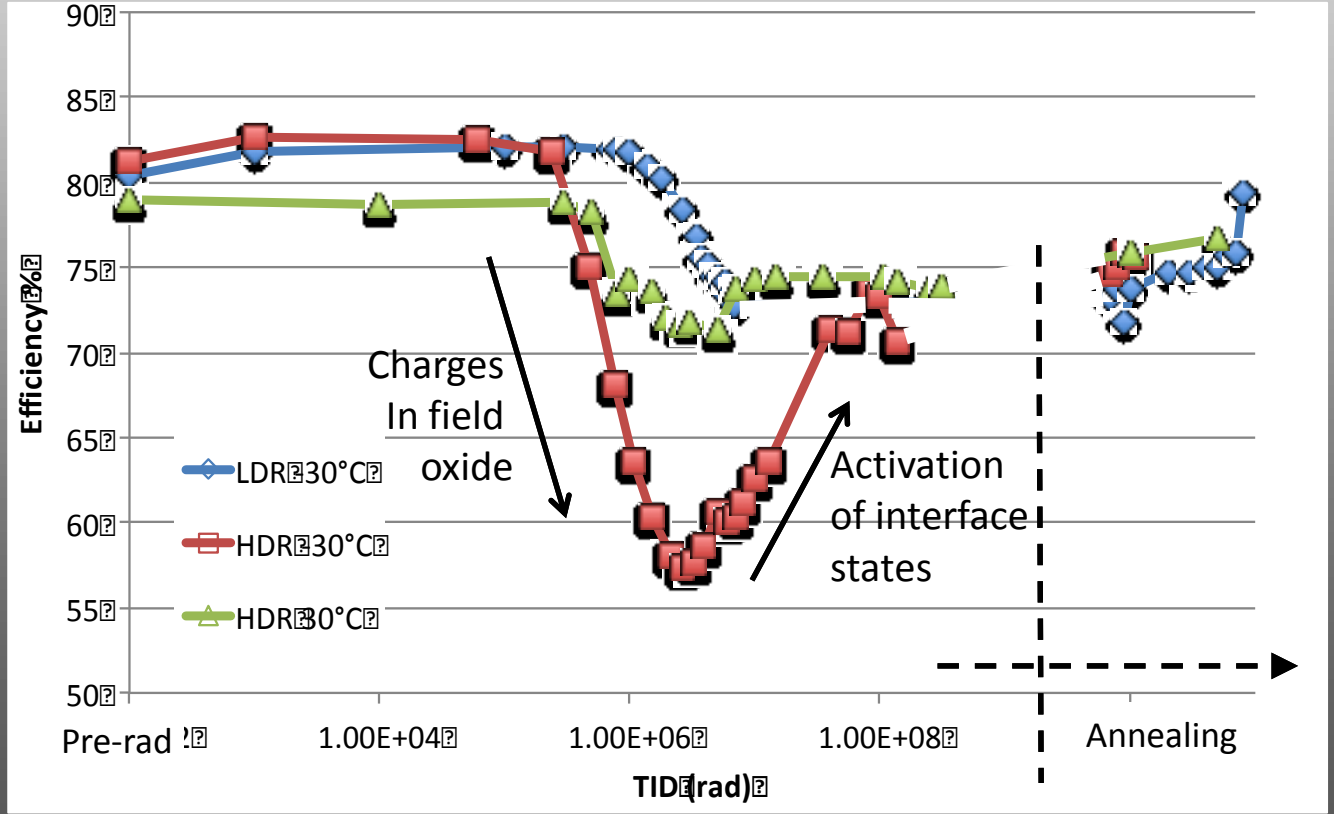
AMIS2 Radiation tests

AMIS2 has been tested with different Dose Rate:

- High Dose Rate (HDR) = 77Krad/min (250Mrad reached in few days)
- Low Dose Rate (LDR) = alternating 300 rad/min with no irradiation for the same exposure time (2Mrad reached in 1 month)

LDR is more similar to HLLHC dose rate of 47rad/min (calculated as 250Mrad over 10 years, worst case condition)

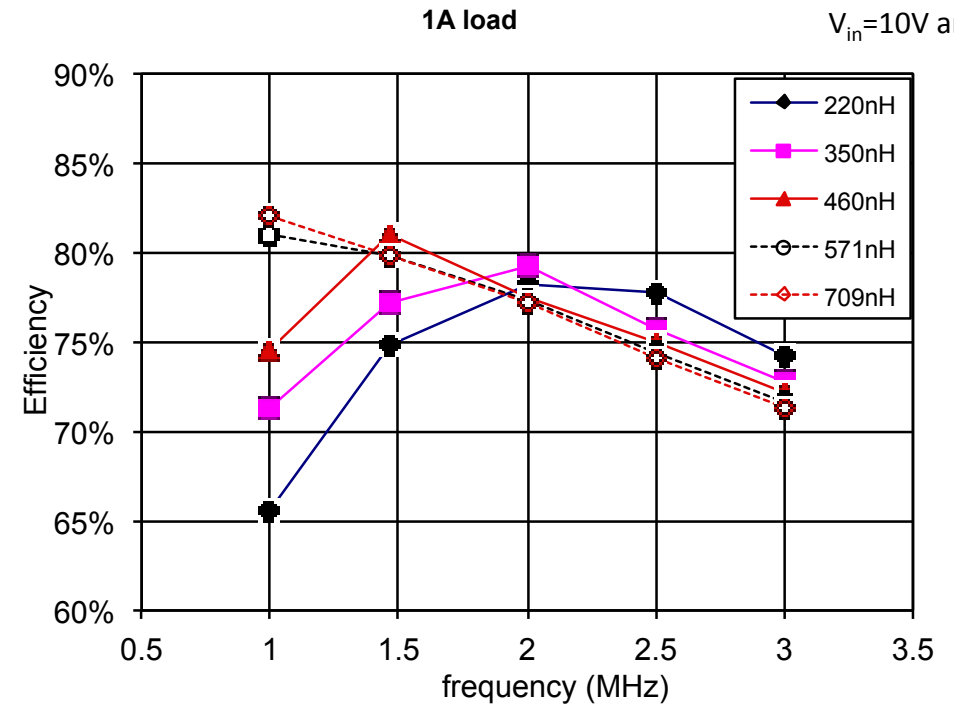
Two different testing temperature: 30°C and -30°C (more similar to experiment environment)

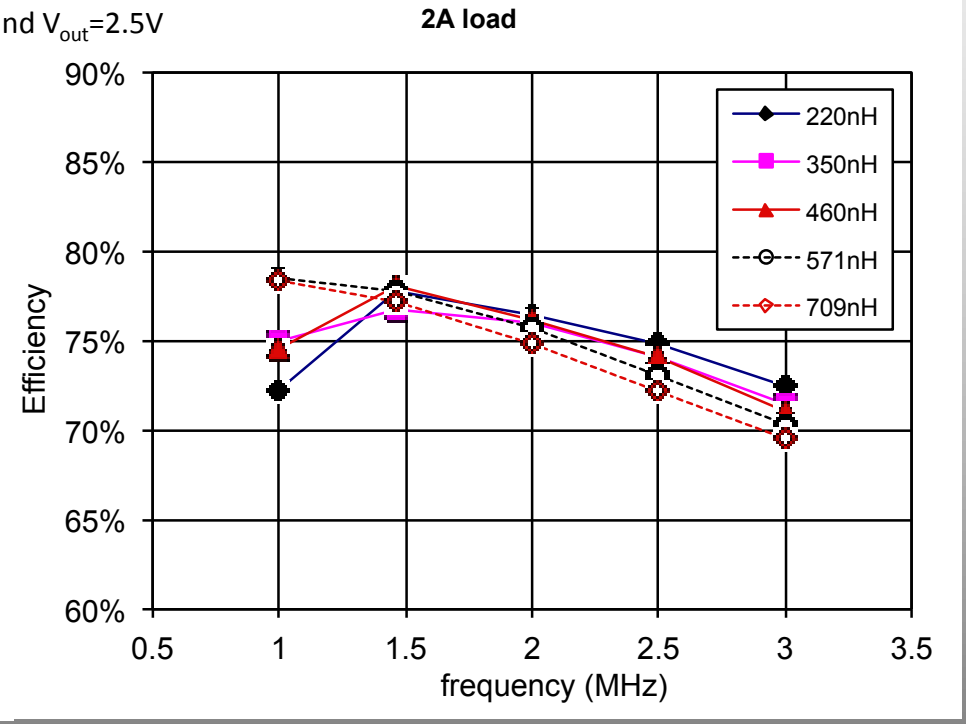


With LDR the maximum drop is limited to 9%, reduced to 2% after 3 days annealing at 100°C.

With respect to the HLLHC dose rate this is by far a worst case results.
In addition, in the new design AMIS4, the number of parasitic source drain path is reduced

AMIS2 efficiency

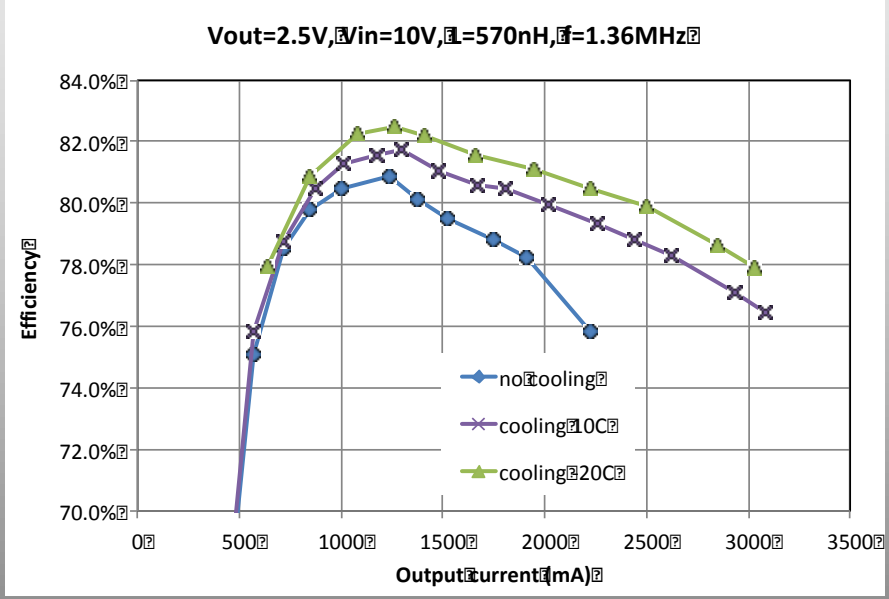




- the best efficiency is obtained at 1MHz with high value of inductance (>460nH).
- At 2MHz the efficiency drop is 2-3%, but it allows using a smaller inductor (220nH), helpful for limiting the total weight of the converter.

Temperature tests

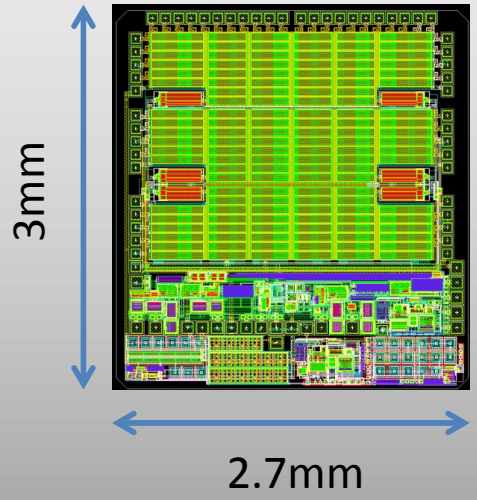
- In the absence of cooling, the output V increases steeply as from about 1.2A load. We can estimate the following chip T:
  - T=50C @1.5A
  - T=90C @2A
  - T=110C @2.2A
- Efficiency is heavily influenced, especially at large loads



AMIS3 chip

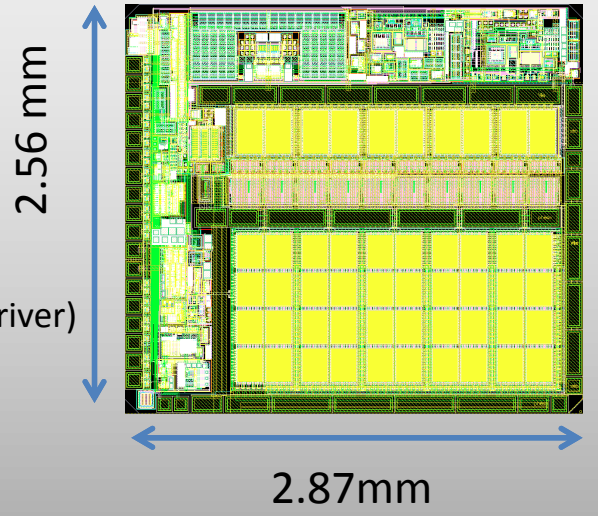
- Third prototype in the On-Semi I3T80U technology
- Design included in MPW run of October 2010
- Expected back in Mid March 2011
- It is the same layout of AMIS2 with additionally:
  - Integrated linear regulator (one for all the chip)
  - High voltage bandgap
  - Change in sawtooth generator to avoid the duty cycle limitation found in AMIS2
- Similar Pinout of AMIS2
- Package in QFN48 for testing
- Package in QFN32 for system tests

- External component needed:
  - Capacitor for Linear regulator
  - Capacitor for Bootstrap



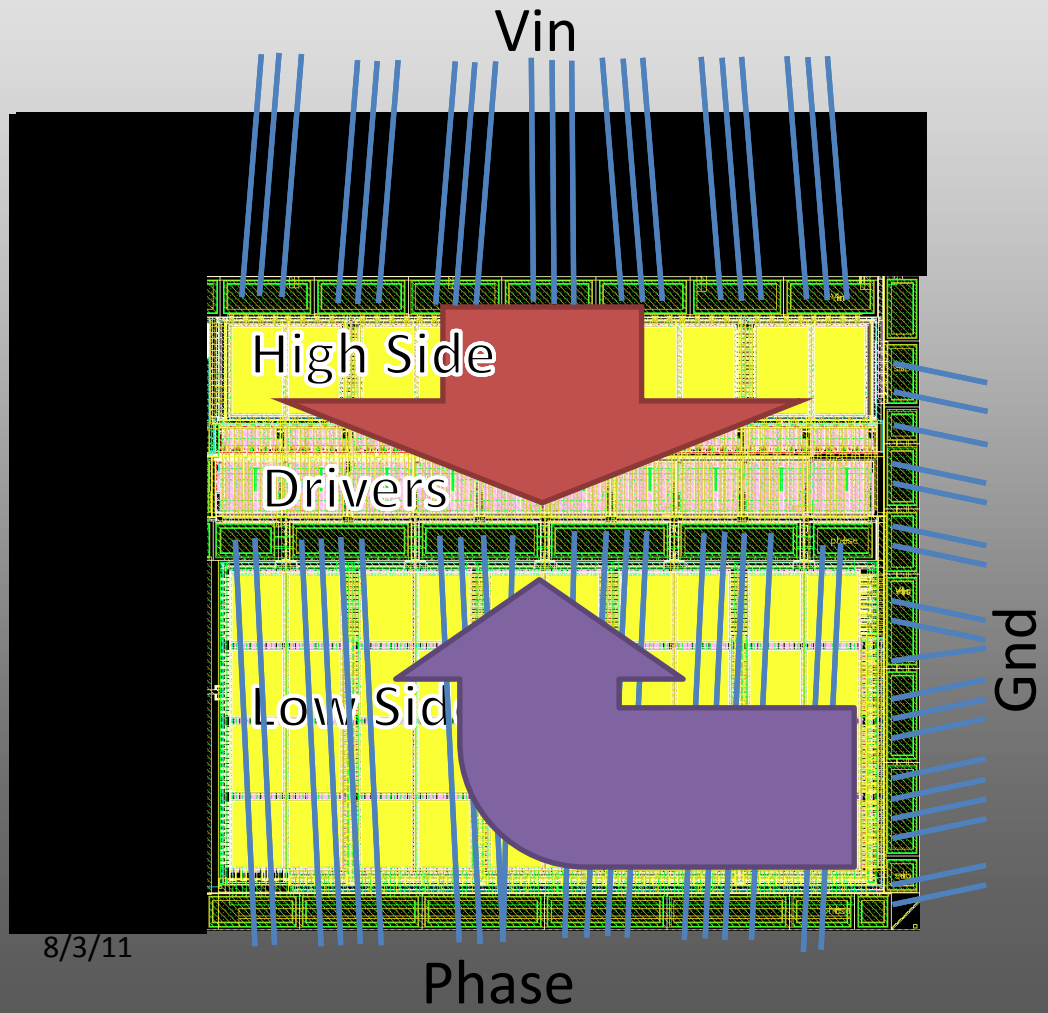
AMIS4 chip

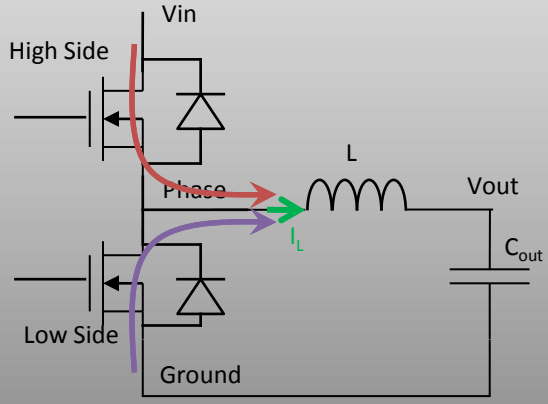
- Forth prototype in the On-Semi I3T80U technology
- Design included in MPW run of January 2011 (4 months in advance)
- Expected back in Mid May 2011
- Completely new design, based on knowledge from IHP ASICs
- Features integrated in the prototype:
  - Bandgap
  - Linear regulators (four different regulators: Pre-Reg, Analog, Digital and Driver)
  - Oscillator (with sawtooth)
  - Handling of the dead time with adaptive logic (improved from IHP2)
  - Triplication and logic against SEU
  - Improvement of the power transistors' design to reduce TID effects
  - Possibility to enable only 2/5 of the power transistors for small Iout
  - Protection
    - Over-current
    - Over-temperature
    - Input under-voltage
  - State machine for more reliable start-up procedure and handling of the signal from protection circuitry and Power Good signal generation
  - Enablers
    - Complete circuit
    - Dimension of the power transistors
- External component needed:
  - Capacitor for Linear regulator
  - Capacitor for Bootstrap



New layout and bonding

The pad disposition on-chip is very different than in our previous designs. This has been done to minimize the on-chip power distribution and optimize of the number of bonding

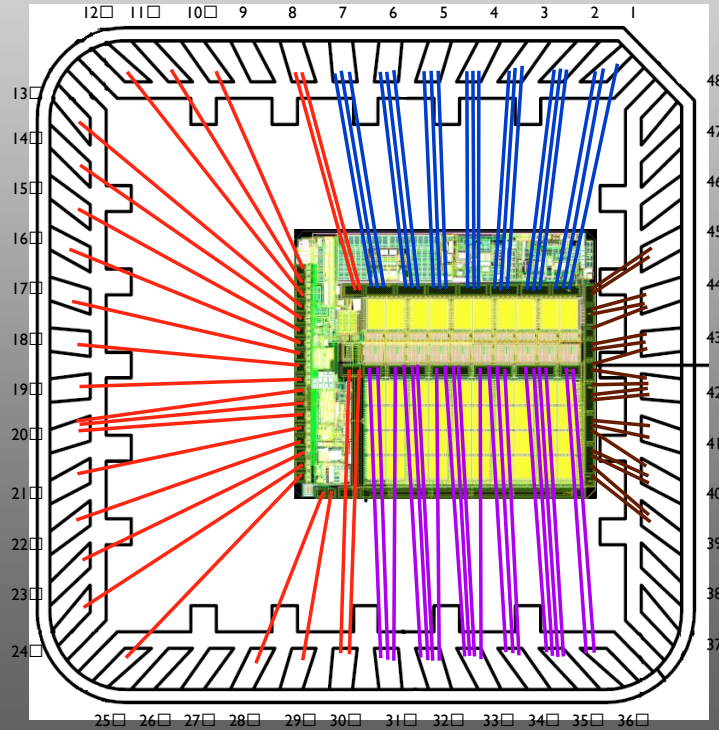




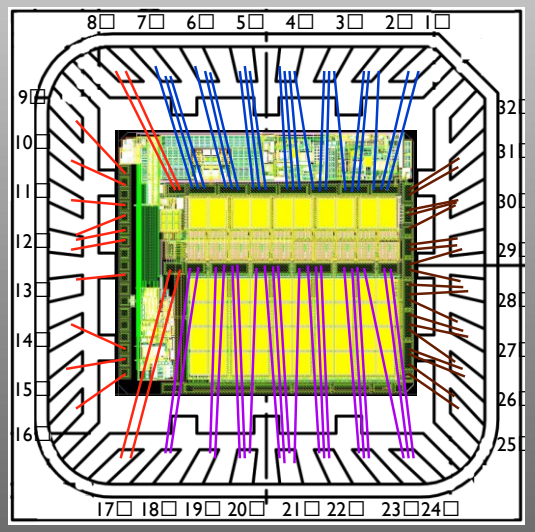
Bonding Diagram

The ASIC will be packaged in QFN48 for first testing phase, then in QFN32 for system tests. We are looking if this bonding diagram is feasible for mass production.

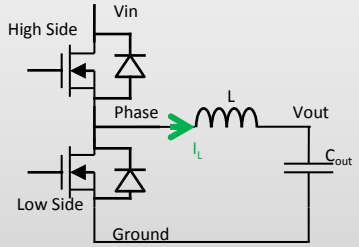
QFN48, 7x7 mm^2



QFN32, 5x5 mm^2



Switch dimensions

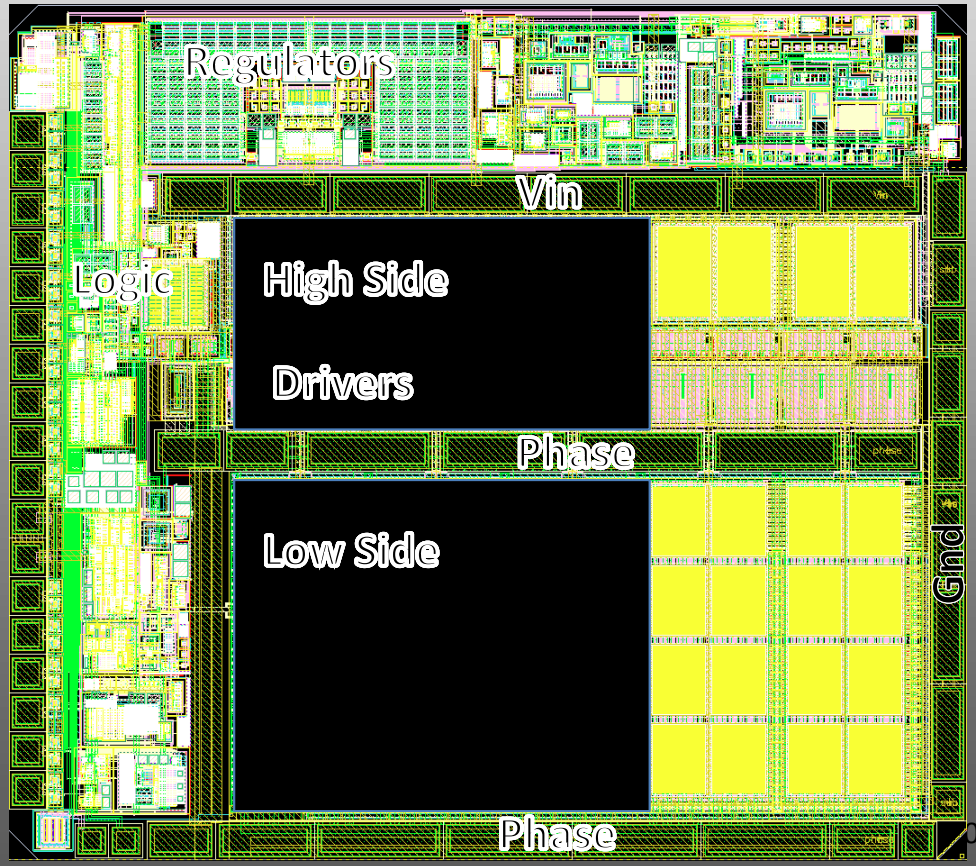


Power transistors have been carefully for maximum efficiency for

- Iout=1-3A
- L=200nH-400nH
- f=1-3MHz

As for AMIS2 with L=200nH the efficiency is few % smaller but the inductor mass is strongly reduced

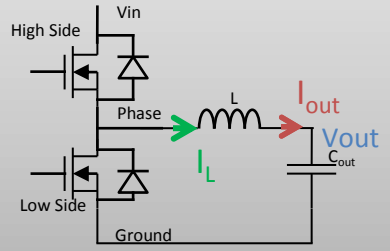
With an external pin only 2/5th of the switches can be enabled
This allows having less power dissipated in switching and driving operations

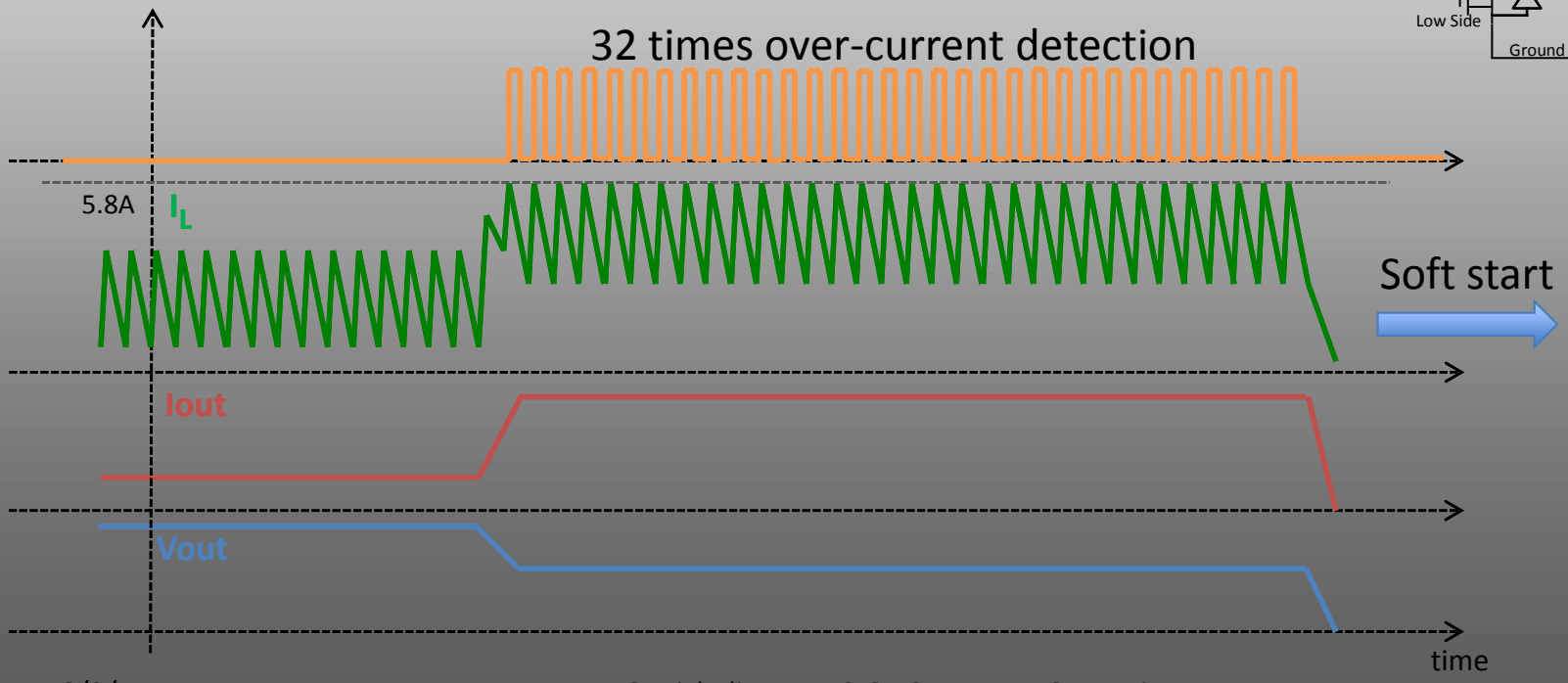


State Machine

It allows handling the soft start procedure and the fault signals from protection circuitry:

- Over – Current: if High Side current over 5.8A for 32 consecutive times
- Under – Voltage: control on Vin if lower than a threshold
- Over – Temperature: if Tchip>115°C
- Disable Buck: from external pin





IHP technology tests

- HV transistors used in IHP1 have been improved from IHP for Single Event Burn Out tolerance
- We received the test structures from IHP
- We are currently preparing the test board
- Heavy Ions test is scheduled for the first week of April at Louvain-la-Neuve
- If the test is positive, then TID and protons tests will be done
- If also these tests are positive, then we will go for a submission of a chip similar to AMIS4 in this technology.