Mitch Newcomer
Representing work at RAL, Liverpool, BNL and Penn

SERIAL POWER UPDATE ATLAS BARREL SCT

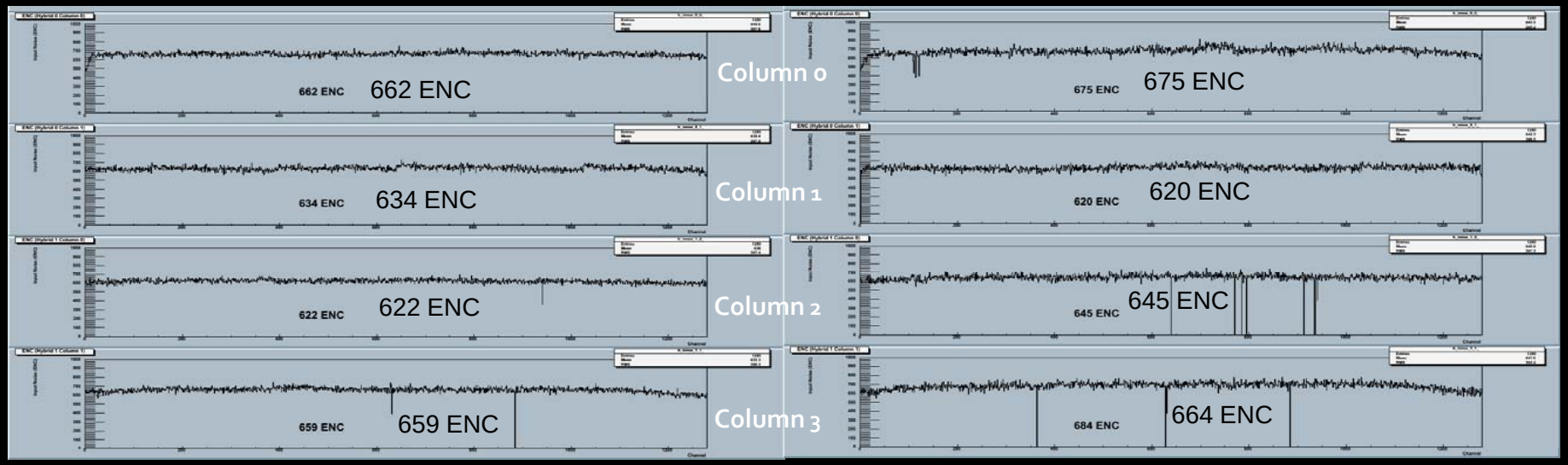
Stave Module – Electrical Performance

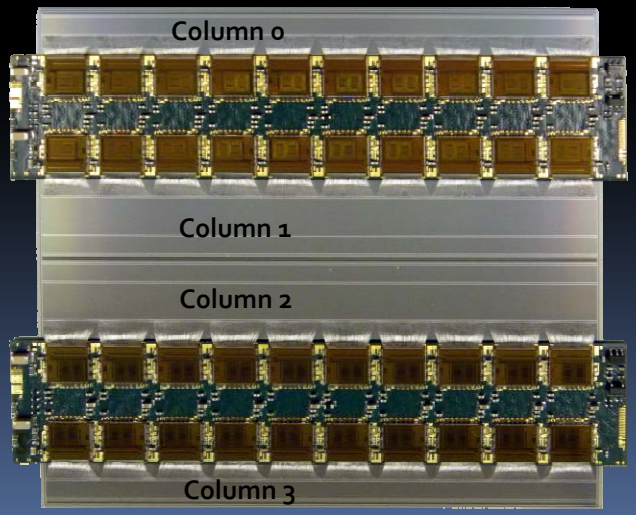
- Measurements on Modules @ Liverpool
- First Measurements on Stavelets @RAL
- Control of Serial Powering
- New stuff

****Serial Powered Module Material Burden: ~.016% Xo**
Based on SPP ASIC & passives including capacitive coupling caps for digital signaling and hybrid area required for components. Thanks to Tony Affolder, Liverpool

Stave Module – Electrical Performance (Liverpool)

Parallel Powered (reference) | **Serially Powered**





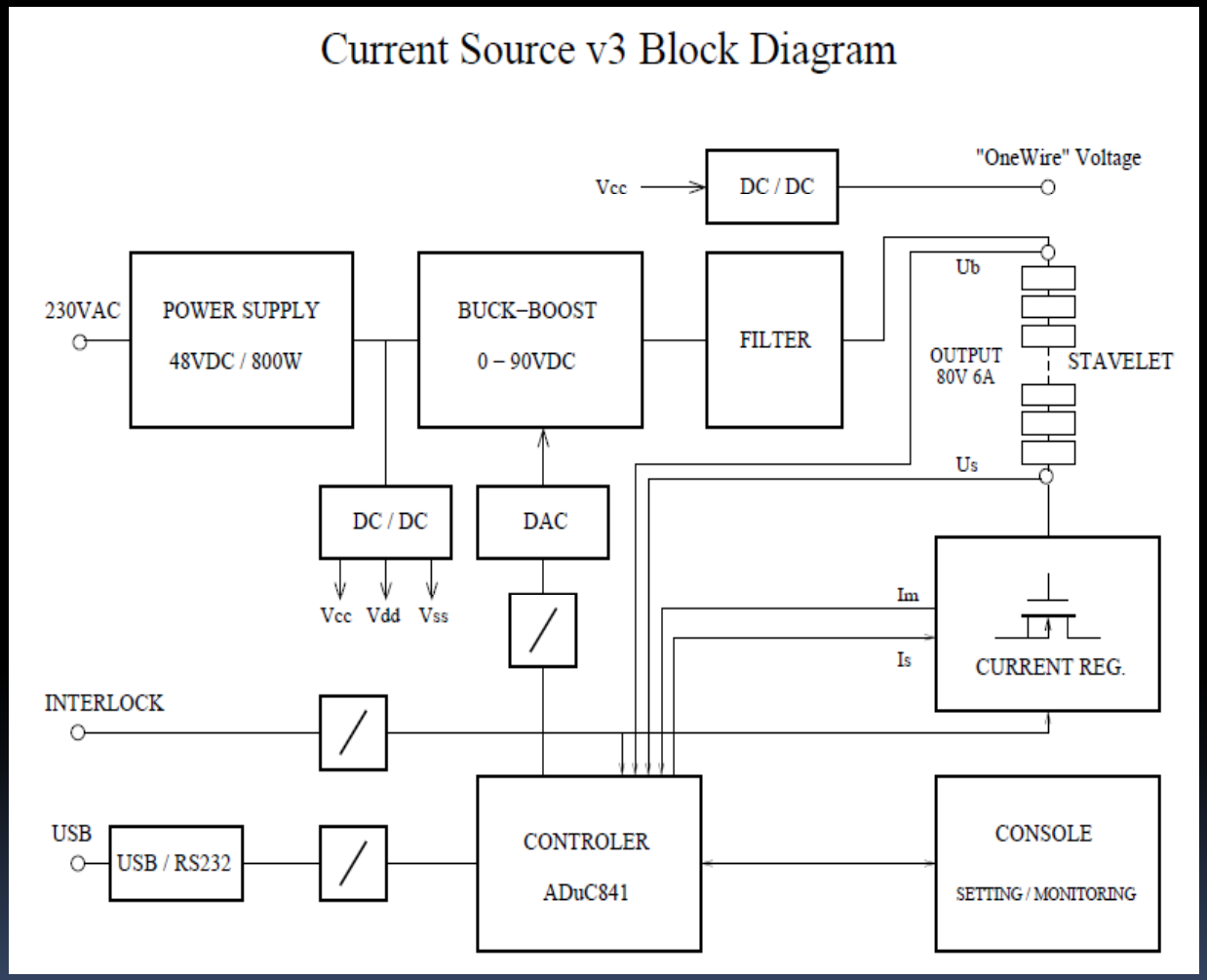
Serially Powered Module Works!

- Input Noise comparable between powering schemes
- Evidence of a noise signature seen on module(s)
  - Outer columns have higher noise compared to inner
  - Irrespective of powering scheme

New Generation of Serial Power Current Source

2nd Gen Current Source*

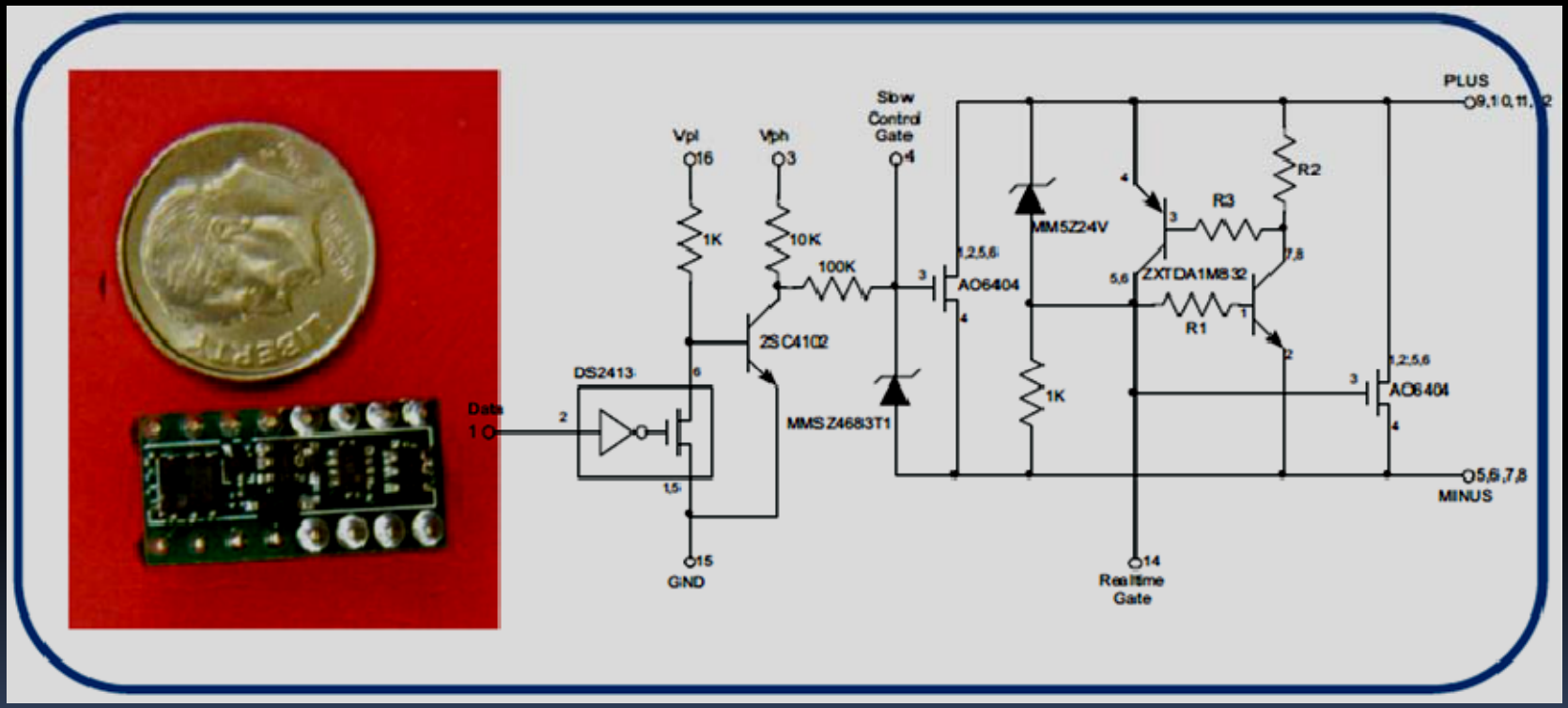
• Includes overvoltage protection, isolated USB interface and Programmable PID coefficients for system tuning.



* Designer Jan Statsny (work supported by RAL)

Stavelet Protection

One wire Addressable by Hybrid Serial Power Control developed by BNL.
Installed on each of the 8 Stavelet Hybrids.
An SCR function allows autonomous shut down on Over Voltage Sense



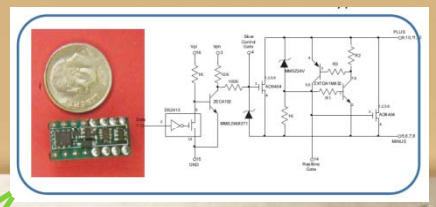
Progress on SCT Stavelet's @ RAL

Slides from : Peter Phillips

John Matheson

Giulio Villani

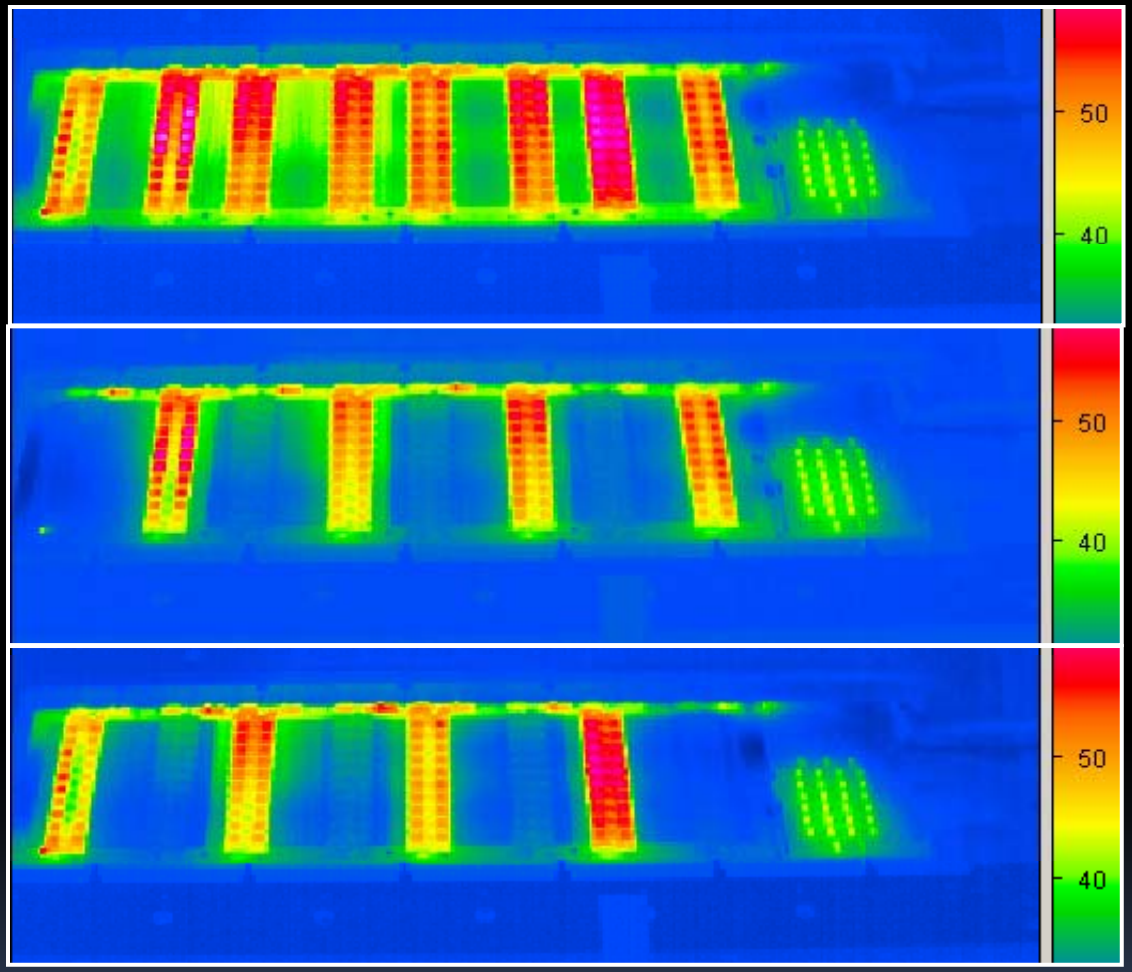
Stavelet Numerology (@RAL)



S@

Hybrid	0	1	2	3	4	5	6	7
BCC	62	61	60	59	58	57	56	55
MUX	7	6	5	4	3	2	1	0
DEMUX	14/15	12/13	10/11	8/9	6/7	4/5	2/3	0/1
Coupling	DC	AC	AC	DC	AC	DC	AC	DC
Module	0		1		2		4	
s/n	1		9		3		4	

Thermal Images of the Stavelet in Operation (RAL)



All hybrids on

22.7V
5.09A

Slow control disables odd hybrids

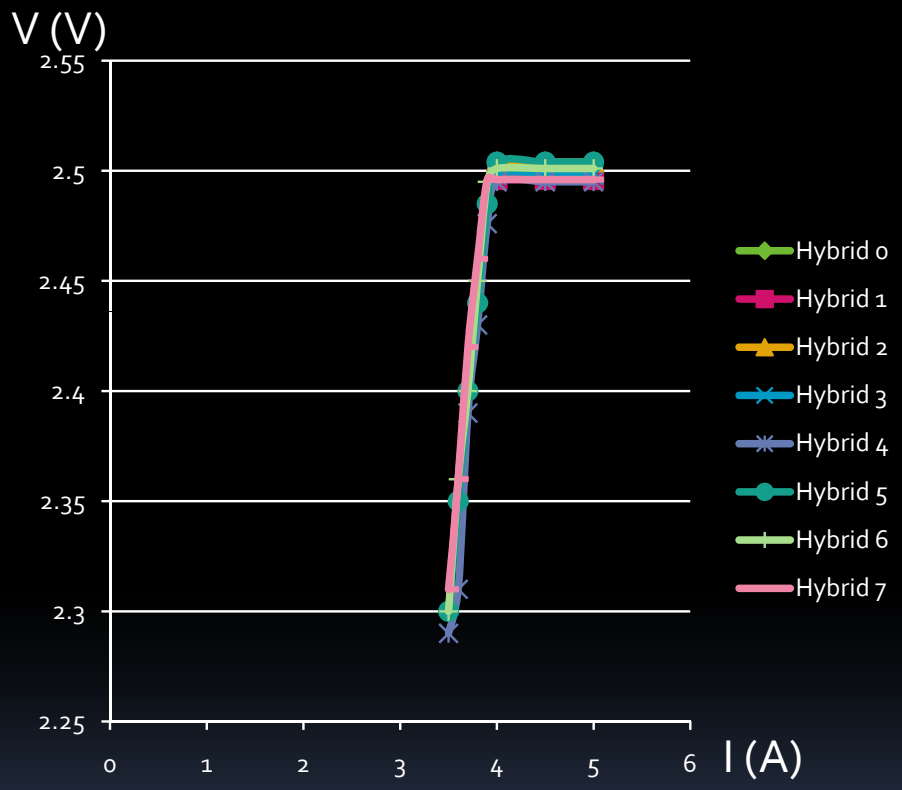
12.7V
5.09A

Slow control disables even hybrids

Each hybrid may be bypassed using the PPB 1-wire operated shunt
Voltage differences consistent with 2.5V per hybrid
2.7V overheads: bus tape, bond wires, PPB PCBs, external cabling

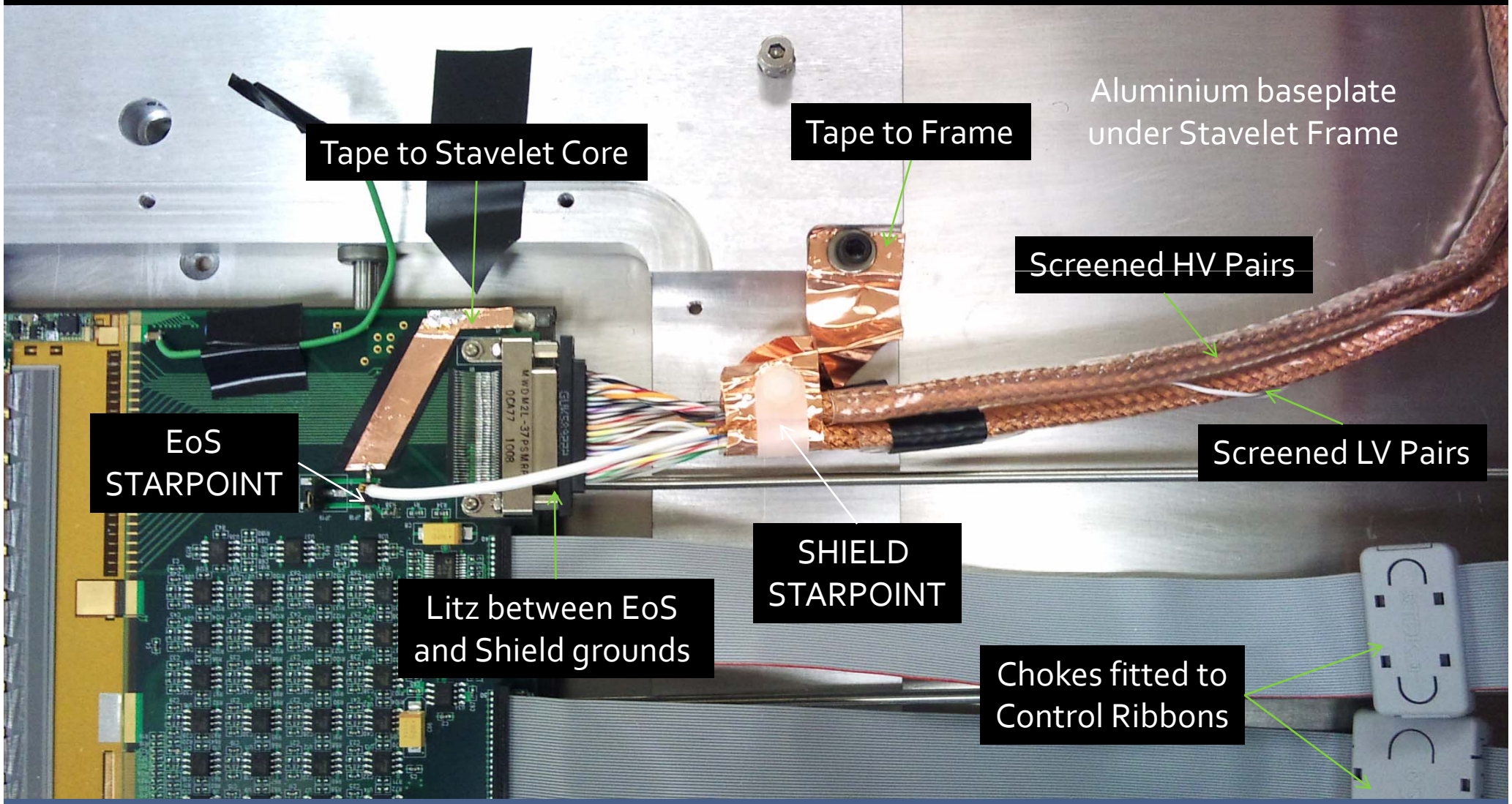
Stavelet Hybrid Voltages vs Current (RAL)

I	H0	H1	H2	H3	H4	H5	H6	H7
3.5					2.29	2.3	2.3	2.31
3.6					2.31	2.35	2.36	2.36
3.7					2.39	2.4	2.4	2.42
3.8					2.43	2.44	2.45	2.46
3.9					2.476	2.485	2.495	2.496
4.0	2.499	2.496	2.504	2.498	2.495	2.504	2.501	2.496
4.5	2.499	2.496	2.504	2.498	2.495	2.504	2.501	2.496
5.0	2.499	2.496	2.504	2.498	2.495	2.504	2.501	2.496
A	V	V	V	V	V	V	V	V



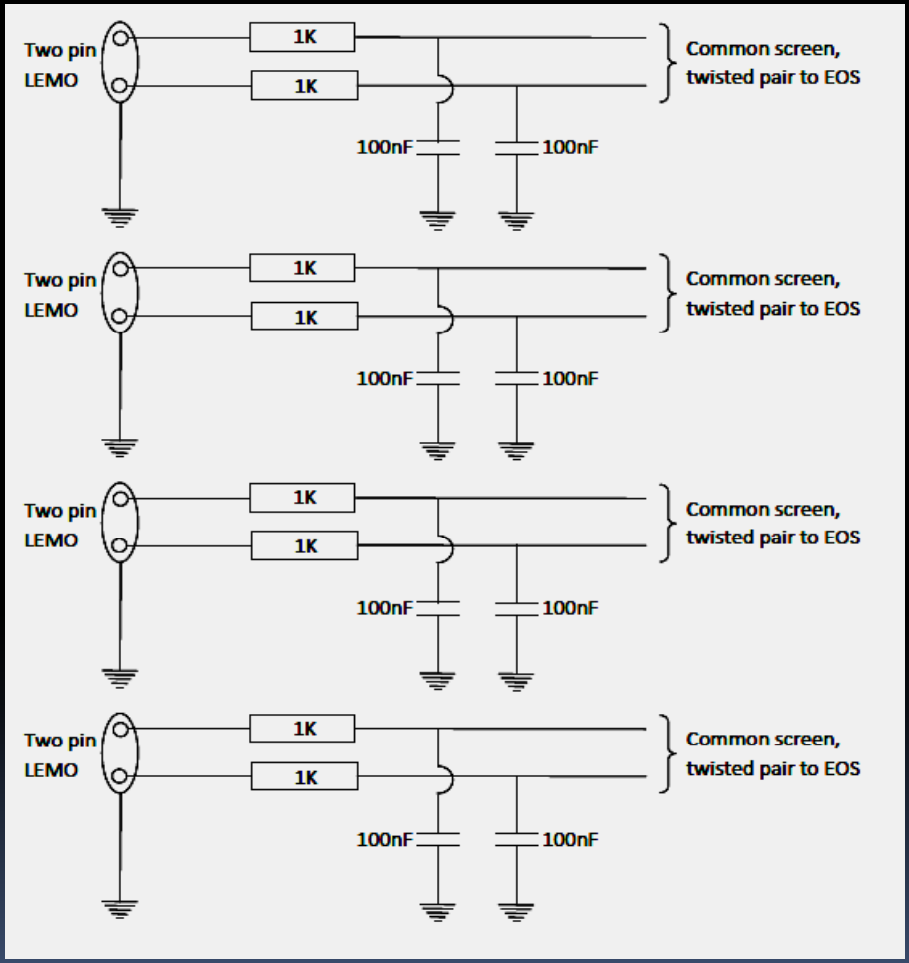
The ABCN-25 "M" shunt and the hybrid's control circuitry work as expected: Constant hybrid voltage from 4.0A

G&S Improvements (RAL)



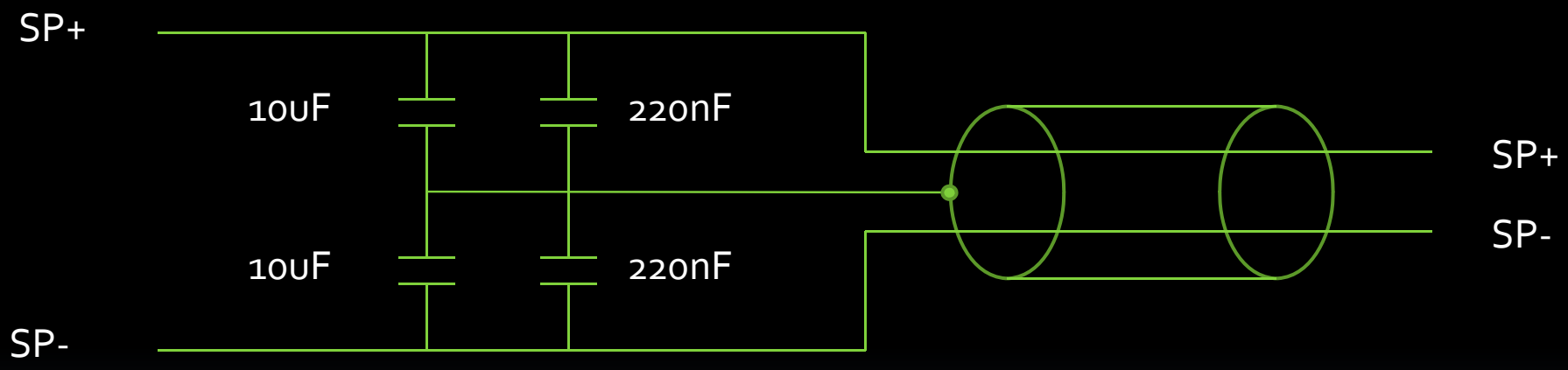
Aluminium cover connected to baseplate with Cu Tape

Stavelet HV Filter (RAL)



Implemented within diecast box

External LV Filter (RAL)



FROM PSU

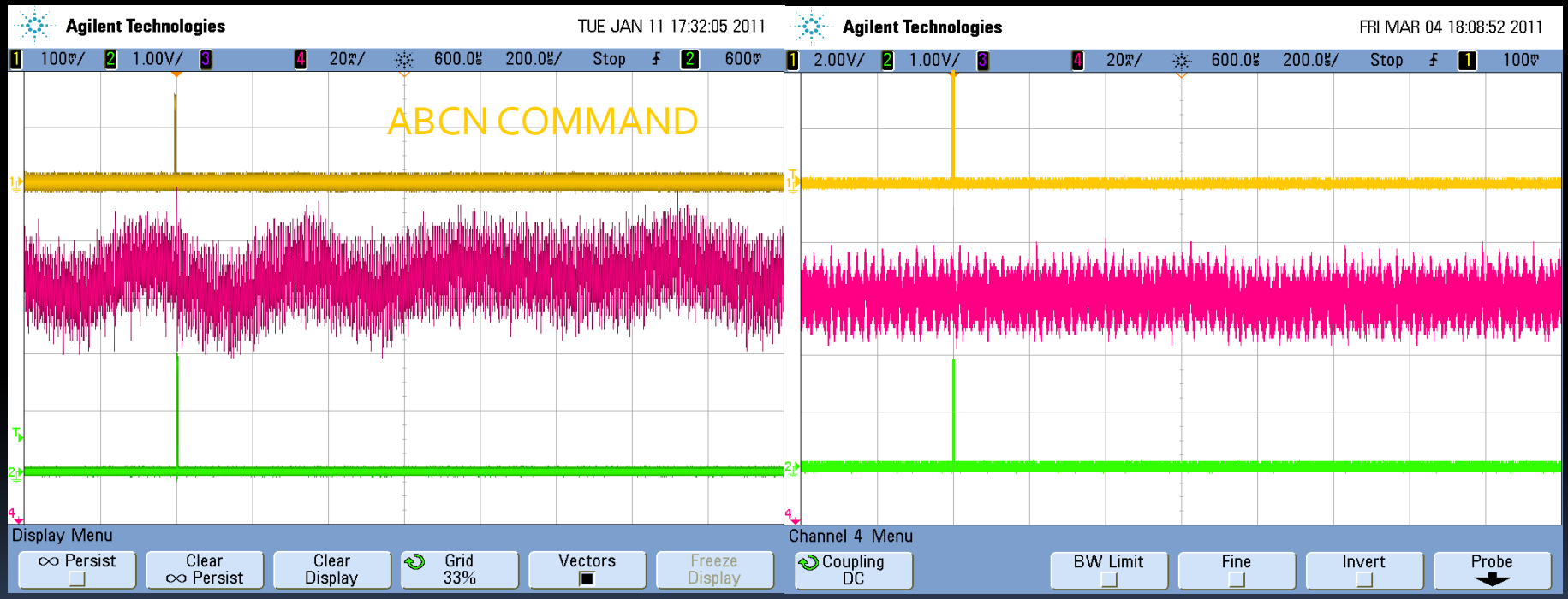
Screened LV cable to Stavelet
(screen is connected to shield)

Jan Stastny's Current Source: Current Noise, Stavelet running at 5A

COM

I_{SP}

DATA



Before G&S Improvements, without Internal Filter

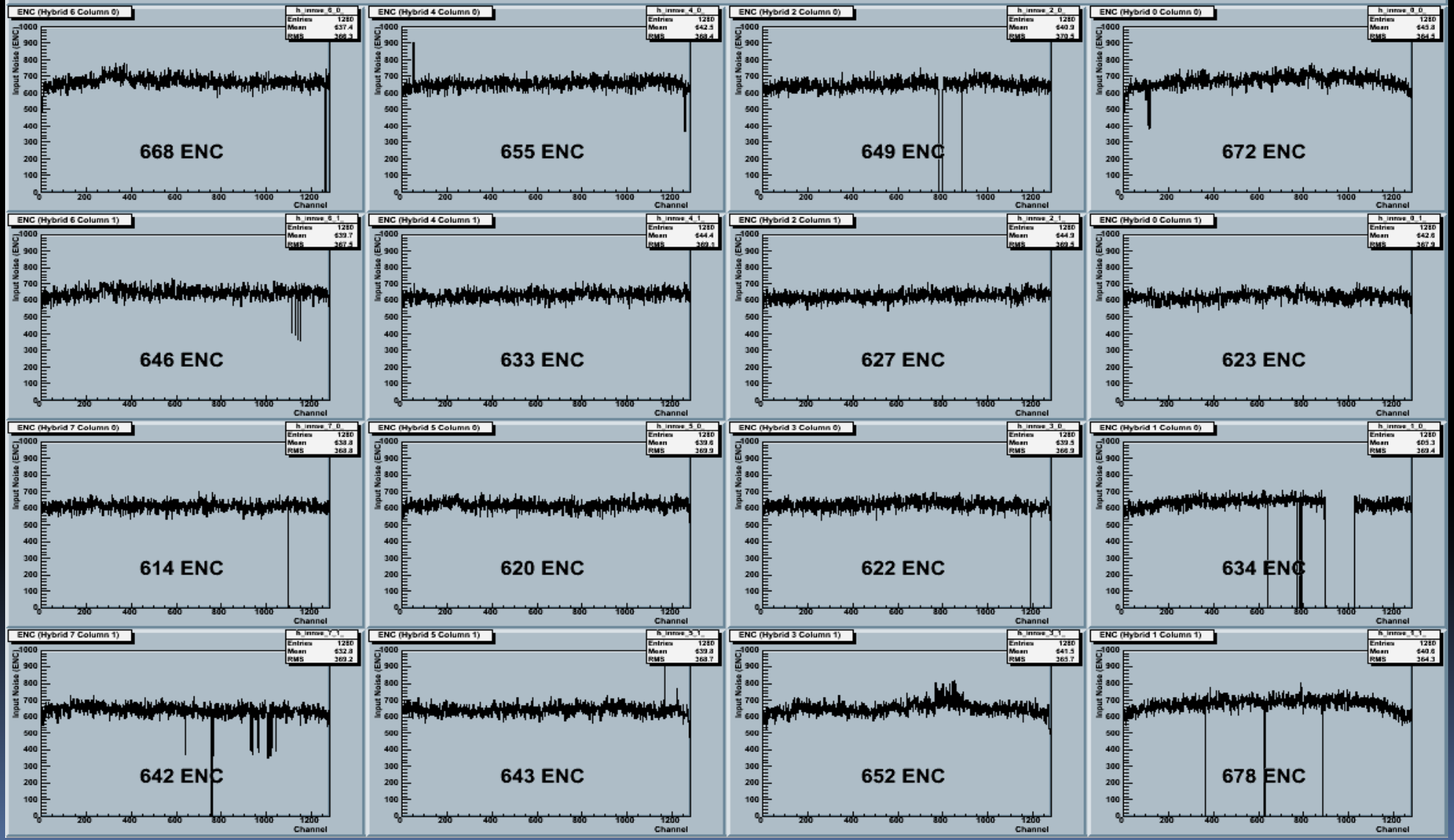
After G&S Improvements & with Internal Filter

ATLAS Stavelet Measurements @ RAL (Peter Phillips, John Matheson)

3rd Mar 2011

Jan Stastny Current Source at 5A, 230V bias, ALL MODULES ON

Run 1451 Scan 3

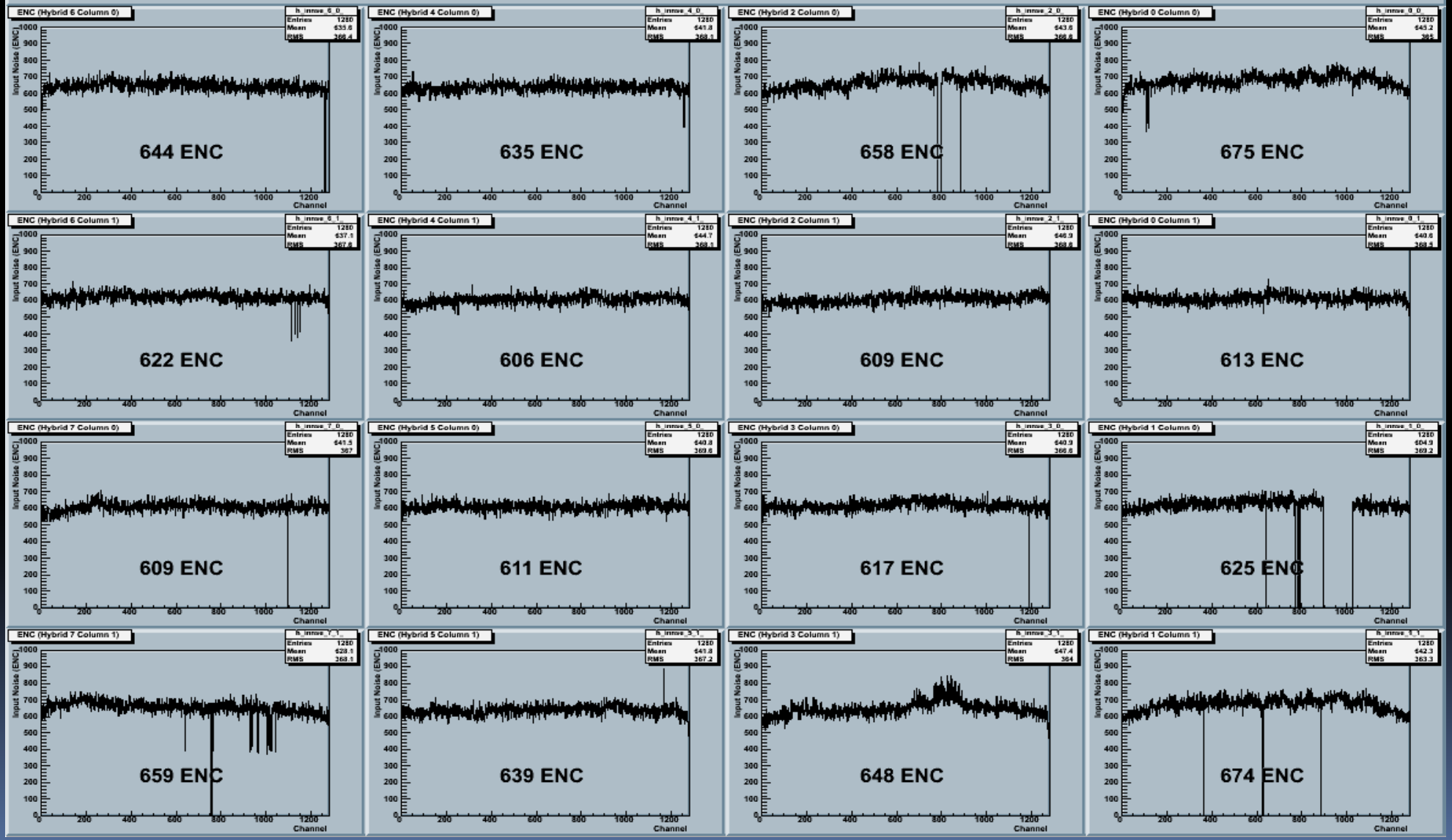


ATLAS Stavelet Measurements @ RAL (Peter Phillips, John Matheson)

3rd Mar 2011
COMPOSITE

Jan Stastny Current Source at 5A, 230V bias, ODDS AND EVENS

Run 1 Scan 3



Evolving Serial Powering Protection ASIC

2010 Power Working Group Presentation Described SPP chip and simulations in detail.
"Serial Power & Protection (SPP) ASIC for 1 to 2.5V Hybrid Operation"

http://indico.cern.ch/getFile.py/access?contribId=11&resId=0&materialId=slides&confId=85278

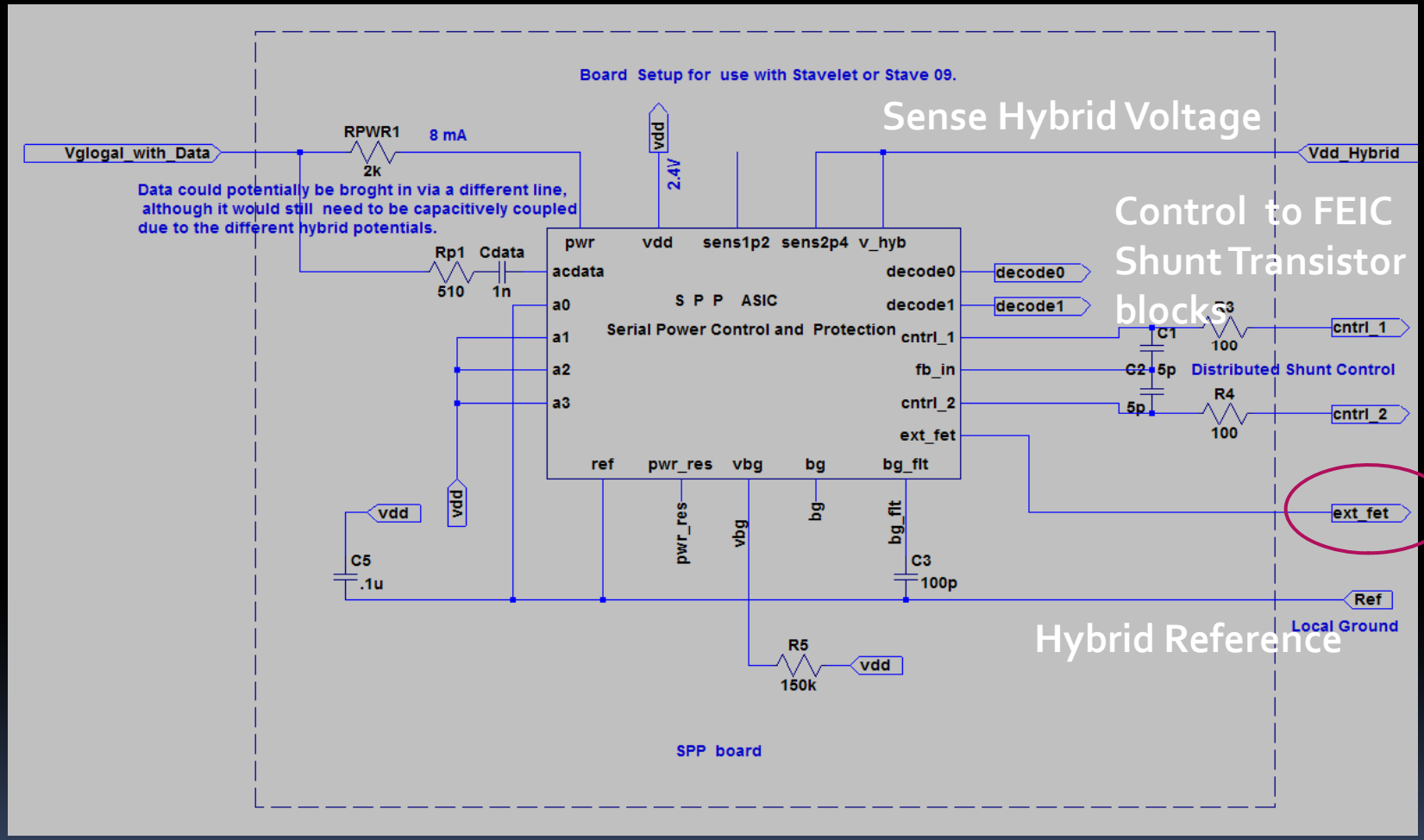
•SPP chip has internal shunt regulator to set its voltage to 2.3V.
•Allows two operating regimes for control voltage going to FEIC based shunt transistors: .4 to 1.0 regulate, 2.1 to 2.3 shut down hybrid.
•On chip band gap forms reference for SPP 2.3V and for hybrid voltage.
•Hybrid voltage may be set from 1V to 2.5V using an attenuator network on V hybrid.

2010 SPP Prototype

•Autonomous shut down for Over Voltage.
•One extra stave wire supplies power to the SPP and Programmable shut down control

Additional features considered in 2011:
•On board shunt transistor available to guarantee hybrid switch off.
•Hybrid Voltage programming planned after first prototype
•Rad Hard Version next

SPP Block with Signals (2010)



First Prototype of SPP block ready for testing

IBM CMOS8RF 130nm Technology

Analog Control loop includes:

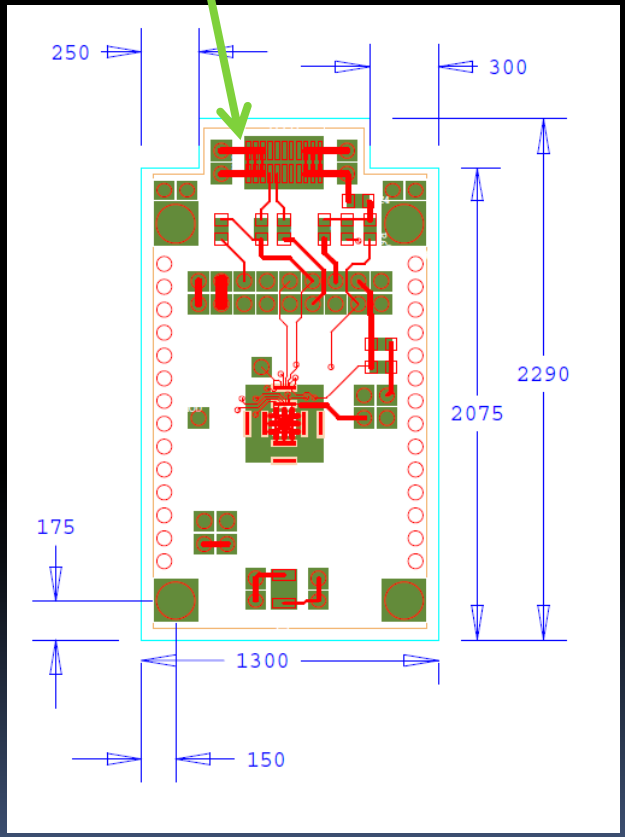
- 1.1 V BandGap .
- SPP 2.3V internal shunt regulator.
- Hybrid Regulation loop suitable for use on hybrids or staves.

Submitted for fab May 2010
Returned Jan 2011

Chip on board test PCB prepared
but due to bond pad size: 60X95um
Pad layout needed to be reworked.
To be sent out this week.

Test board plug in compatible with ABCn Modules and Stavelets.

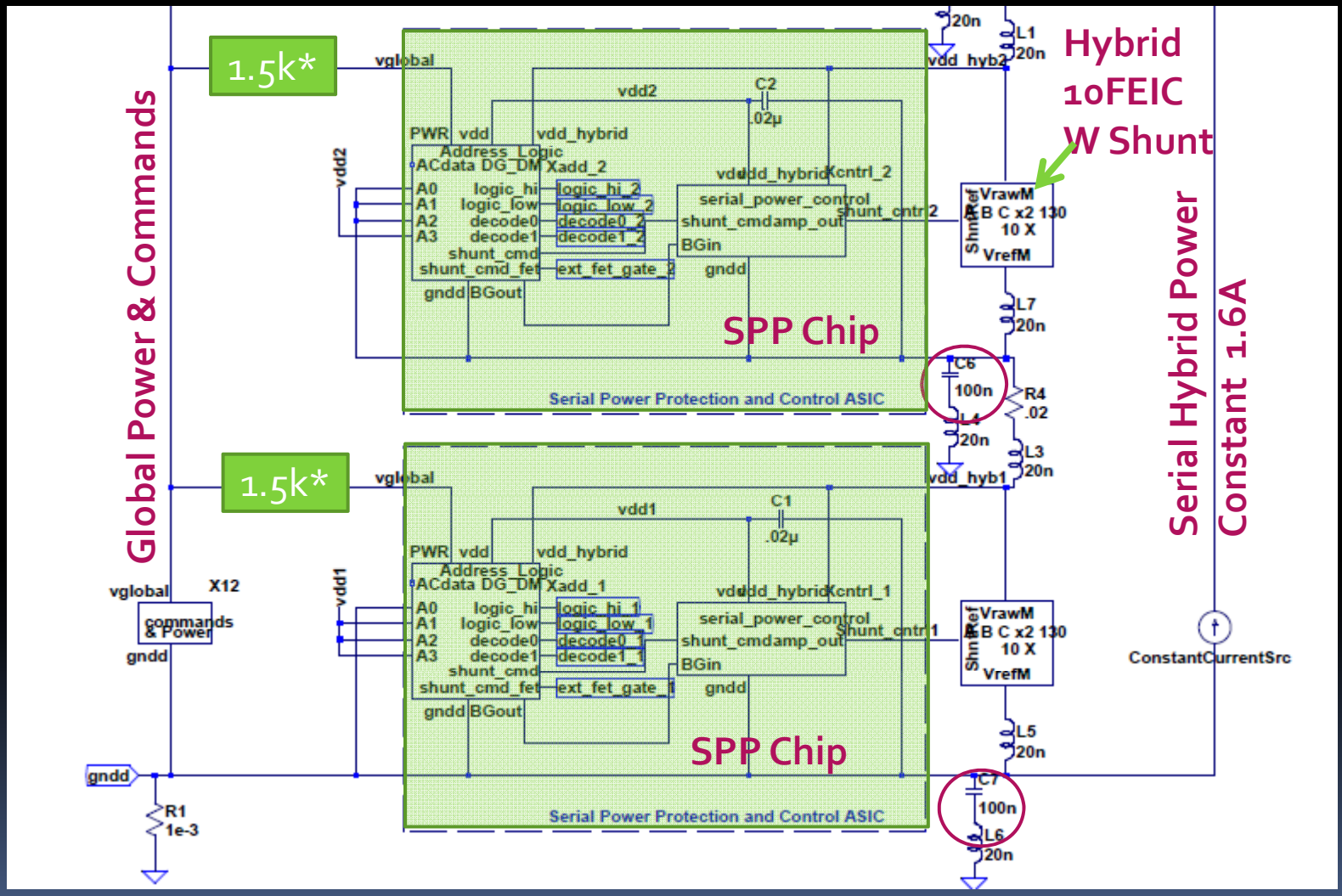
Connector Pin compatible with BNL Protectiion board socket on Hybrid



SPP – Fall 2010 Hybrid simulations

- Full Monte Carlo HSPICE schematic simulation of 12 hybrids including realistic connections and parasitics CMOS 8RF models for SPP.
- Pulse-width modulated signal superimposed on Vglobal (25v)
  - Command pulse amplitude: 2.2v
  - Narrow pulse: 50 ns
  - Wide pulse: 150ns
  - 4 address bits/1 data bit

Serial Hookup of SPP Chip for Simulation



*See Slide 17 for proper hookup to V global

SPP – 12 hybrid HSPICE simulations (Monte=10)

Vglobal (25v) SPP pwr

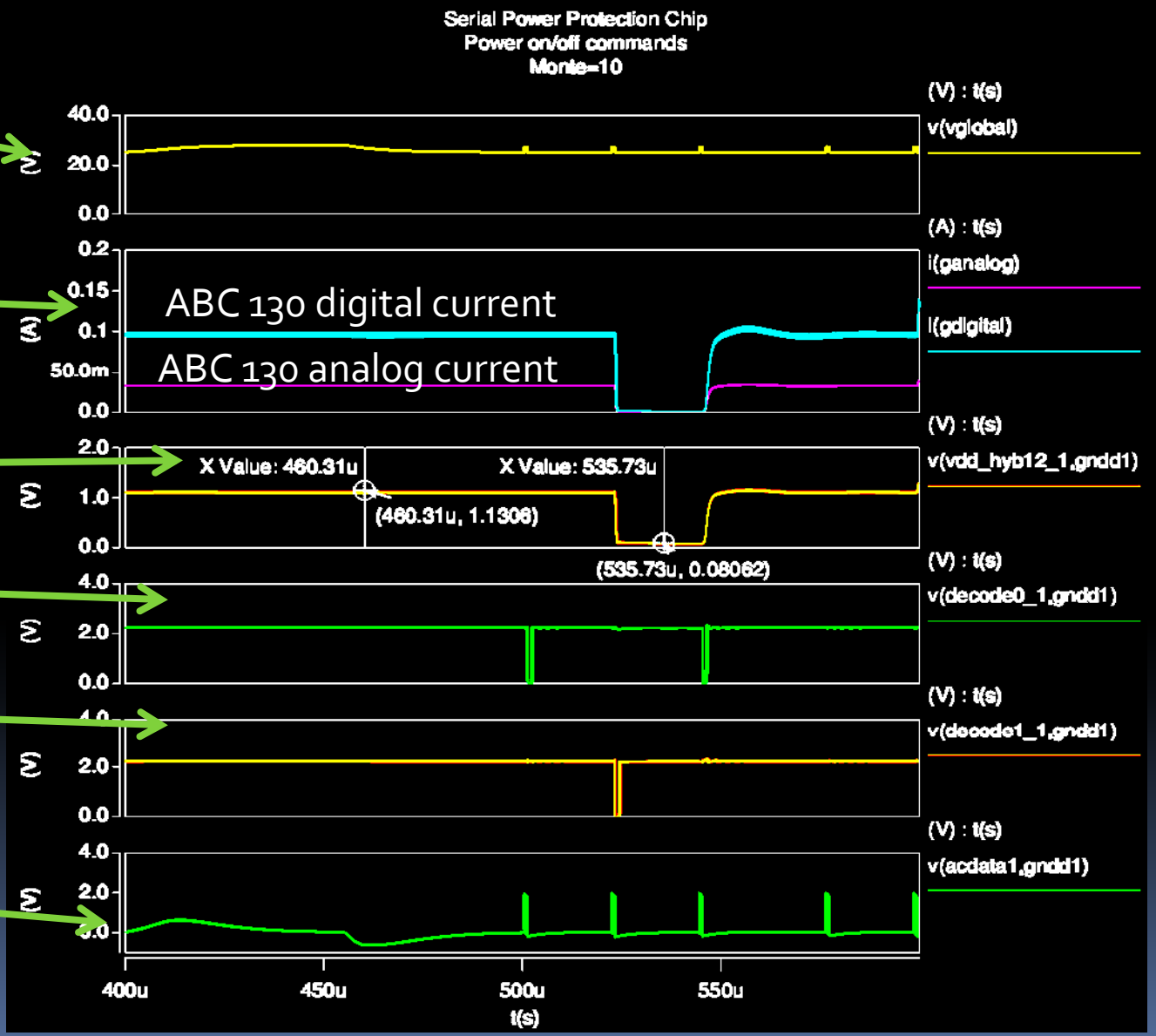
Load Current in one FE IC

Hybrid voltage (1.2v) 80mv when shorted

Decode 0: unshort hybrid

Decode 1: short hybrid

AC coupled pulse-width modulated signal

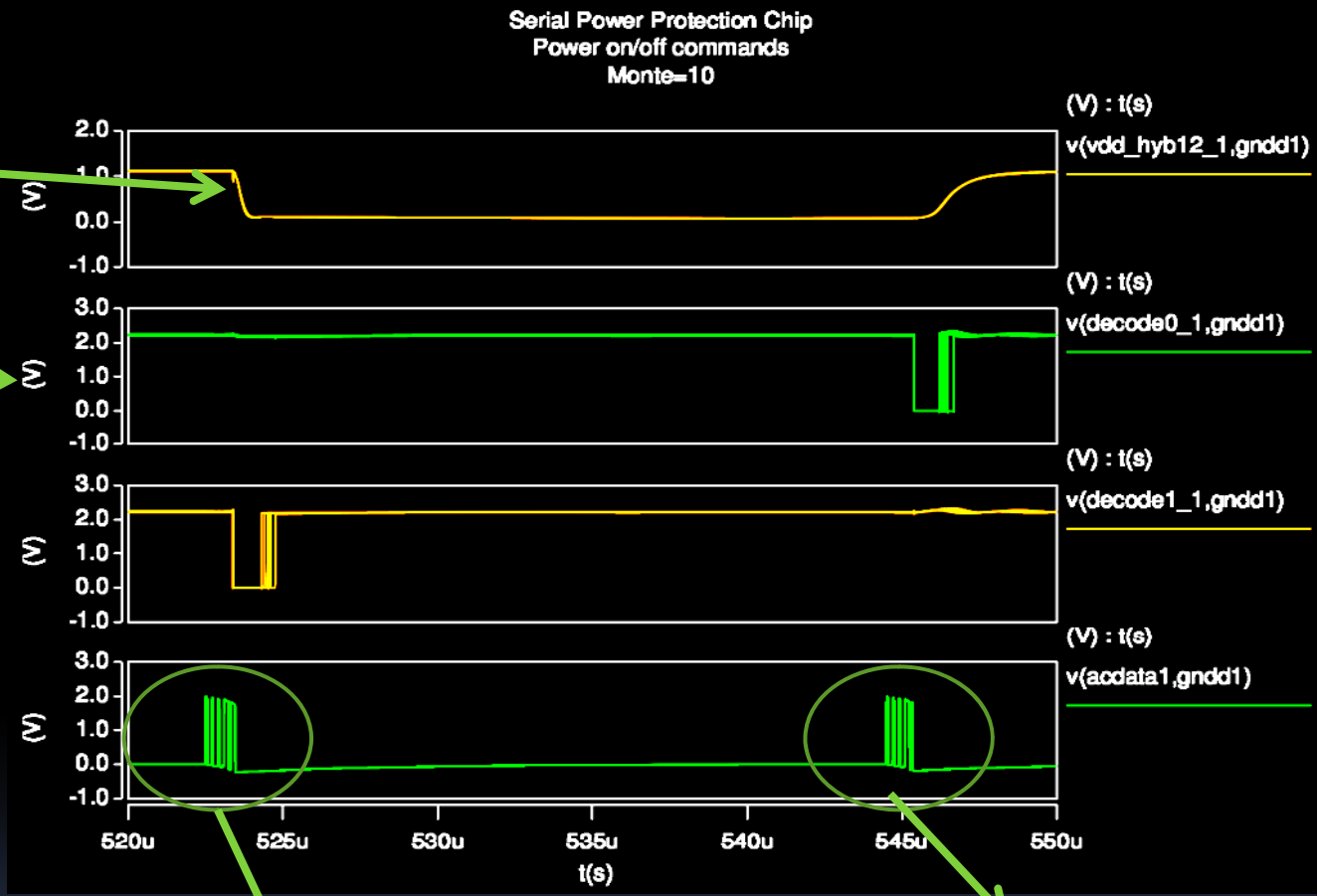


SPP – 12 Hybrid HSPICE simulations (Monte=10)

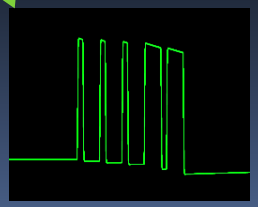
Hybrid voltage (1.2v) 80mv when shorted

Decode 0:unshort hybrid

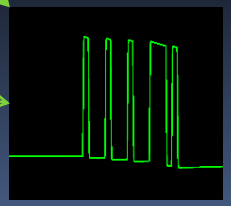
Decode 1: short hybrid



Decode 1: short hybrid

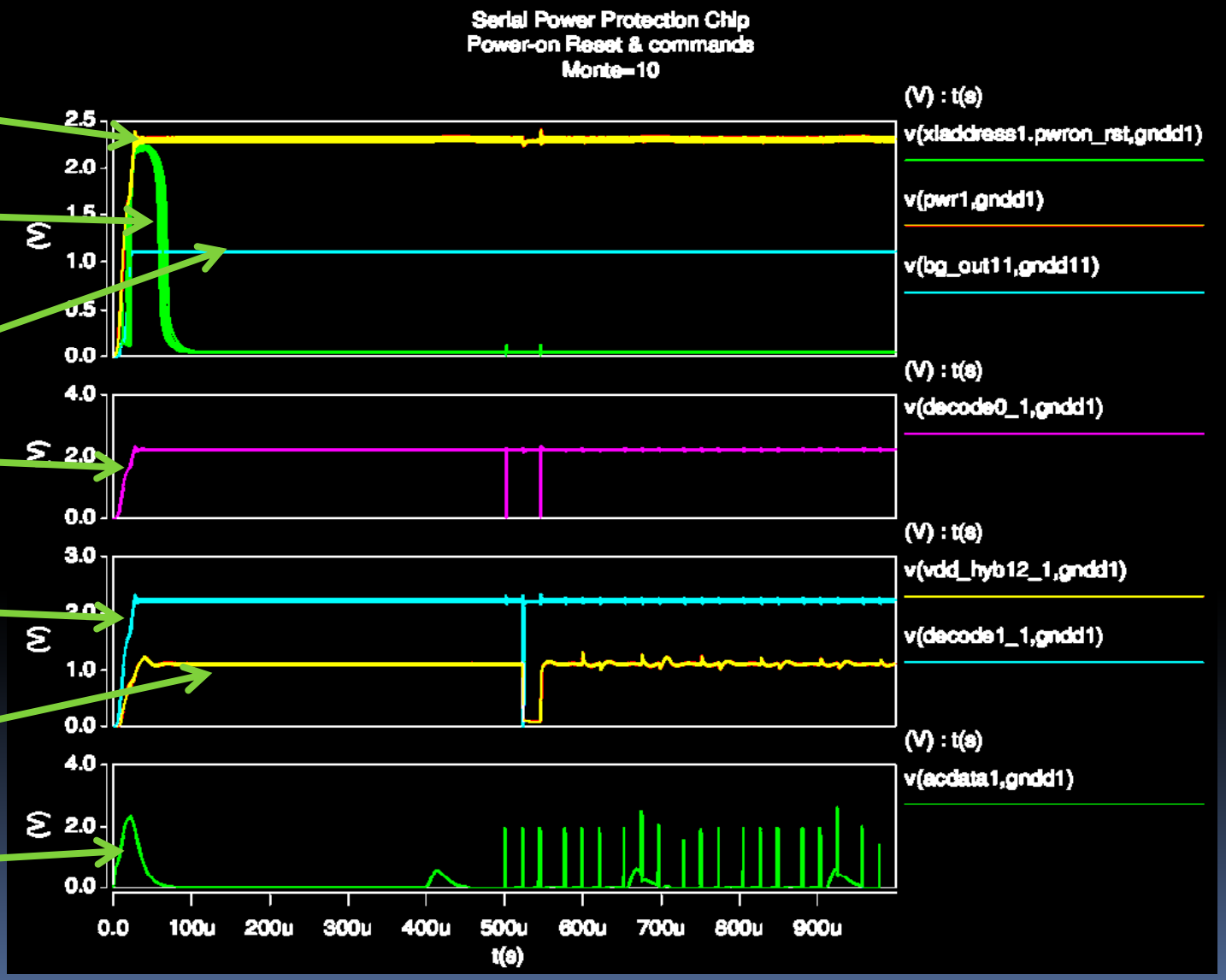


Decode 0: unshort hybrid



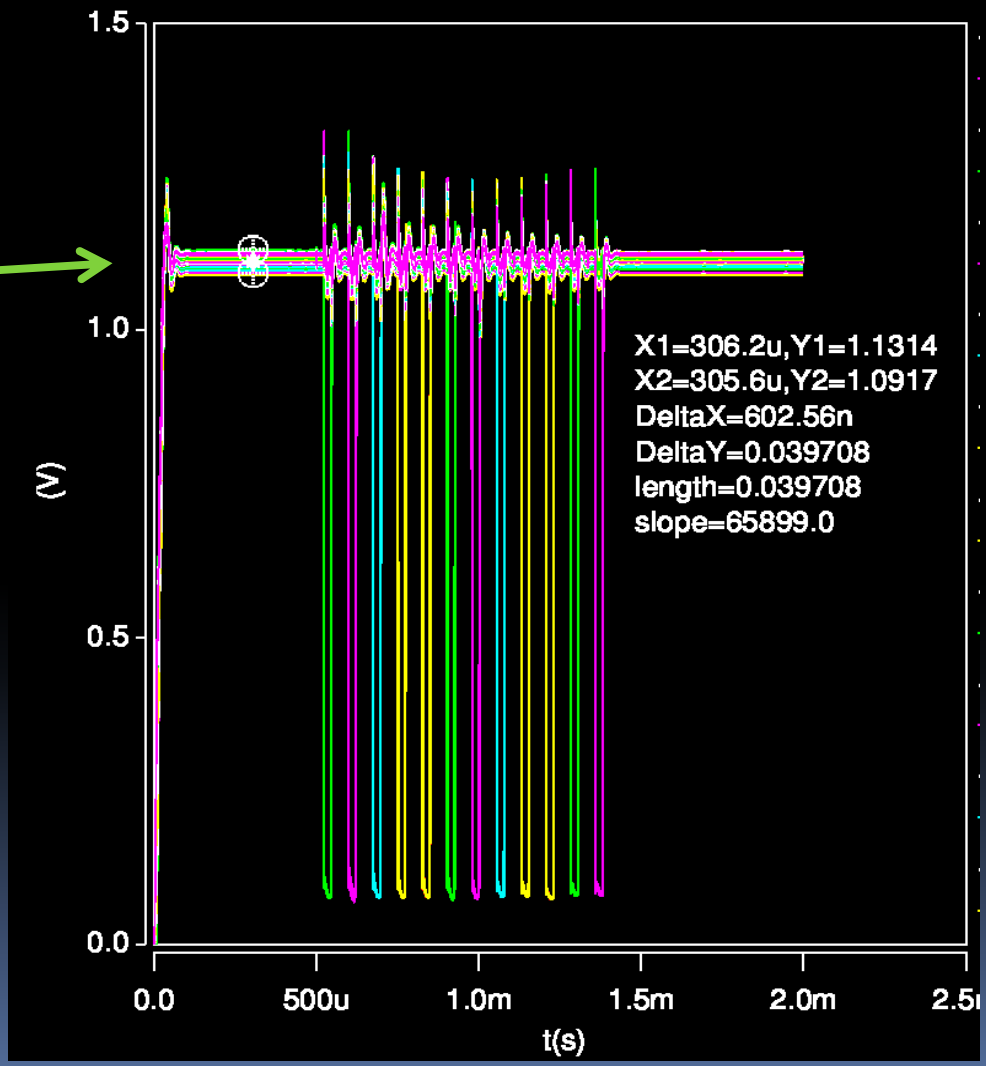
SPP – 12 hybrid HSPICE simulations (Monte=10)

- Vdd hybrid (2.2v)
- Power-on reset
- Bandgap voltage (1.1v)
- Decode 0:unshort hybrid
- Decode 1: short hybrid
- Hybrid voltage (1.2v)
- AC coupled pulse-width modulated signal



SPP – 12 hybrid simulations (Monte=10)

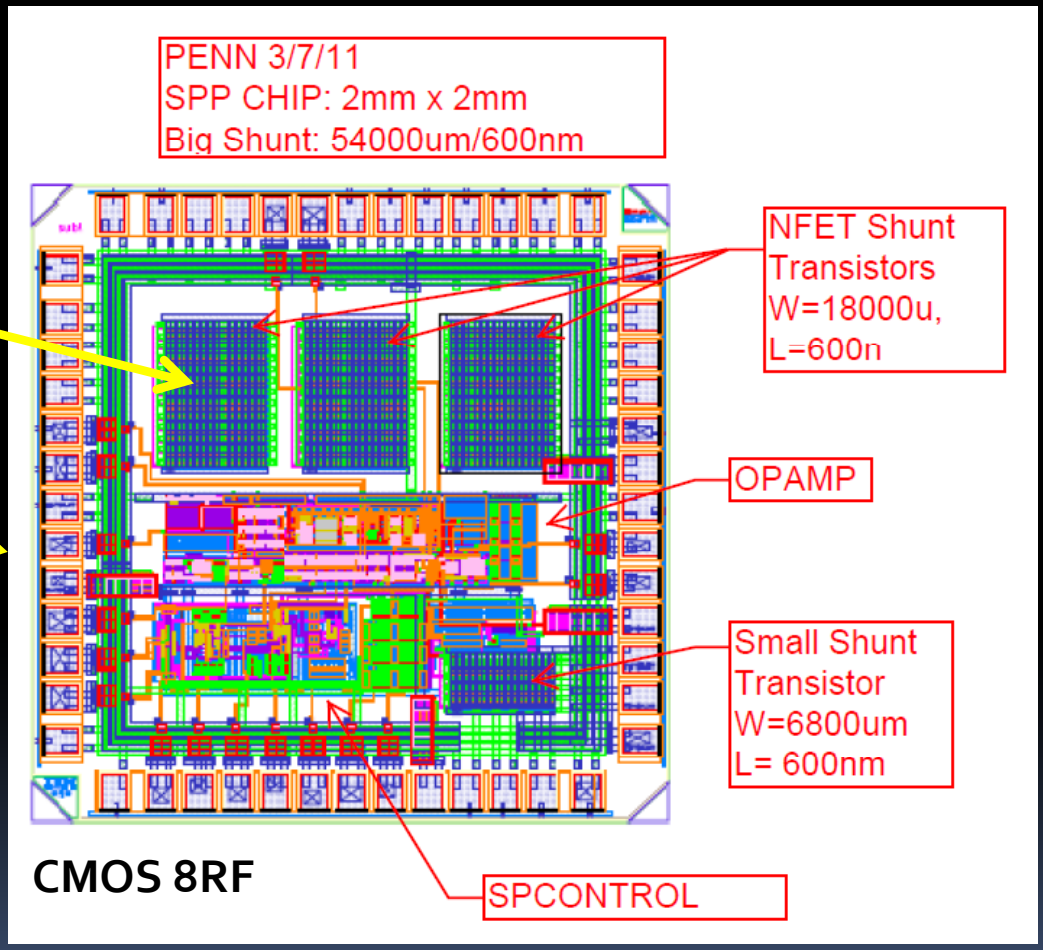
Hybrid voltages: absolute spread over all hybrids <40mV
12 Hybrid Voltages plotted each with shut down and turn on cycle.



SPP full Prototype Chip Layout (2011 submission)

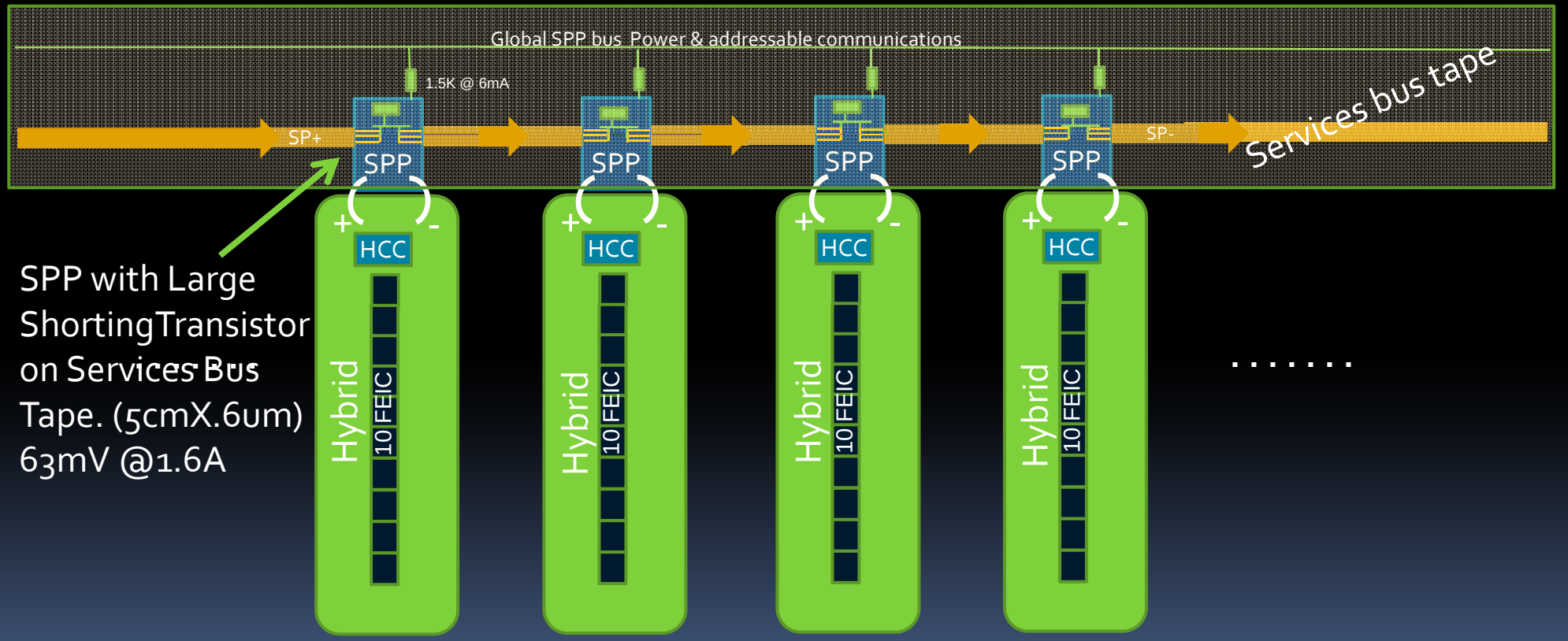
Shorting Transistors
5cm X ..6um Added
63mV @ 1.6A

SPP chip as in 2010



Serial Power Protection and Control

- Single Global power line supplies each SPP with independent power
- SPP is addressable to turn "on" and "off" a hybrid.
- Built in Transistor capable of shunting hybrid current Independent of ASIC based Shunt Transistors



Summary

- **Serial Powering shown to be successful at the Module and Stave Level.**
- **Current Source operates reliably with a 5A, 2.5V ABCn based Stavelet. (Should be easier to build for a lower current, 1.2V 130nm Chipset.)**
- **One wire protection shown to work with Stavelet. Remote addressing works.**

- **Optimization of G&S underway**
  1. **AC coupled Sensor.**
  2. **AC coupled signaling.**
  3. **Need to study coupling of module Reference to EOS reference to minimize common mode.**

- **Testing of fabricated SPP Control loop including Bandgap, Opamp and hybrid regulation will start in a couple of weeks. Results will feed into submission of first complete SPP ASIC. Expected in Q2 2011**