Switched Capacitor DC-DC in FE-I4

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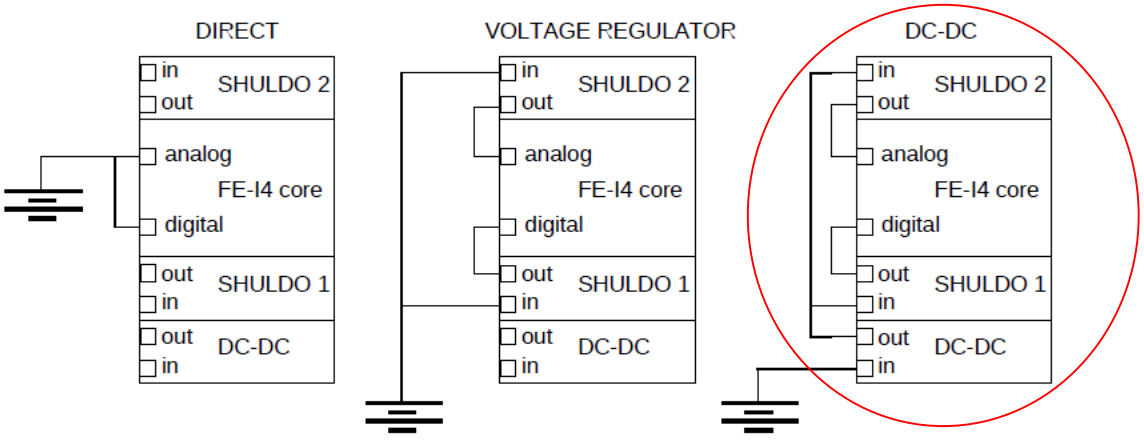
FE-I4 Introduction

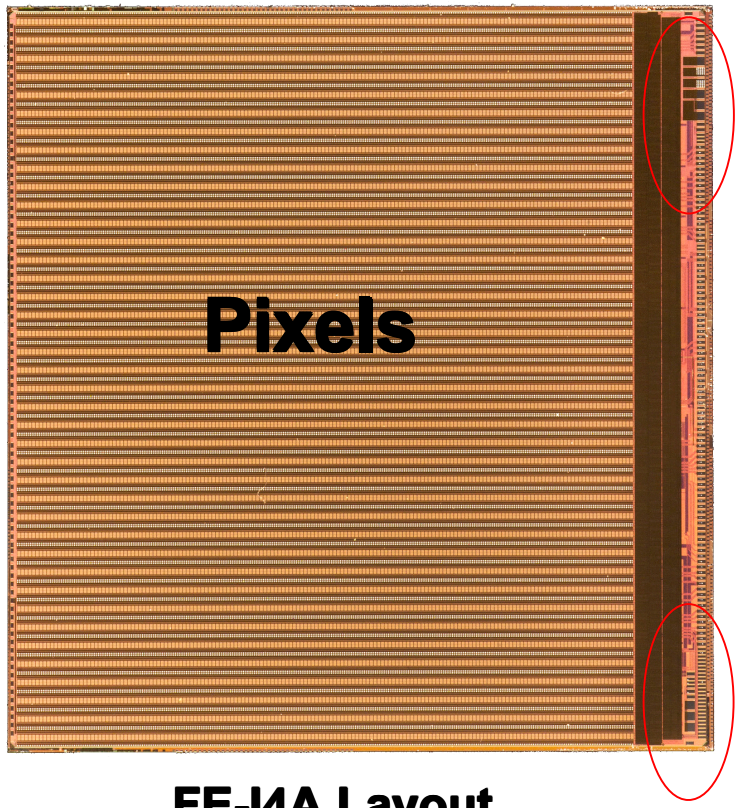
- Designed in a 130nm feature size bulk silicon process.
  - Chip size: 2cm×1.9cm
  - Pixel array: 80col×336row (26,880 pixels)
  - Pixel size: 250um×50um
  - For each pixel: free running CSA + shaping + discriminator
  - Sophisticated digital logic porcessing "firing time" and "time over threshold(TOT)" of each pixel, and transmitting data out of the chip via a pair of 160Mb/s differential signals.

Power Options for FE-I4

- Basically the power rail inside FE-I4 are devided into 4 groups and attached to seperate pads:
  - VDDD1/GNGD1, VDDD2/GNDD2, VDDA1/GNDA1, VDDA2/GNDA2
  - In addition dedicated power nets for PLL, EFUSE and T3 isolation as well.
- 3 isolated power modules in the chip.
  - Two linear-shunt LDOs(ShuLDO)-> **Laura's talk.**
  - One switched capacitor DC-DC converter-> **this talk.**
  - Neither is hard-wired inside the chip. Thus Wire connections outside the chip needed.



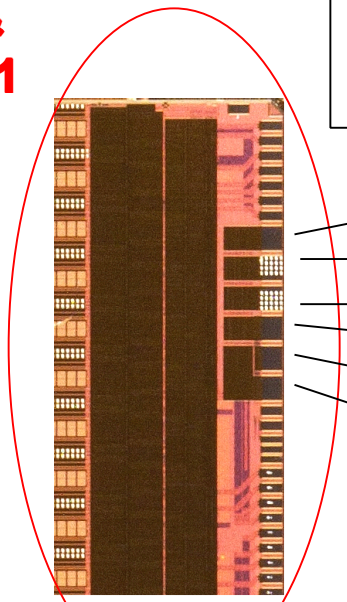
Power Modules in FE-I4 Layout



FE-I4A Layout

DC-DC & ShuLDO1

ShuLDO2

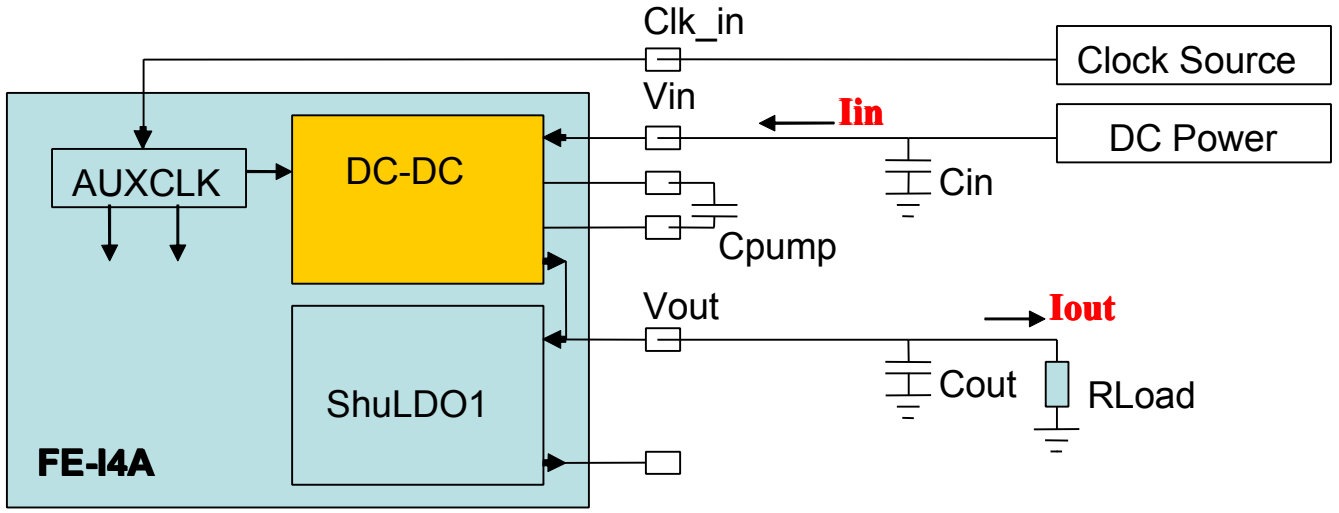


250um pads for power modules while 100um pads for signals

DCDC_IN
Cpump1
Cpump2
REG1_IN
REG1_OUT
REG_GND

Magnification of DC-DC & ShuLDO1

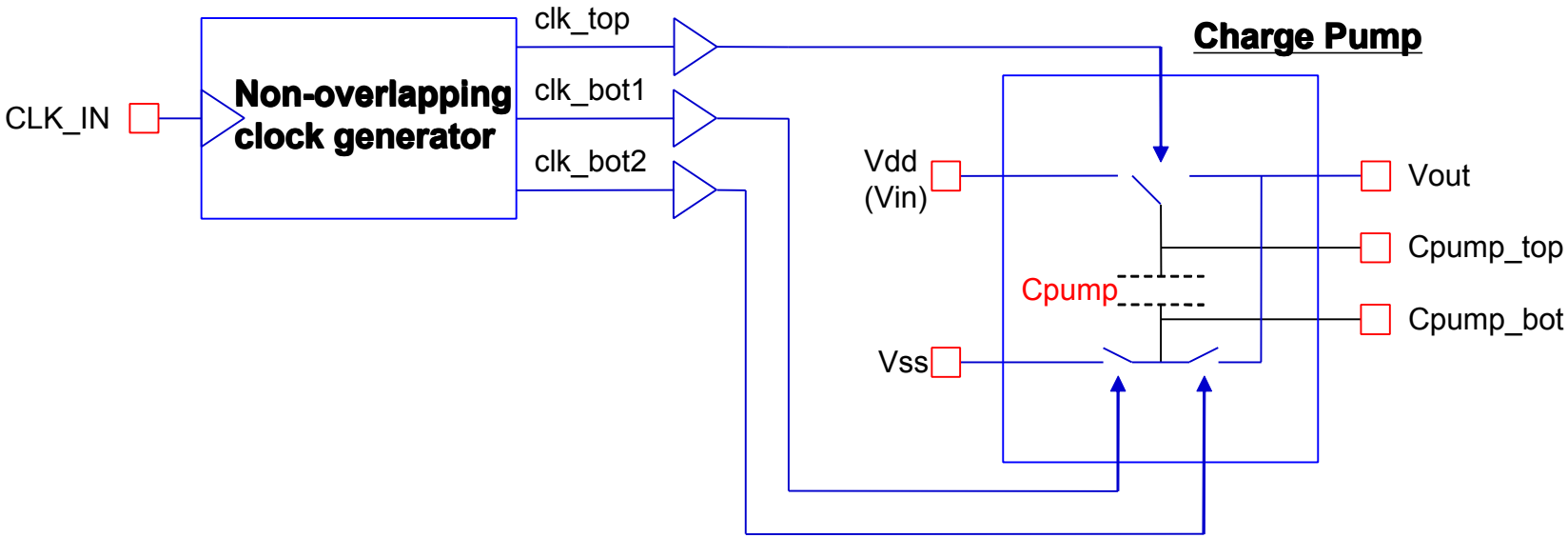
DC-DC configuration in FE-I4



- CLOLK is provided from outside the chip. This clock also serves as auxiliary clock for the chip.
- Ceramic capacitors used for the test. Cpump is mounted on the board as close to the chip as possible.
- DCDC_OUT and ShuLDO1_IN are connected in the chip and share the same pad.
- As a "devide-by-two" converter, ideally: Iout=2Iin & Vout=Vin/2.

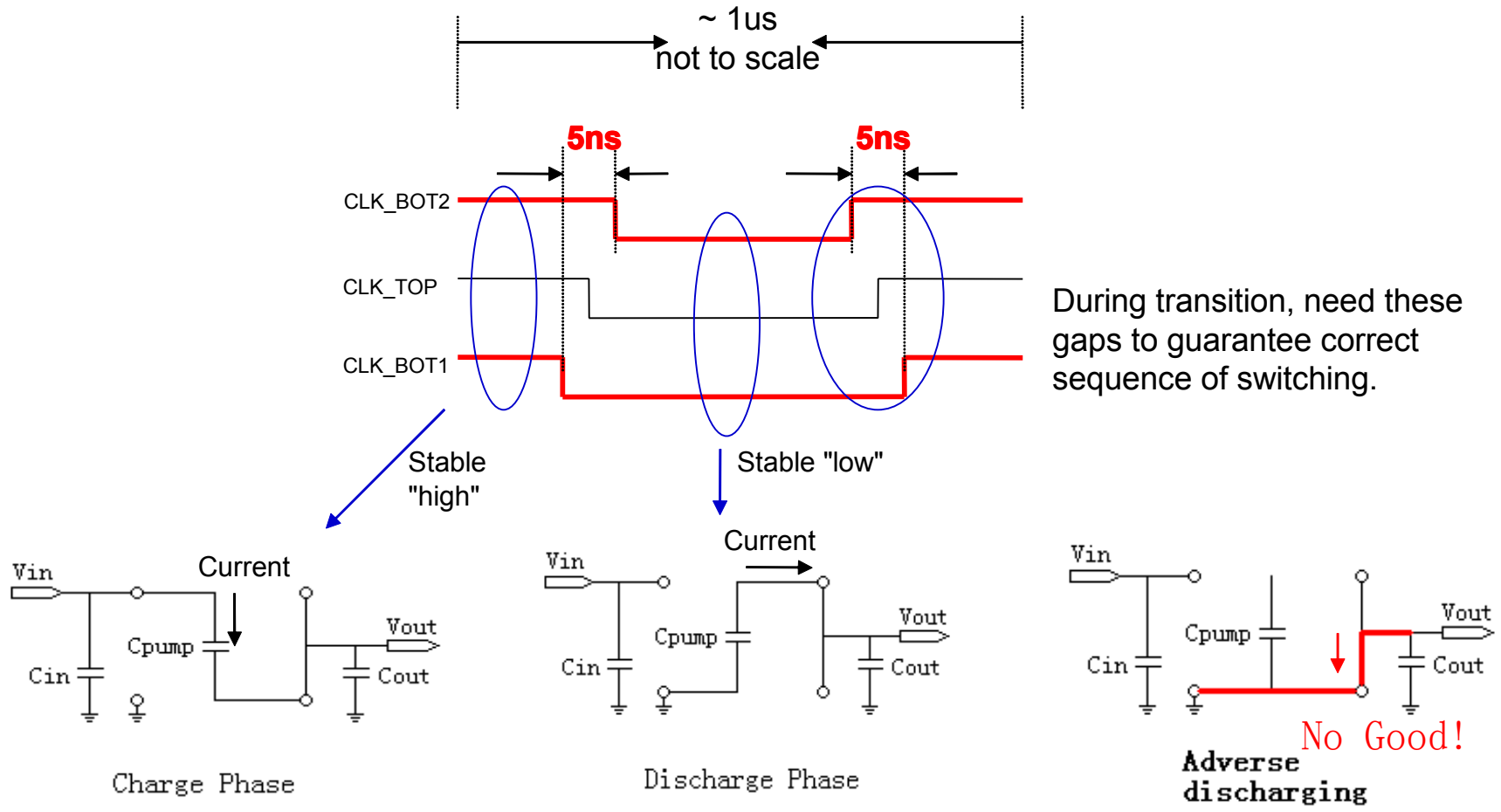
DC-DC Schematic Diagram

- Non-overpapping Clock generator:
  - generates 3 internal clock signals from CLK_IN
  - the same frequency but different phase.
- Charge pump:
  - consists of 4 transistors working as switches
  - manipulates the pump capacitor under control of clock signals.



Non-overlapping clocks

- 5ns gap between CLK_BOT1 and CLK_BOT2 to eliminate adverse discharging.

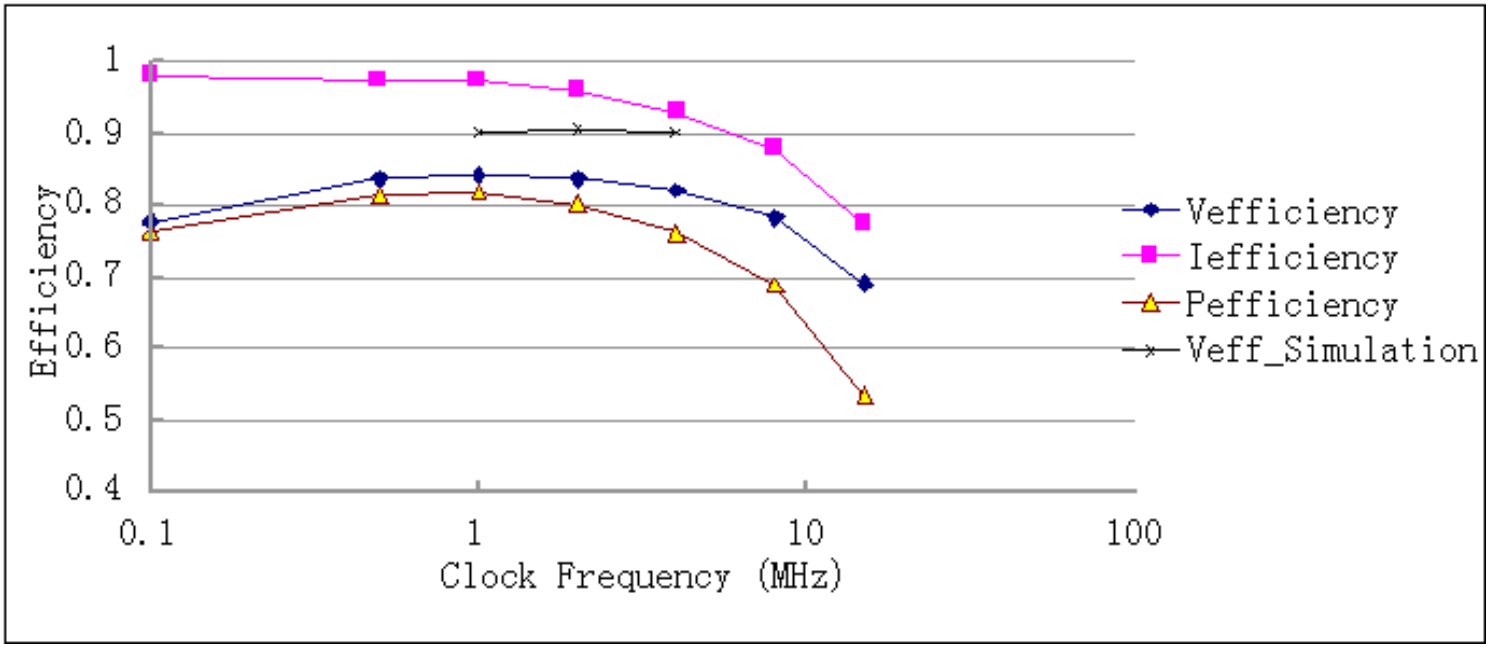


During transition, need these gaps to guarantee correct sequence of switching.

Testing Results

Efficiency vs Clock frequency

Vin=3.3V, Rload=5Ω



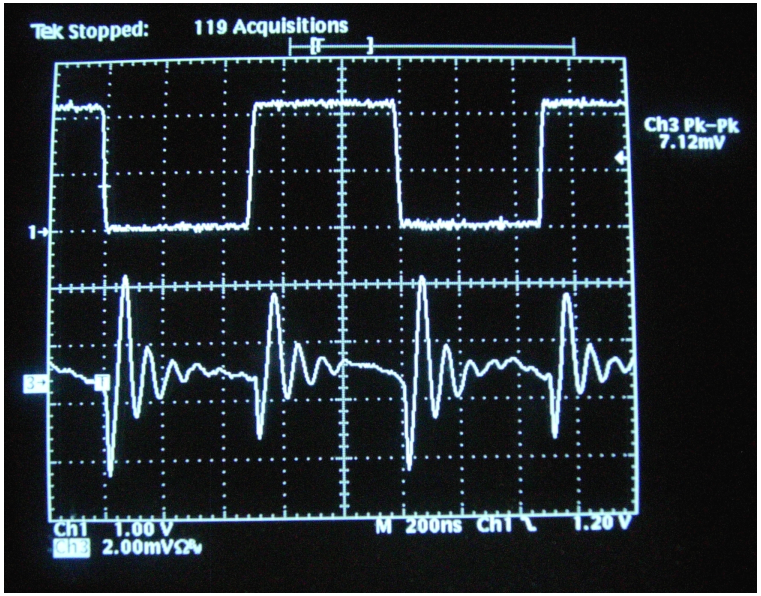
- Simulation result shows Vefficiency around 90%, while the test result shows Vefficiency of about 84%.
- Just take 1MHz as the optimal frequency for the following test.

Ripple Voltage

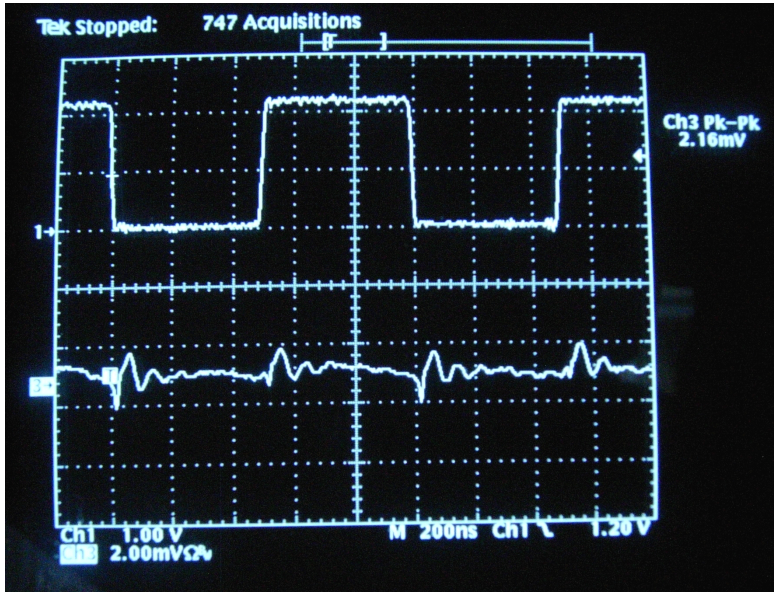
- Observed ripple voltage was much larger(7mV) than the value predicted by simulation(<1mV).
- Its amplitude depended on load current(as shown in pictures below).
- We can't regenerate comparable ripple voltage by simulation. Still can't understand it by now.

Clock, 1MHz →

DC-DC output →
AC coupled



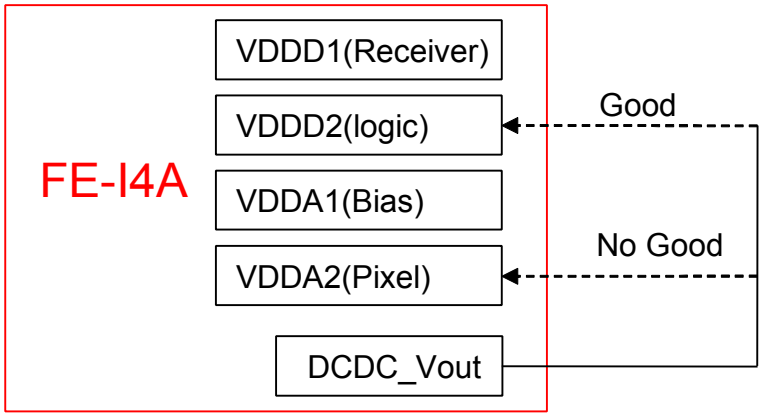
250mA Load Current

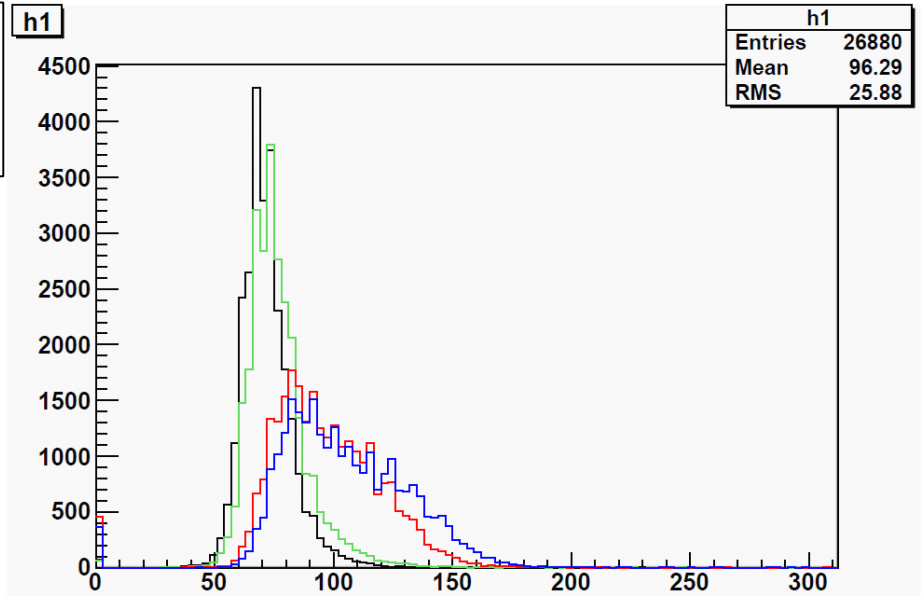


84mA Load Current

Noise in Threshold Scan

DC-DC powering analog-->Noise increased;
DC-DC powering digtal--> Noise seemed good;





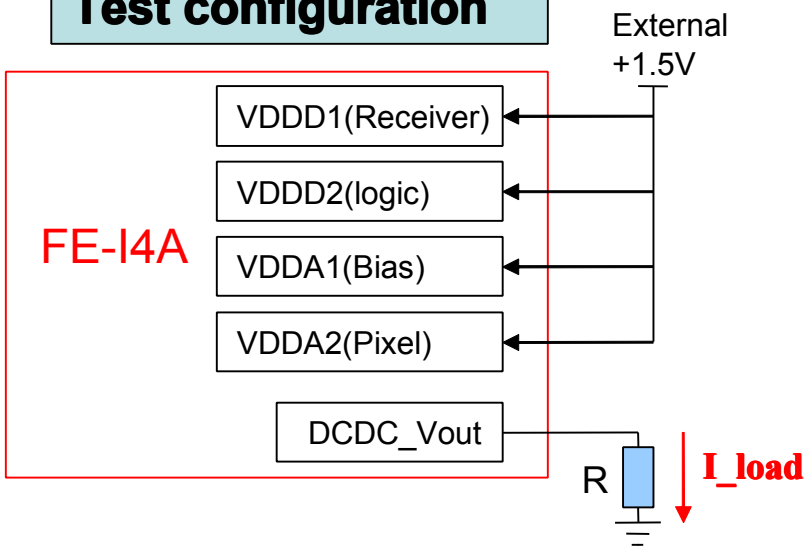
Power Scheme	Noise(e-)	Total Current(mA)
External_Power	72	396
DCDC_VDDD2	76	356+27=383
DCDC_VDDA2	96	121+148=269
DCDC_ (VDDA2+VDDA1+VDDD2)	104	76+169=245

Is it safe to say:
good for digital, but not good for analog?

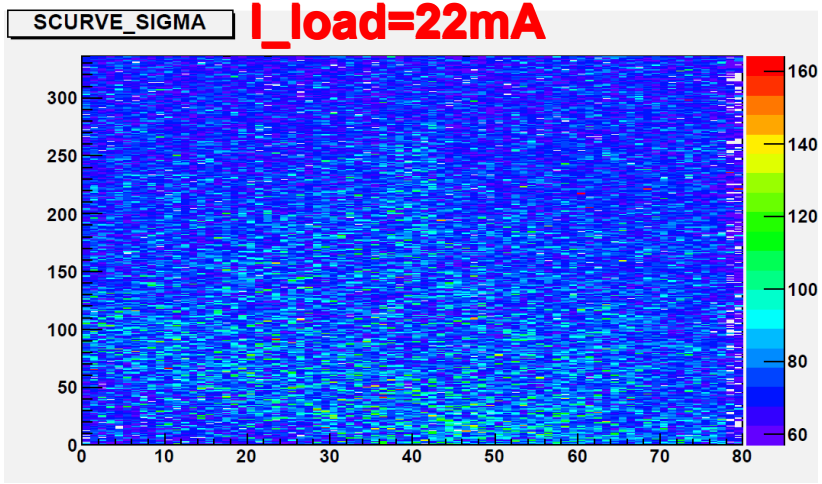
Well, it depends...

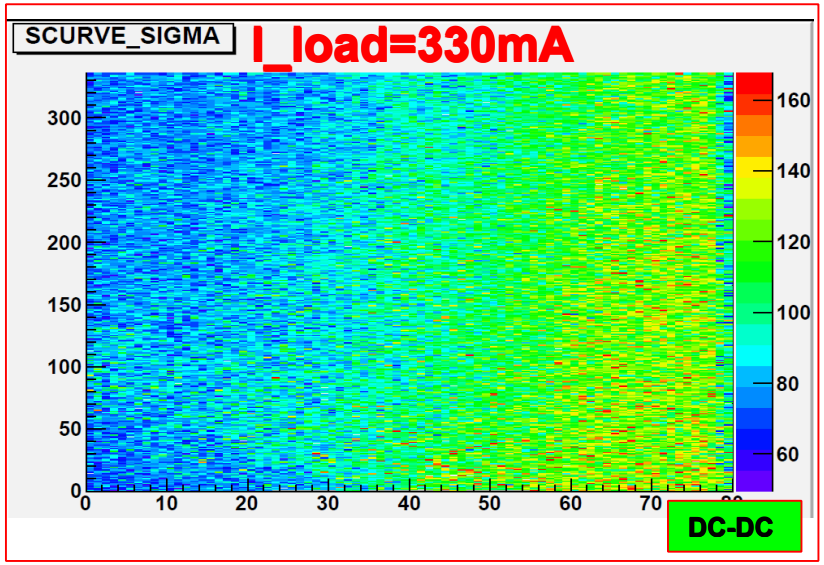
Effect of running DC-DC standalone

Test configuration



Noise map

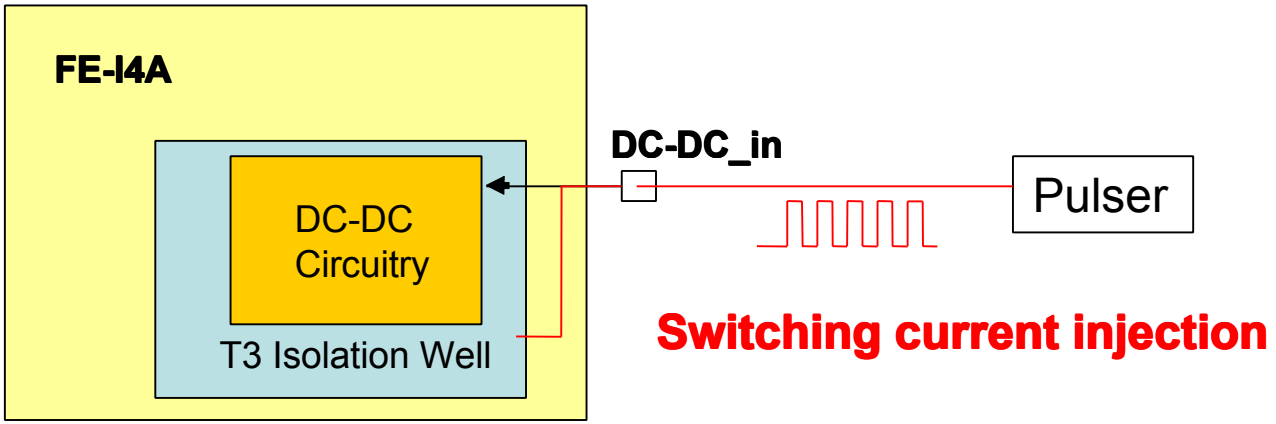




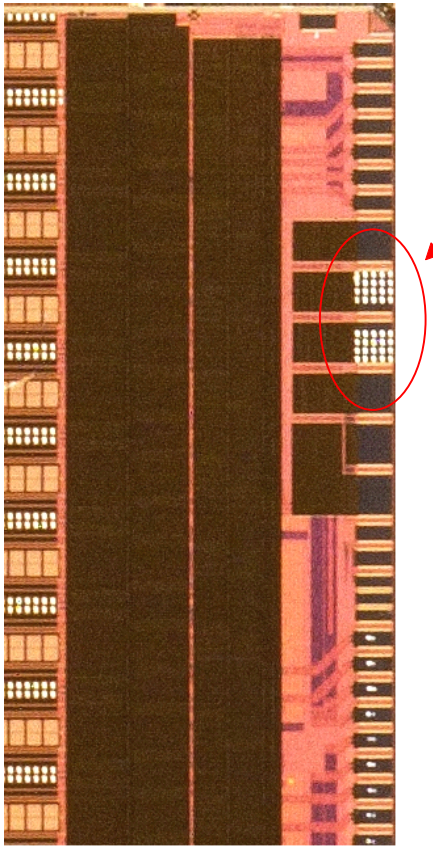
- Running DC-DC but not using it to power the chip.
- Noise depends on DC-DC current.
- Seems like that DC-DC is not well isolated from the rest of the chip as expected.
- To investgate this problem, we made a test shown on next page.

An attempt to inject switching current via DC-DC_T3 isolation well

- DC-DC module sits in a T3 isolation well.
  - which is connected to DC-DC_in.
  - expected to be isolated from the rest of the chip by this way.
- Injecting switching current into the T3 isolation well, to see if noise from threshold scan increased.
- But it doesn't work by far. Two alleged reasons:
  - The current(tens of mA) from the pulser is not big enough.
  - The capacitance between T3 well and substrate smoothed the little switching current.



Follow-up



1. To find out where does the noise come from?
   - Put more efforts into the trial of switching current injection.
2. To put the pump capacitor on the bonding pads
   - smallest package available: "0201";
   - not sure it will work or not since not clear where the noise comes from.
   - should increase operating frequency--minimum of output resistance at higher frequency due to no wire bonds.
3. To make a board to test the irradiated chips.
   - 3 chips irradiated last Dec. and under test now.
   - But no wire bonding for DC-DC can be made on the boards.
   - Plan to make a small board sitting on top of chip. DC-DC will be wire bonded to this board and further attached to wires for test.

- Thanks for paying attention!

Backup Slides

Power Requirments in FE-I4

- 2.2nm gate oxide for all transistors(except for DC-DC converter and EFUSE programming circuitry).
- Thickest gate oxide in the process(5.2nm) used for DC-DC converter and EFUSE programming circuitry.
- The voltage ratings are conservatively estimated according to the gate oxide thickness, area, lifetime, operation temperature, and expected failure rate.
  - 1cm^2 gate area is rated for 1.6V with a 1ppm failure rate after 100KPOH at temperature of 125℃.
  - The benifits from low operation temperature are not included.

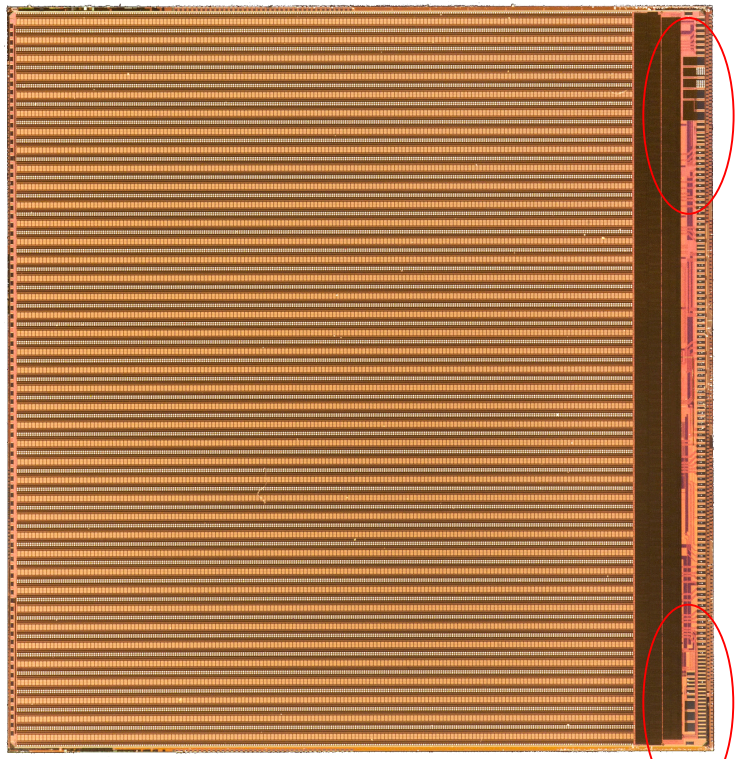
Voltage rating and current consumption

	Internal Nodes	Linear Regulators	DC-DC Converter	Units
Min. operating voltage	1.20	1.30	2.20	V
Max. operating voltage	1.50	1.65	3.40	V
Nominal operating current	0.60	0.60	0.31	A
Max. current at max. voltage	0.90	0.90	0.46	A
Peak transients allowed	1.75	2.00	4.0	V
Max. voltage at power supply[1]	2.10	2.50	4.73	V
Derived R/T drop allowed in cables	0.60	0.85	1.33	V

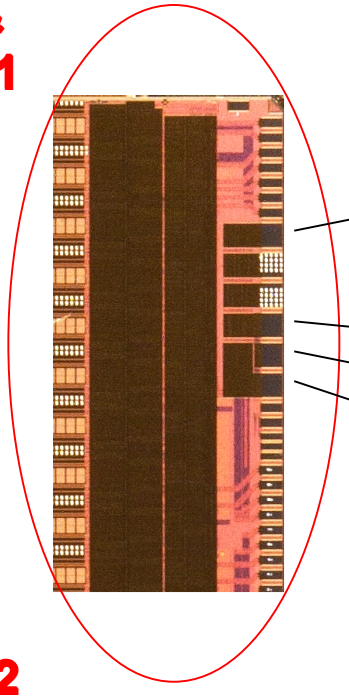
1: The chip will see this voltage minus the cable voltage drop. This limit is chosen under the worst case assumption that a zero voltage drop in the cables can occur.

Switched Capacitor DC-DC

- Merits of switching capacitor DC-DC:
  - converting "high volatege low current"(good for power cables) to "low voltage high current"(required by front-end electronics);
  - using capacitors for energy storage benifits from the the industrial trend of high capacity small shape capacitors(and therefore decreasing mass).
- Pending questions:
  - Noise imposed upon the analog part when integrated into the same chip.
  - Power efficiency degraded by irradiation, about 10% observed on a prototype.



DC-DC & ShuLDO1



250um pads for power module

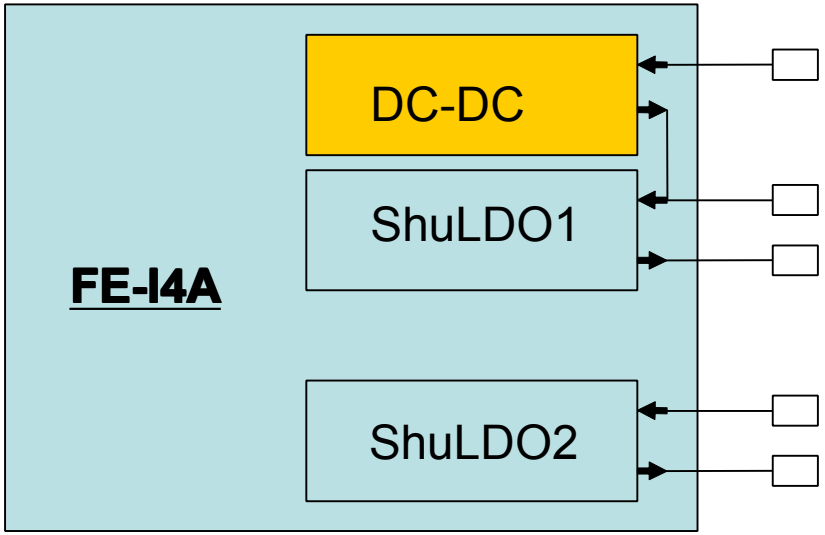
DCDC_IN

REG1_IN

REG1_OUT

REG_GND

ShuLDO2



DCDC_IN

DCDC_OUT& REG1_IN

REG1_OUT

REG2_IN

REG2_OUT

DCDC_OUT and REG1_IN are connected internally and share the same pad. The same way with DCDC_GND and REG1_GND.

Charge pump core schematic