Shunt-LDO in FE-I4

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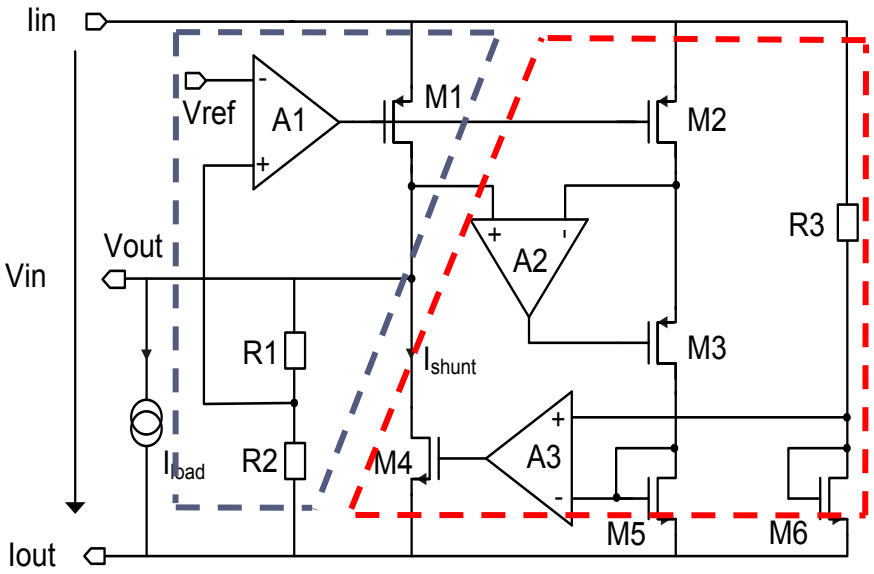
ATLAS-CMS Power Working Group, 08/02/2011

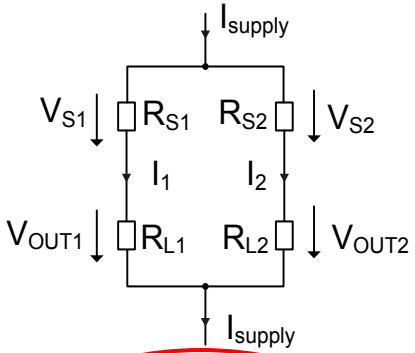
Shunt-LDO reminder

Combination of a LDO and a shunt transistor

Shunt-LDO: simplified schematic



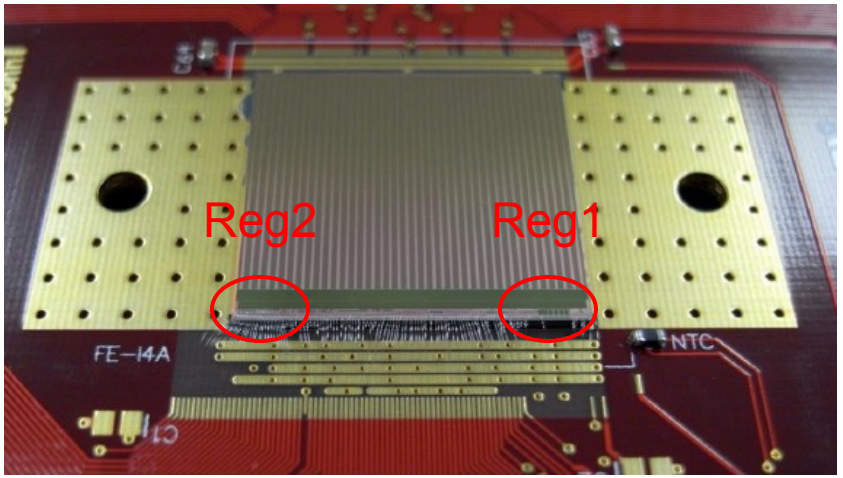
2 Shunt-LDOs in parallel: equivalent circuit



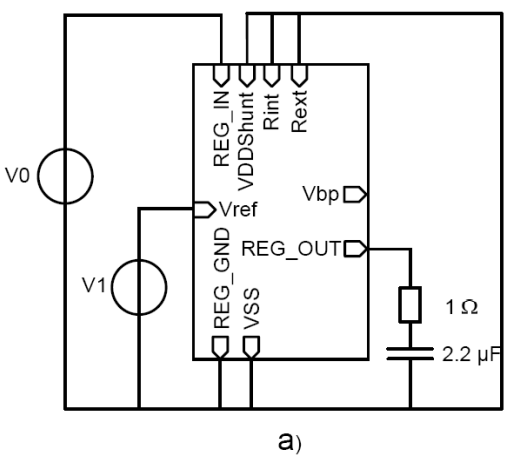
→ Shunt-LDO can be placed in parallel without problems due to mismatch
→ Shunt-LDO with different V_{out} can be placed in parallel
→ Shunt-LDO can cope with increased I_{in}
→ Normal LDO operation when shunt circuitry is off

Shunt-LDO in FE-I4

- 2 shunt-LDO regulators in FE-I4
  - Reg1 input connected to DC-DC output
  - Reg2 independent
- Biasing currents generated internally
- Vref has to be provided externally
- Rint, Rext, and VDDShunt connection selectable to configure the device as Shunt-LDO or LDO

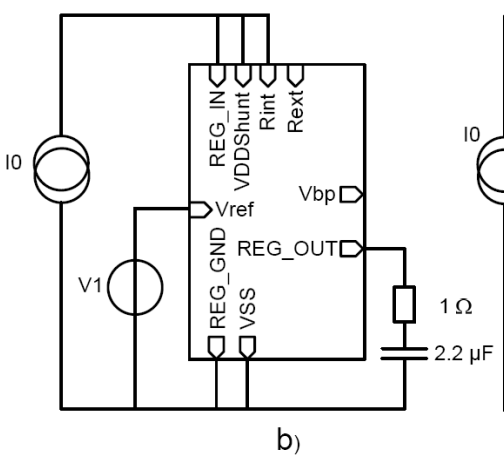


LDO



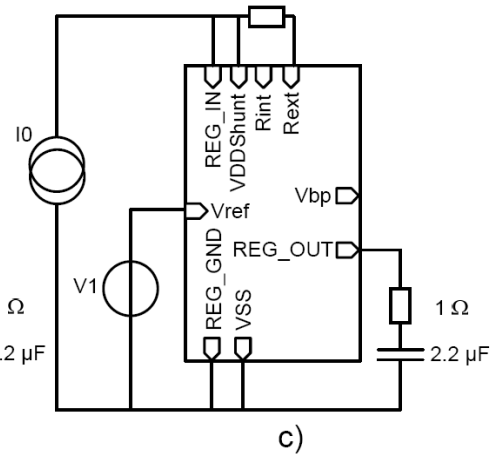
a)

Shunt-LDO with Rint



b)

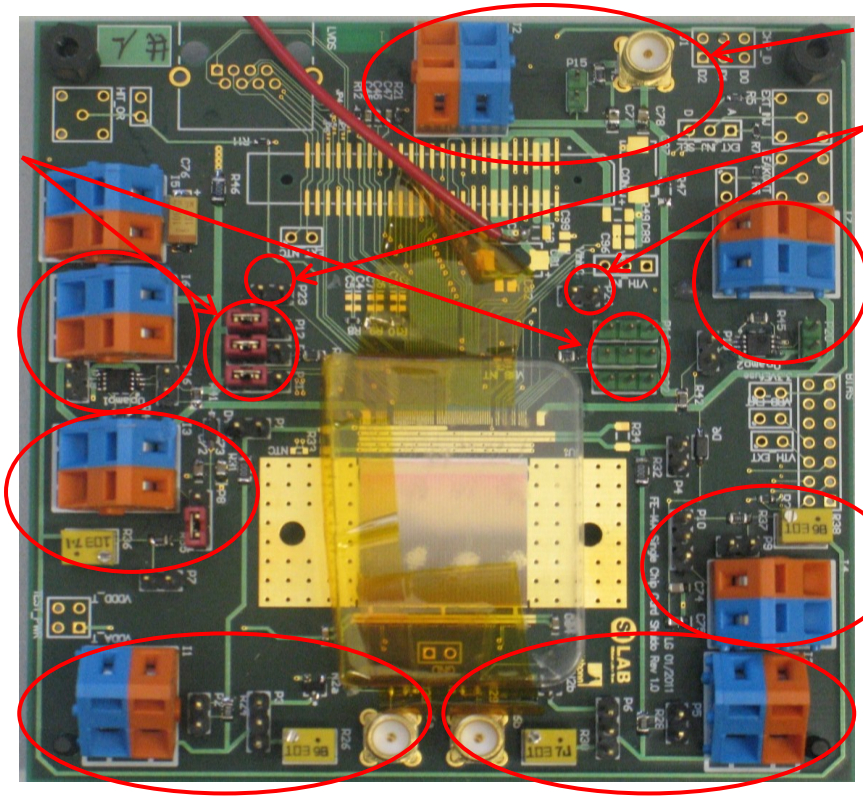
Shunt-LDO with Rext



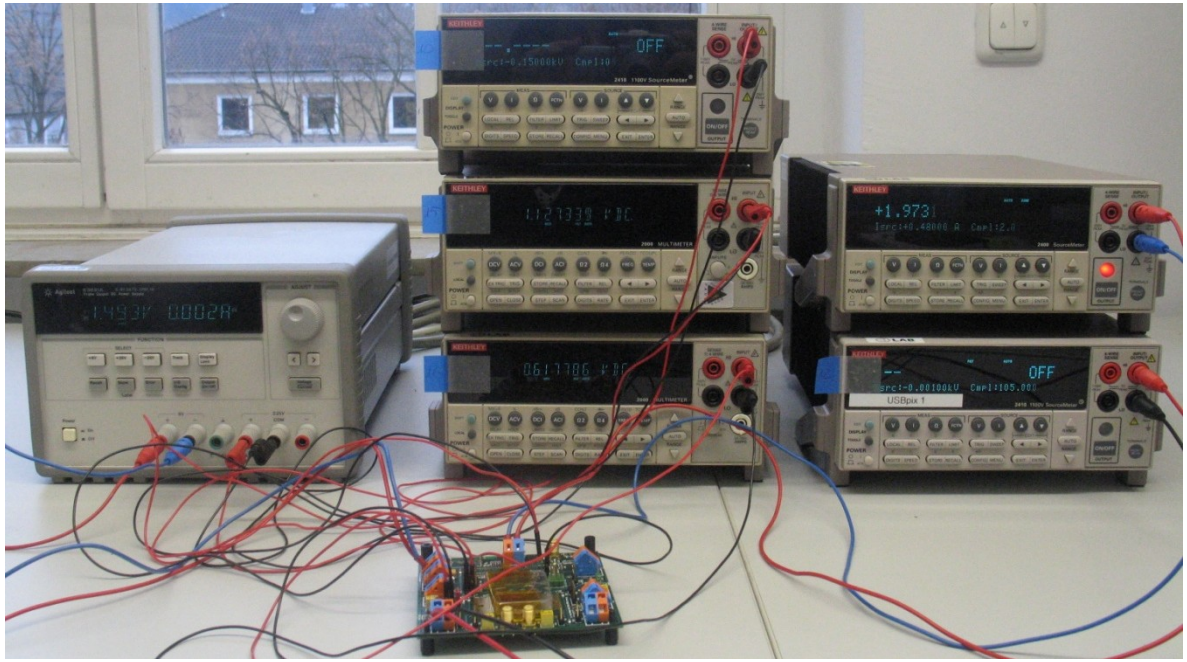
c)

Test board

- Modified FE-I4 SCC allows testing of
  - Both regulators, independently or in parallel
  - FE-I4 with direct powering or Shunt-LDO/LDO powering



Test setup



- For Shunt-LDO characterization
  - Labview software developed by D. Arutinov for Shunt-LDO prototype testing
  - Iin and Iload provided by programmable Keithley sourcemeter
  - Vin, Vout, Vref/Vbp measured automatically using Keithley multimeters
- For FE-I4 characterization
  - USBPix

Test plan & status

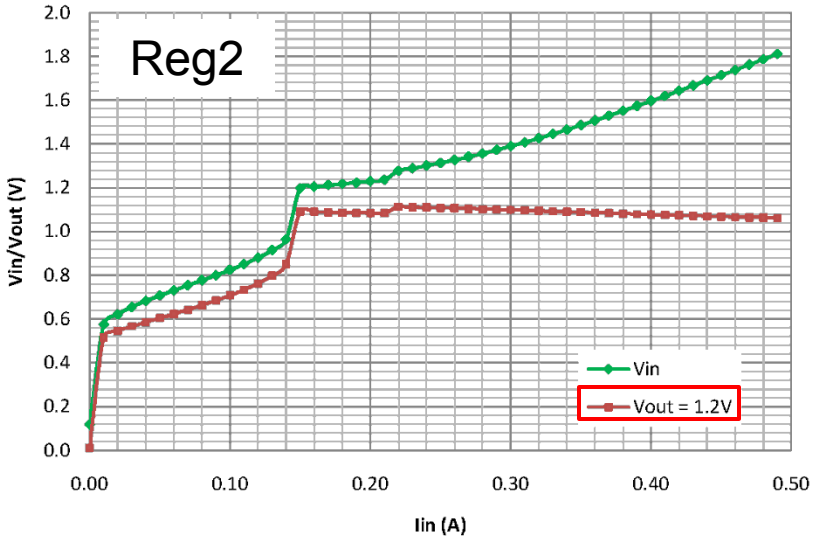
Plan

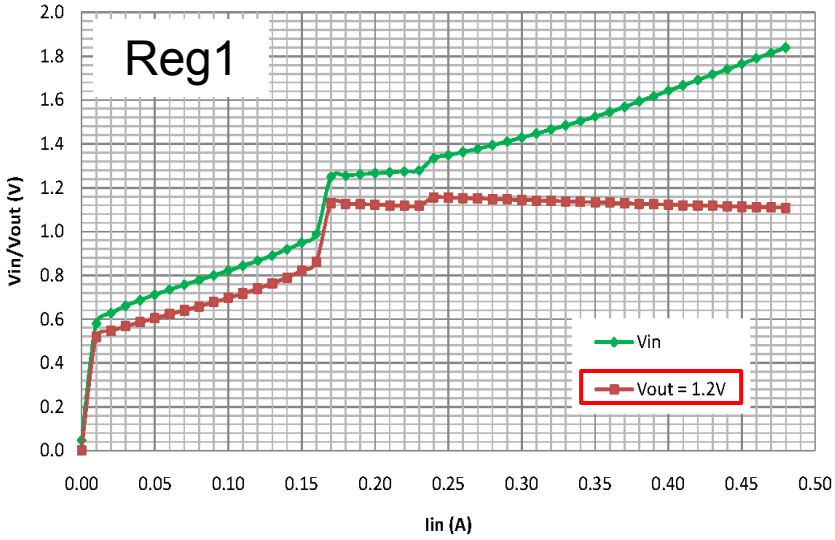
- Tests both regulators in FE-I4 as Shunt-LDO and pure LDO
- Test the 2 Shunt-LDO regulators in parallel
- Test FE-I4 with Shunt-LDO/LDO powering
- Test assemblies with Shunt-LDO/LDO powering
  - New test board needed

Status

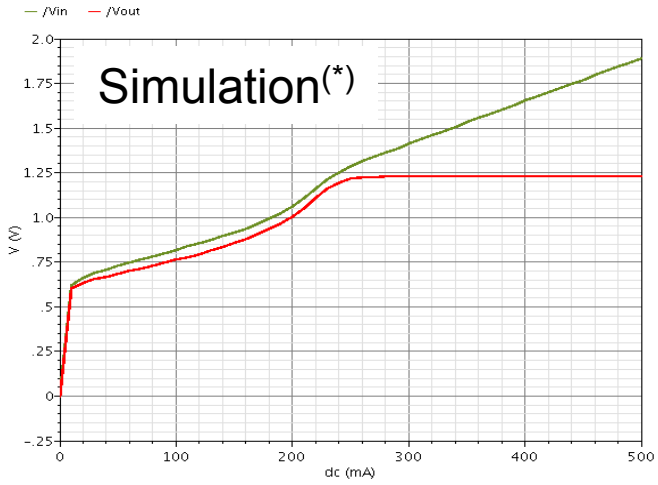
- So far only one chip used for Shunt-LDO characterization
- Focused first on Shunt-LDO characterization
  - LDO characterization just starting
- All results are very preliminary

Shunt-LDO: voltage generation





- Vout reaches the selected value after saturation of the regulator
- Measurement however show differences wrt simulation
  - Abrupt jumps
  - Vout < 2Vref, and decreases with increasing Iin



(*) Shunt-LDO schematics including IO pads

Abrupt jumps investigation

- Dependence on bias: VDDShunt
  - Default connection (in Shunt-LDO mode) to Vin
  - Bias for A3 and for the biasing circuitry
  - Tried to set it to a constant value or connect to Vout

→ no effect on jumps

- Dependence on temperature
  - Board cooled during test

→ no effect on jumps

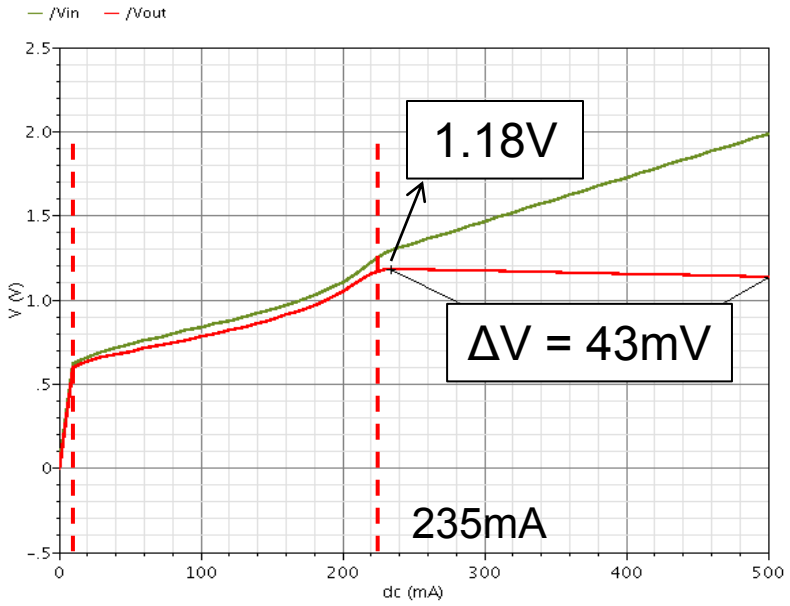
- Still to investigate
  - Parameters variation with MC simulation
  - Offset in mirror current circuit amplifier A2
    - It was shown with the prototypes that this offset influences the distribution of shunt current at start up and that this was linked to the abrupt jump seen in the prototypes

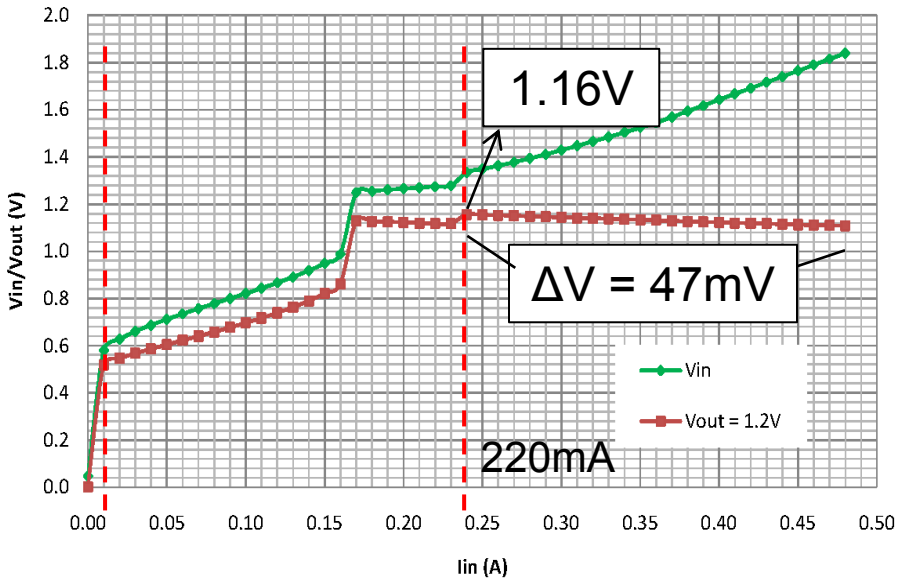
Vout behavior

- Vdrop on the ground line which effectively decreases the Vref
  - Vref referred to the board gnd, Vout(Vin) generated wrt chip gnd and measured wrt board gnd
- Measure gnd difference between chip gnd and board gnd
  - One wire bond between chip gnd pad and measurement point on the board
- Results confirm this hypothesis
- Account for gnd difference in simulation
  - R = 190mOhm between chip gnd and board gnd
    - R value extrapolated from gnd difference measurement

Iin	Vout meas	Vout = 2Vref	2Vref – Vout meas	GND difference
0.25	1.165	1.218	0.053	0.046
0.26	1.163	1.218	0.055	0.046
0.27	1.161	1.218	0.057	0.048
0.28	1.160	1.218	0.058	0.050
0.29	1.157	1.218	0.061	0.052
0.3	1.155	1.218	0.063	0.054
0.31	1.153	1.218	0.065	0.056
0.32	1.151	1.218	0.067	0.058
0.33	1.149	1.218	0.069	0.060
0.34	1.146	1.218	0.072	0.062
0.35	1.144	1.220	0.076	0.064
0.36	1.142	1.220	0.078	0.066
0.37	1.140	1.220	0.080	0.068
0.38	1.137	1.220	0.083	0.072
0.39	1.135	1.220	0.085	0.074
0.4	1.133	1.220	0.087	0.076
0.41	1.132	1.220	0.088	0.078
0.42	1.129	1.222	0.093	0.080
0.43	1.127	1.222	0.095	0.082
0.44	1.125	1.222	0.097	0.084
0.45	1.124	1.224	0.100	0.086
0.46	1.122	1.224	0.102	0.088
0.47	1.120	1.224	0.104	0.090
0.48	1.119	1.226	0.107	0.094

Simulations vs measurement





- Measured Vout behavior can be reproduced in simulation
  - Simulated Vout value and decrease agree with measured ones
- Sim and meas compatible at start-up and after the second jump
  - Second jump seems to correspond to the saturation point
  - Investigations go on to understand the region in between

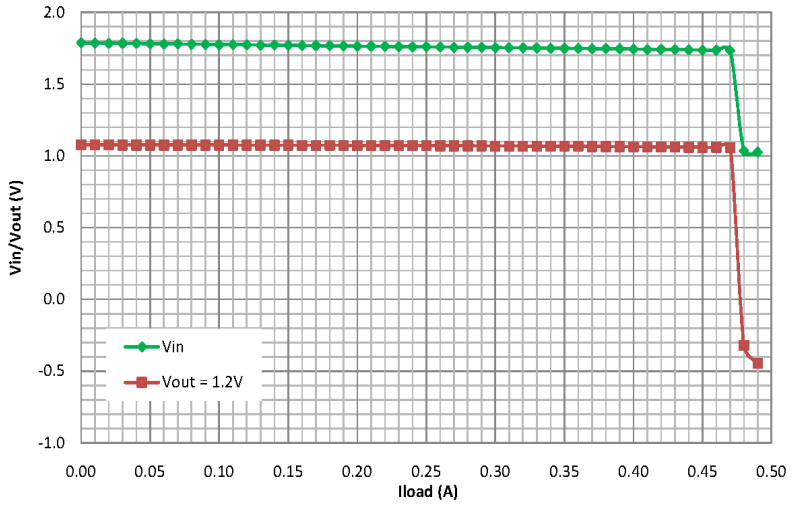
Rin and line regulation

- Correcting for the gnd difference
- Rin = Vin/Iin = ~4.5Ω
  - In agreement with design value (Rin = 4Ω)
- Line regulation = ΔVout/ΔIin(mV/mA)

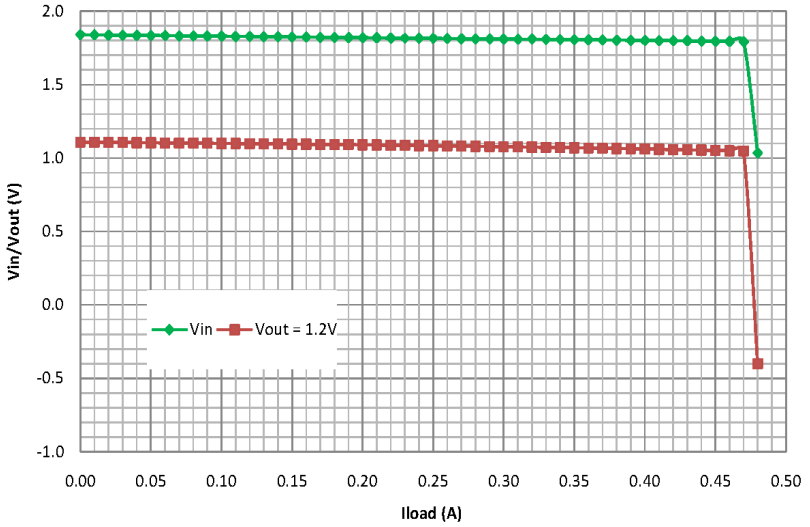
	Vout = 1.2V	Vout = 1.5V
Reg2	1/59	1/30
Reg1	1/40	1/23

Shunt-LDO: load regulation

Reg2



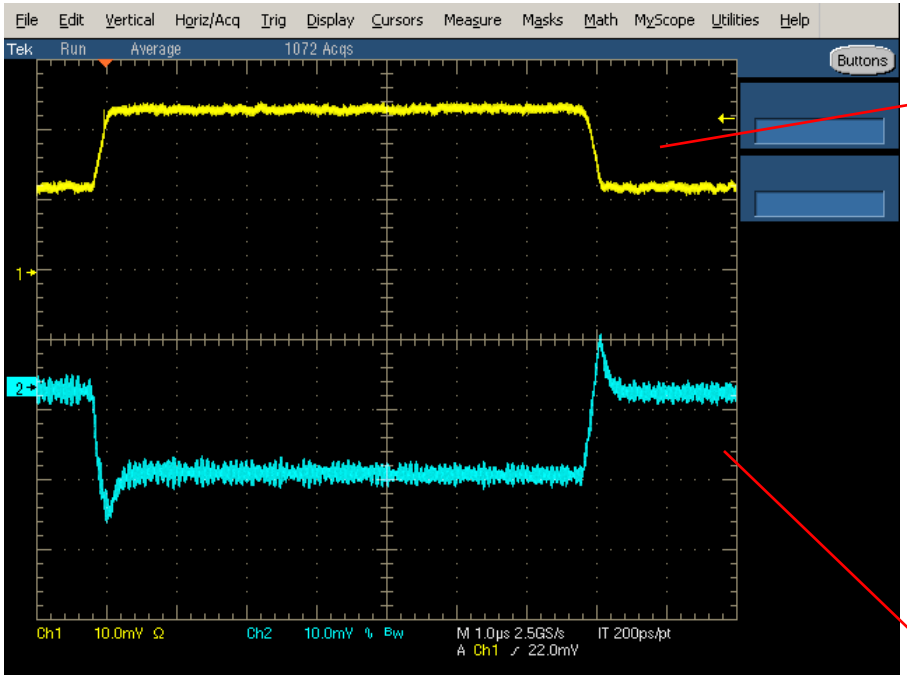
Reg1



- Iin = 480mA
  - The current flowing through the regulator is constant!
  - It splits between the shunt transistor and the load according to the value of Iload
- Vin and Vout are stable until Iload = Iin
- Rout2 = 38mΩ, Rout1 = 128mΩ, including also on-chip wiring, wire bonding, PCB traces
  - Investigate source of discrepancy
  - Extimate influence of wire bonds and PCB traces resistance

Shunt-LDO: load transient

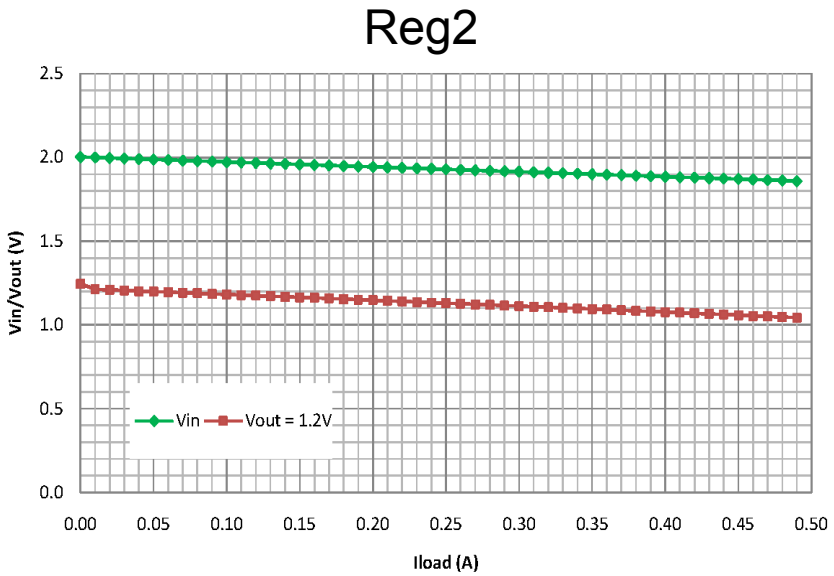
Reg1 only



- Load current pulse of 118mA
  - 11.8mV measured on a 100mΩ resistor
- Rise time 200ns, fall time 200ns
- Pulse width 7us

- Vout changes of 20mV peak to peak
- 12.2mV output change
  - Rout1 ~ 100mΩ. Agrees with value from the load regulation measurement

LDO: load regulation



- Decrease of Vout for increasing Iload due to
  - Rout
  - Increasing ground difference between chip and board gnd
- Rout2 = 217mΩ, including also on-chip wiring, wire bonding, PCB traces
  - Investigate Rout value to extimate the regulator output resistance independently from external contributions

Conclusion

- Both regulators on chip have been operated stand-alone as Shunt-LDO and LDO
- Regulator basic functionalities have been asserted
- The regulator works fine!
- More results to come...

Backup

Specs for LDO in FE-I4

- Line regulation: ΔVout/ ΔVin = 1/20
- Load regulation: ΔVout/ ΔIload = 33mΩ
  - Vin = 1.6V, Vout =1.2-1.5V, Iload(max) = 0.5A