Stability of systems with DCDC converters

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Many thanks to:
G.Spiazzi and S.Buso - Padova University, DEI/PEL
S.Saggini - Udine University
K.Klein and W.Karpinski - RWTH Aachen

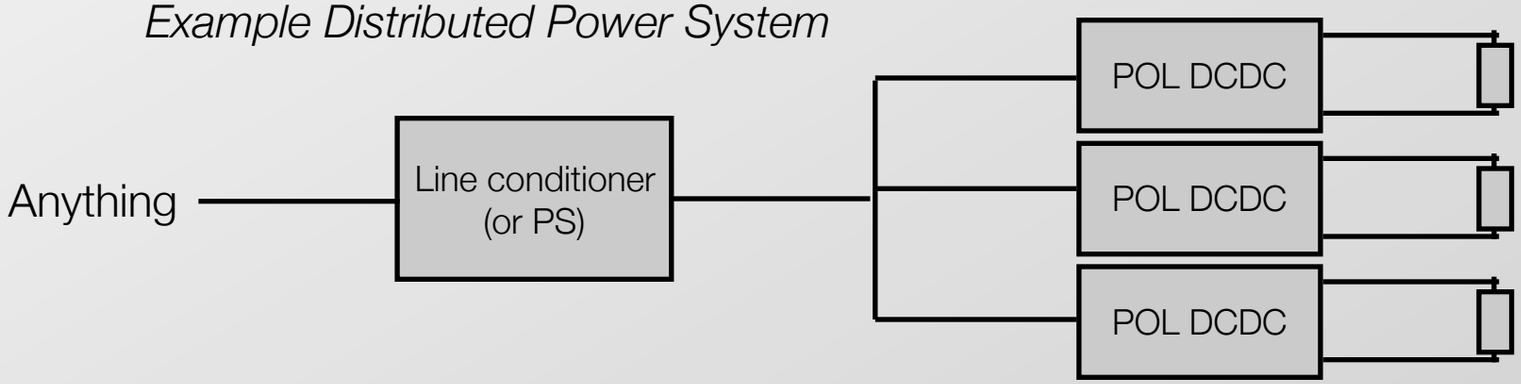
Outline

- DCDC converters' compensation
- Effect of the load impedance
- Effect of the input filter impedance
- Case system study: CMS pixels phase 1 upgrade
- Conclusion

Foreword

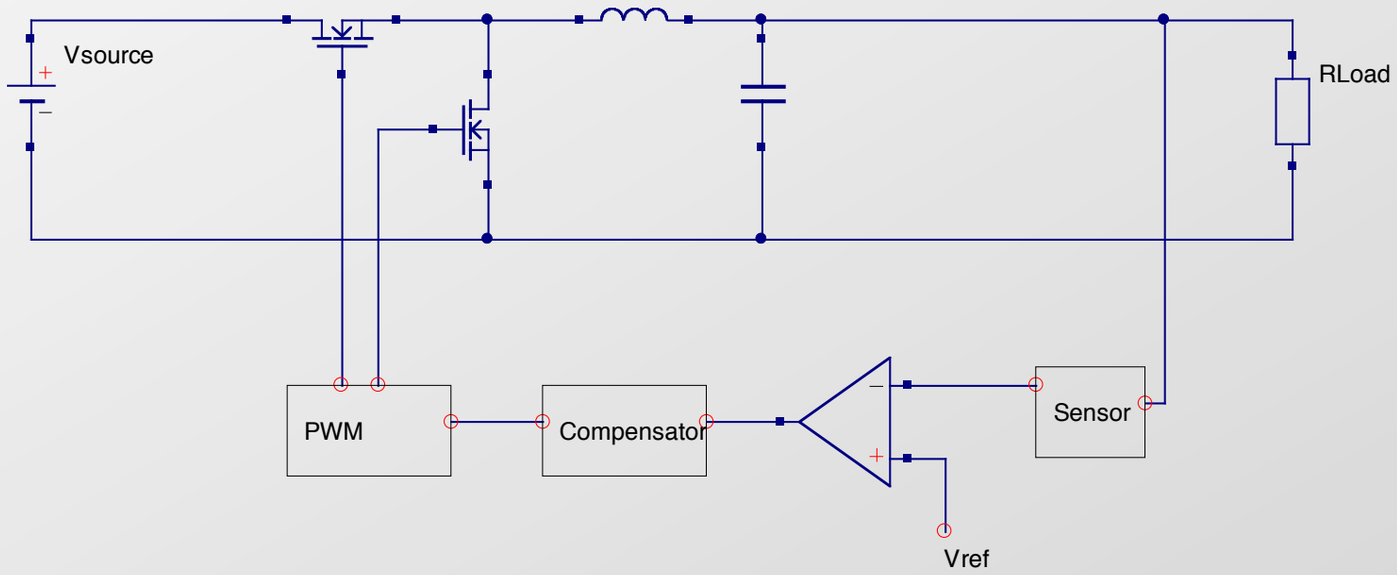
- The generic title “Stability of DCDC converters” is conceptually wrong, but the correct one would have been a little elusive: “System stability issues in the use of Point-of-Load Buck converters”. The stability of the ‘line conditioner’ converter (or Power Supply) will not be discussed

Example Distributed Power System



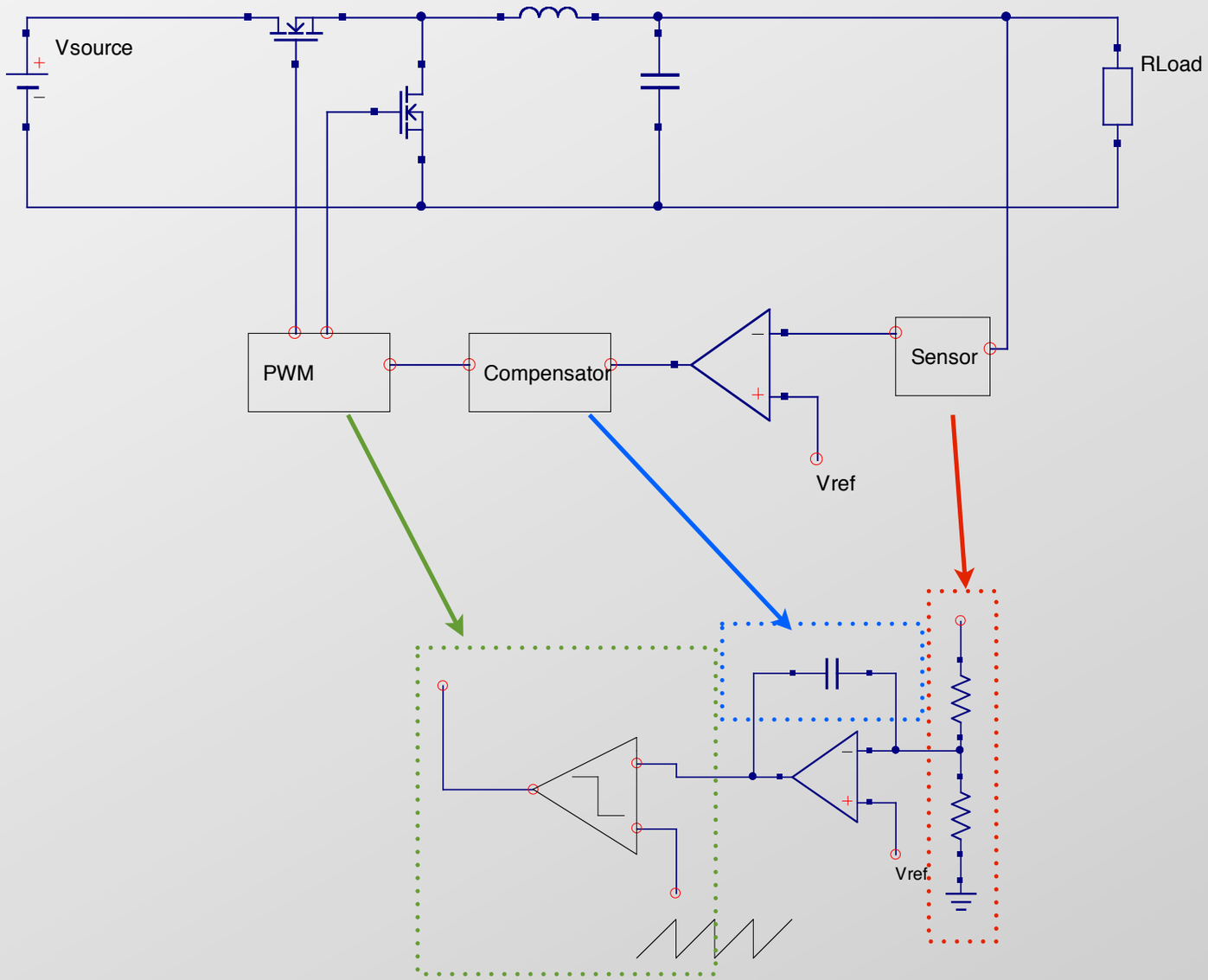
- The presentation contains simplifications for the purpose of clarity. Simulation results are however accurate
- All simulations use behavioral model of AMIS4 DCDC ASIC, using the SIMPLIS simulator from Simetrix technologies
  - Switching @ 2MHz
  - Use inductance of 200nH
  - Transfer function’s corner frequency 120kHz

General DCDC converter



T(s) = loop gain = product of all gains around forward and feedback paths of the loop

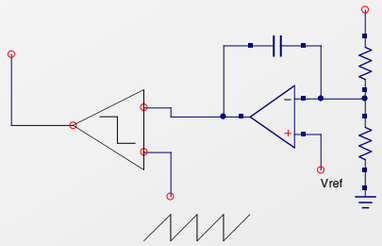
General DCDC converter

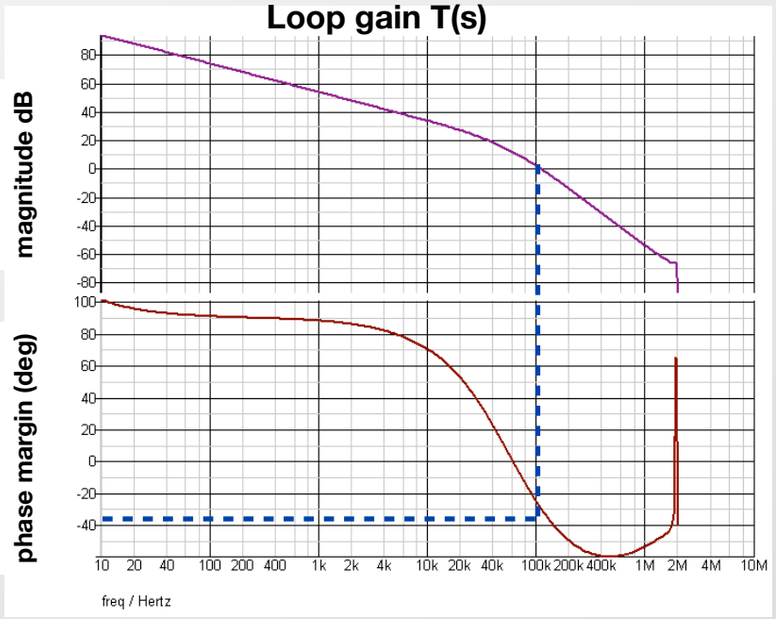


T(s) = loop gain = product of all gains around forward and feedback paths of the loop

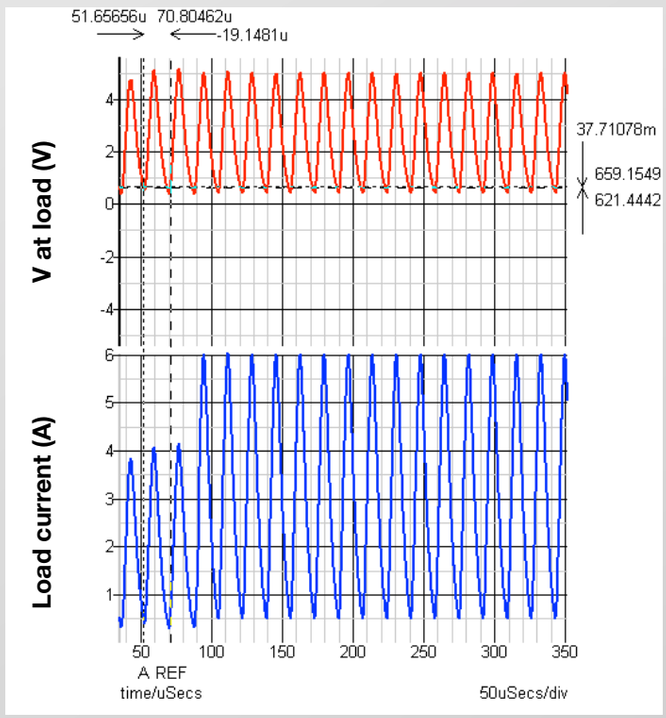
Design of compensator

Inappropriate PI compensator





Time-domain load transient



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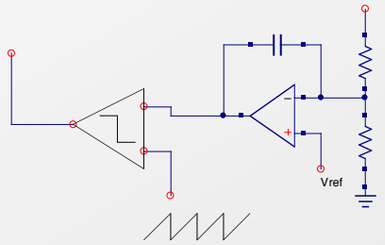
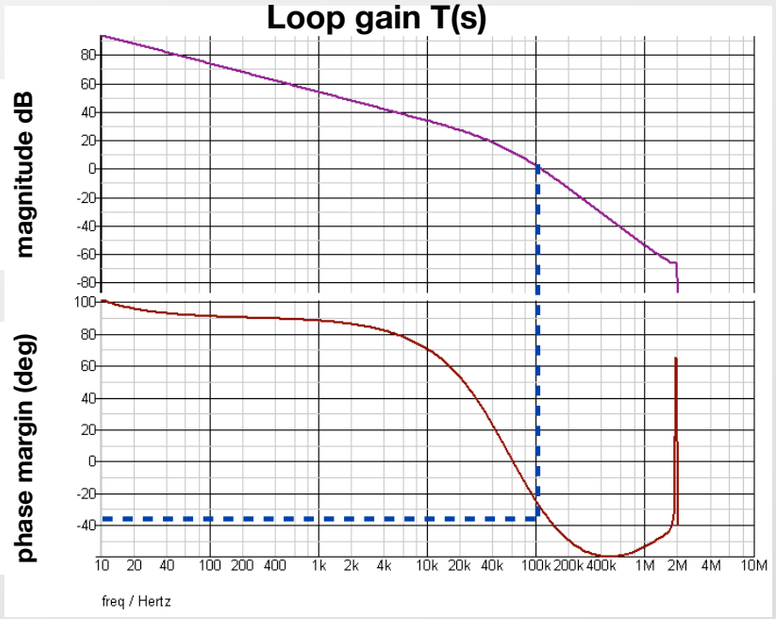
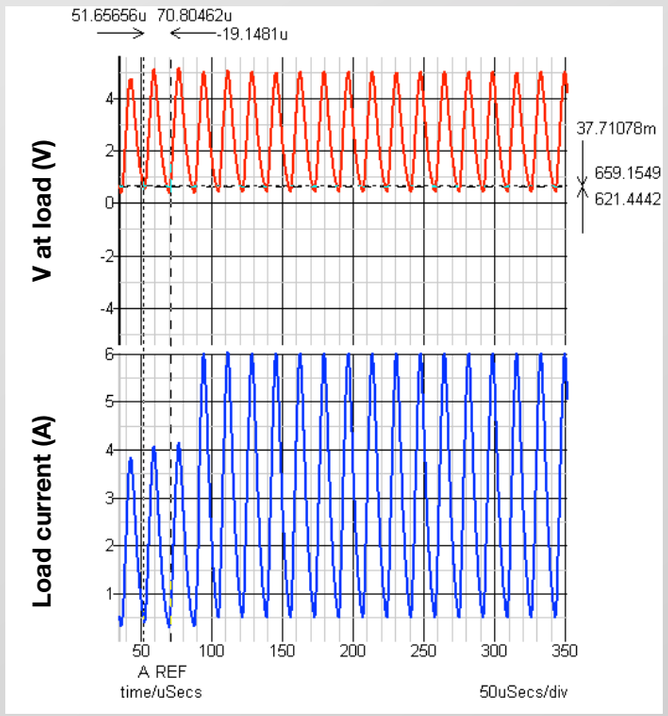
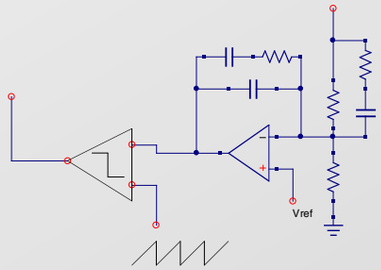


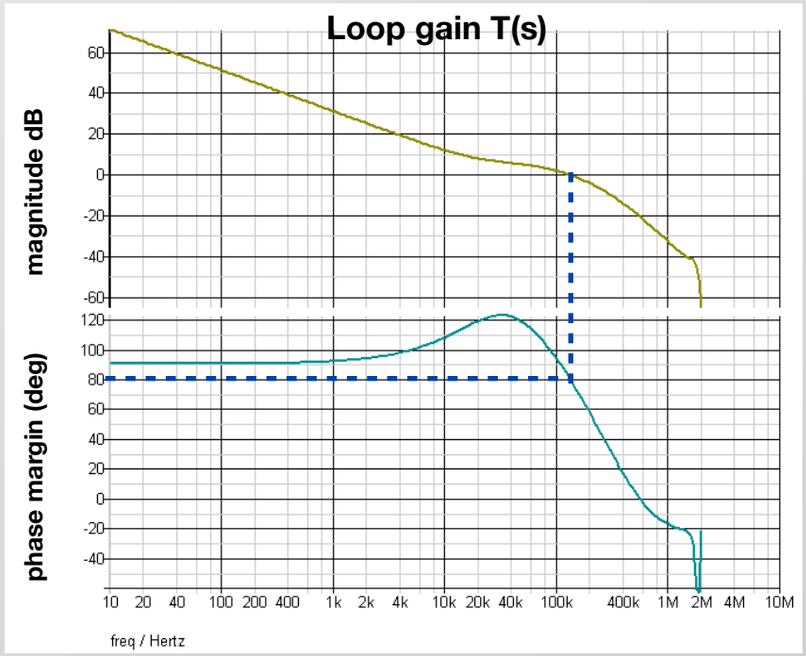


Time-domain load transient

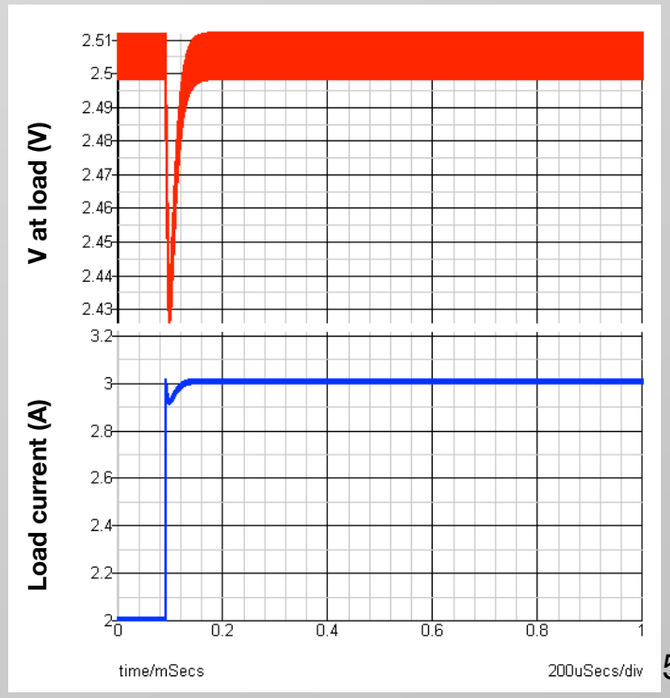


Appropriate PID compensator





Time-domain load transient



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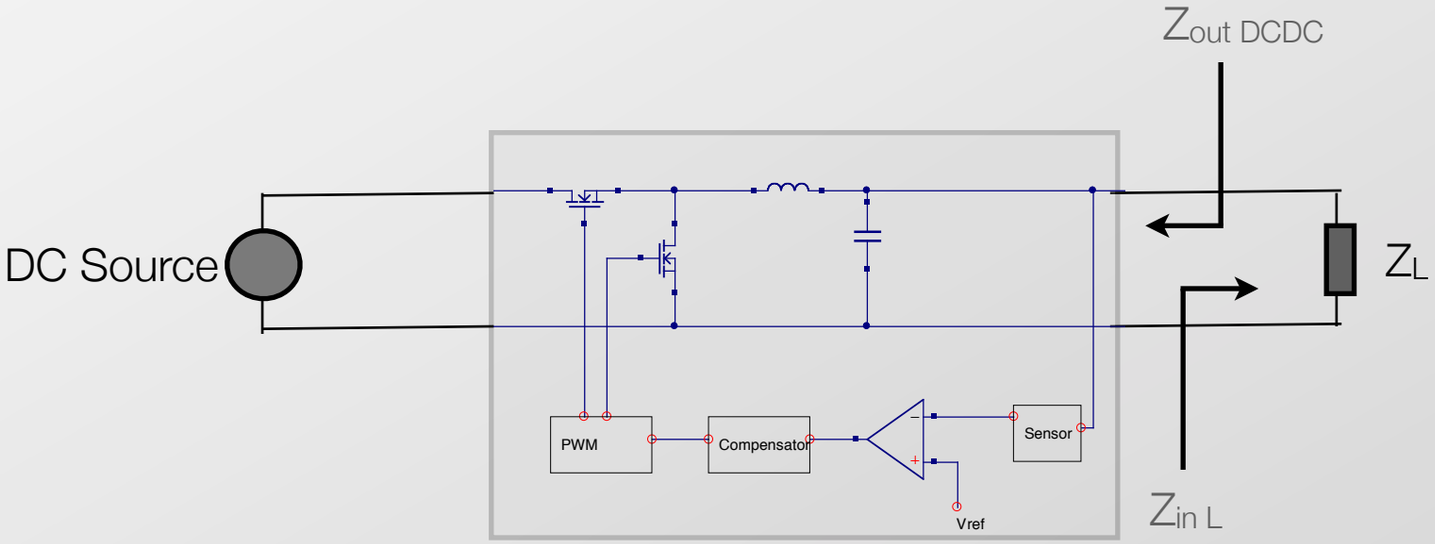
Load effect on converter's loop gain

- The addition of a 'generic' load impedance Z_L to the 'nominal' R_L modifies the Loop Gain: T(s) -> T'(s)

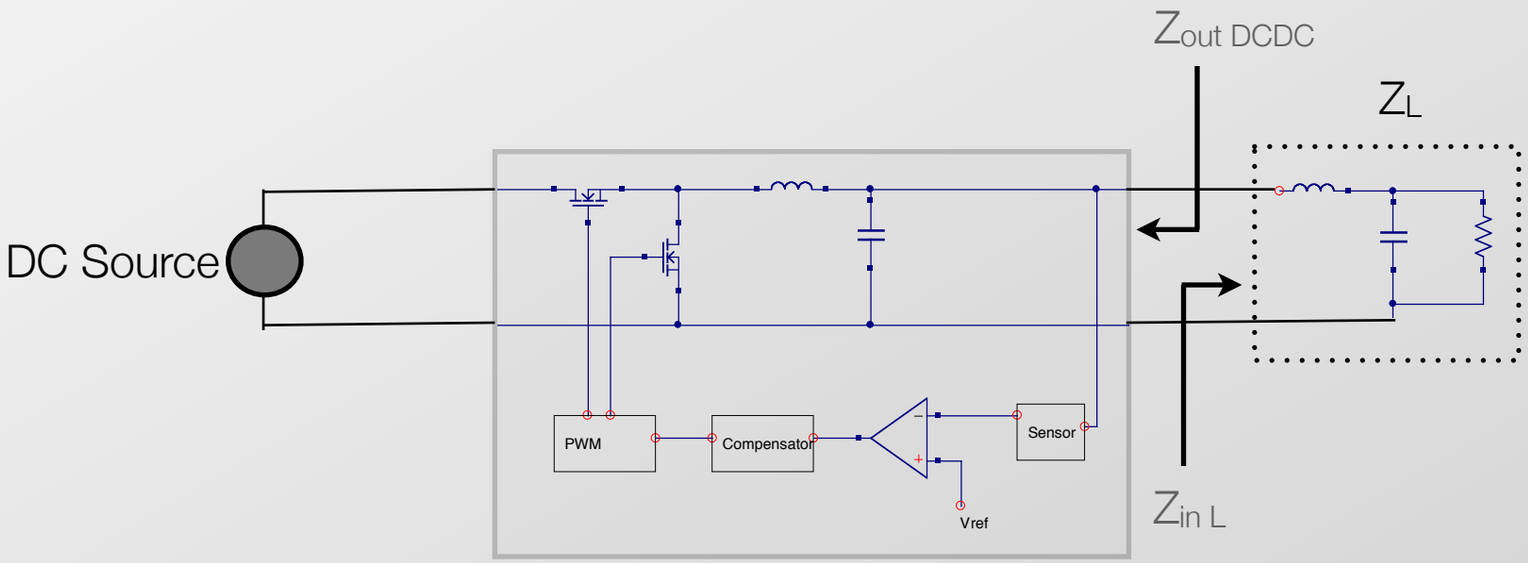


$$T'(s) = \frac{T(s)}{(1+T(s))Z_o/Z_L + 1}$$

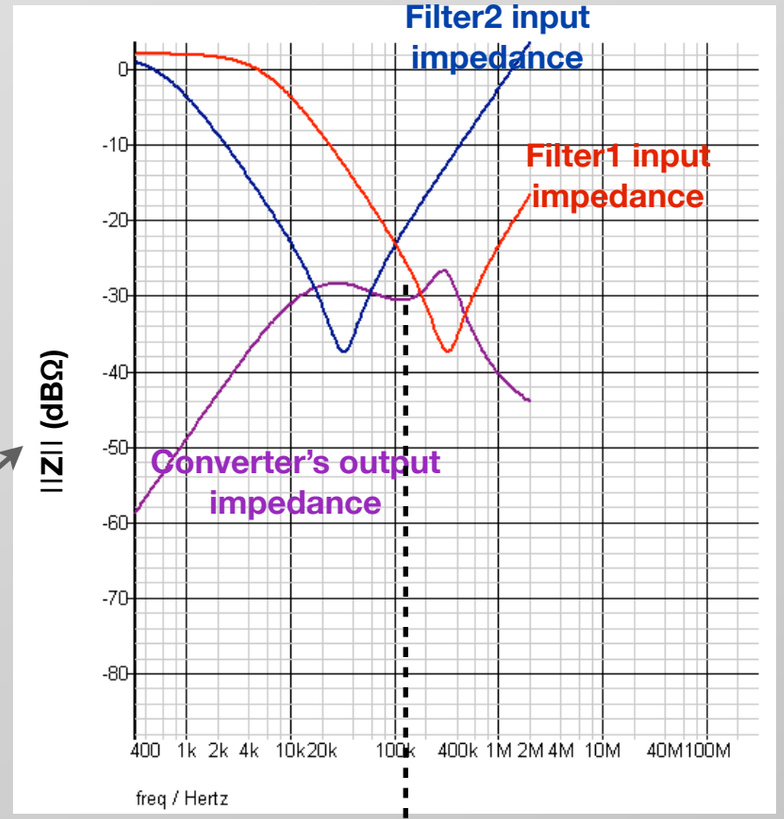
- If $Z_o/Z_L << 1$ then T'(s) = T(s) and the stability of the converter is NOT affected by the addition of the output impedance. This translates in the commonly used stability criterium: $\boxed{Z_o << Z_L}$
- NB: if the criterium is not satisfied, T(s) is modified but the converter could still be stable

Output filter

- The output filter (pi) required to reduce conducted noise represents a load impedance different than the ‘nominal’. Its input impedance has to be compared with the output impedance of the ‘converter



Example for 2 different output filters
(real configuration with ESRs, not exactly the schematic shown to the right)

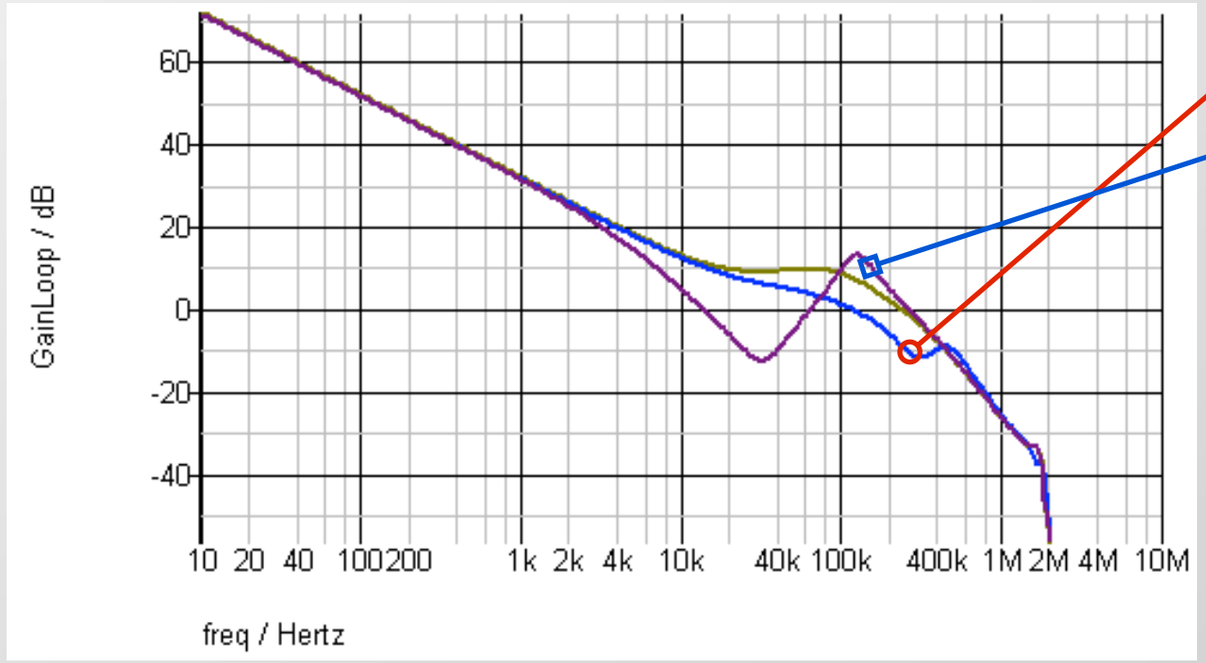


The magnitude of the impedance is expressed in dBΩ:

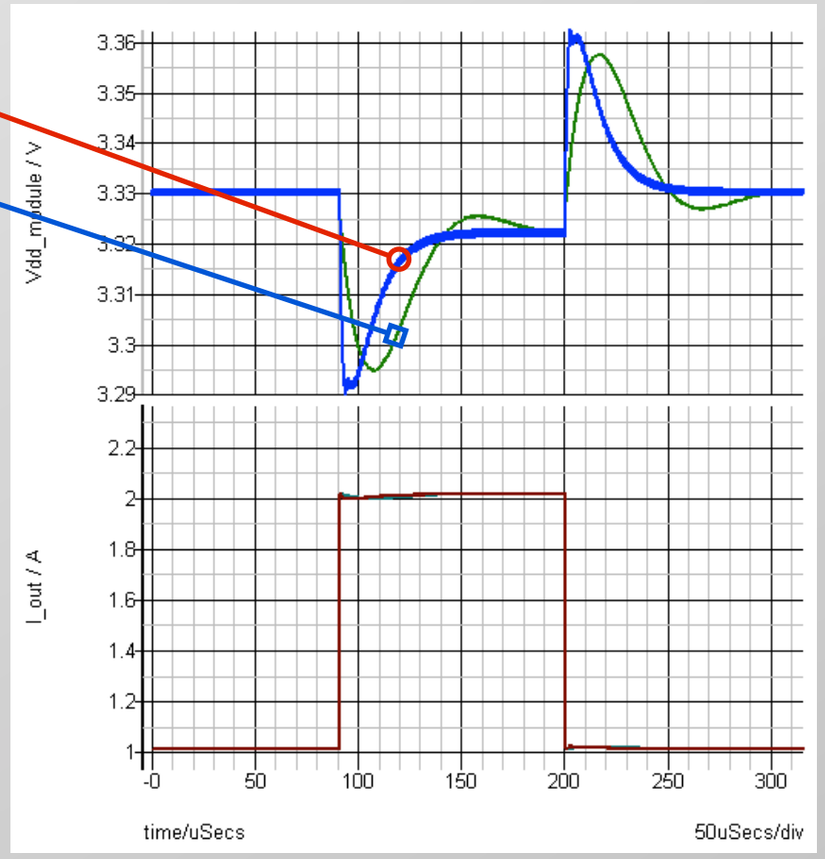
$$IIZII_{dB} = 20 \log_{10} (IIZII/1\Omega)$$

Output filter

- The addition of Z_L modifies the loop gain T(s) of the converter
- In one of the example cases, this happens above the crossover frequency. In the other, below the crossover frequency (and this can introduce instabilities, which does not happen in the shown test case)

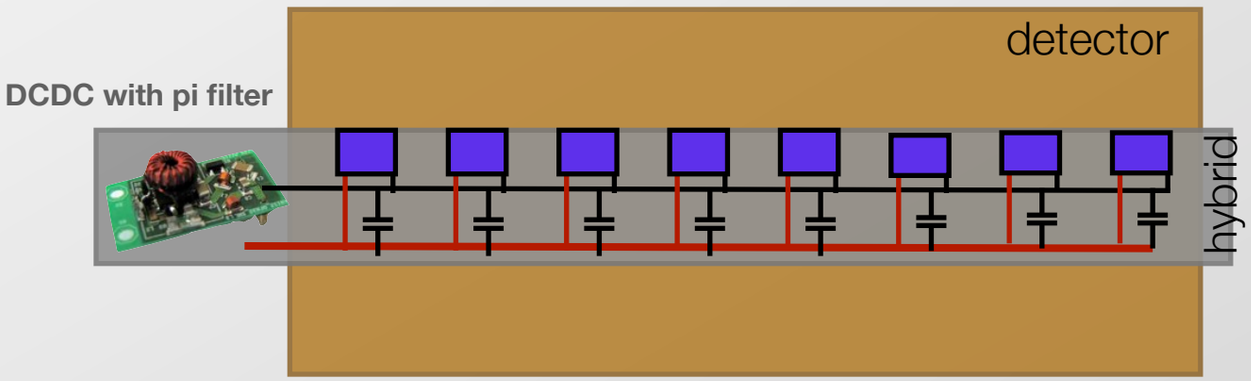


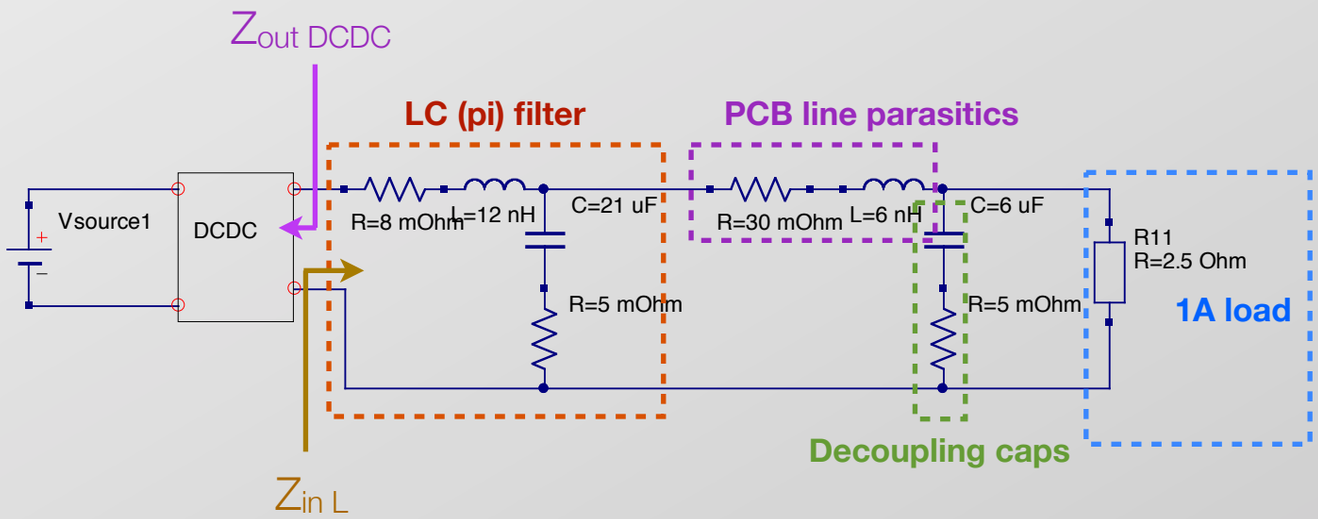
Example voltage variation from a load transient for the 2 filters. The response is different



Test case 1: DCDC on FE module

- A sketch of a possible configuration with a DCDC on the FE module is studied
- Remember that a pi filter is placed in our DCDC prototypes at both input and output of the converter to decrease conducted noise





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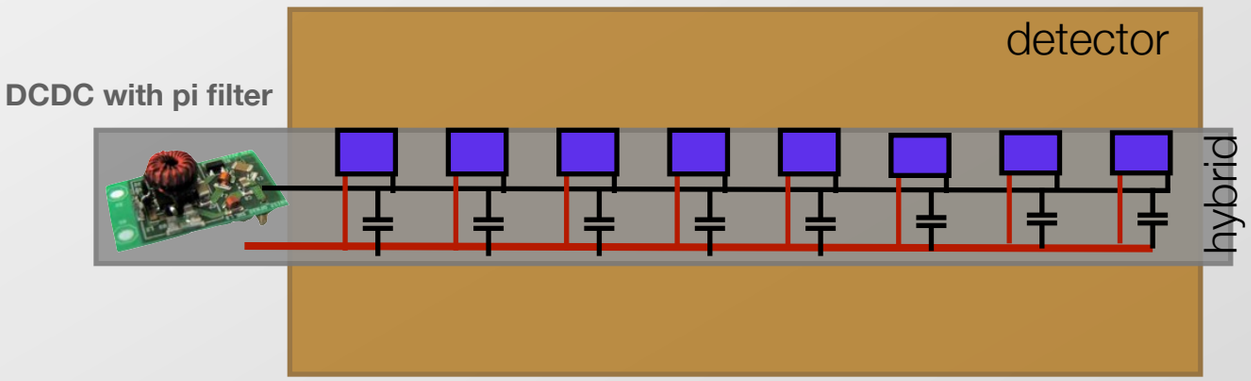
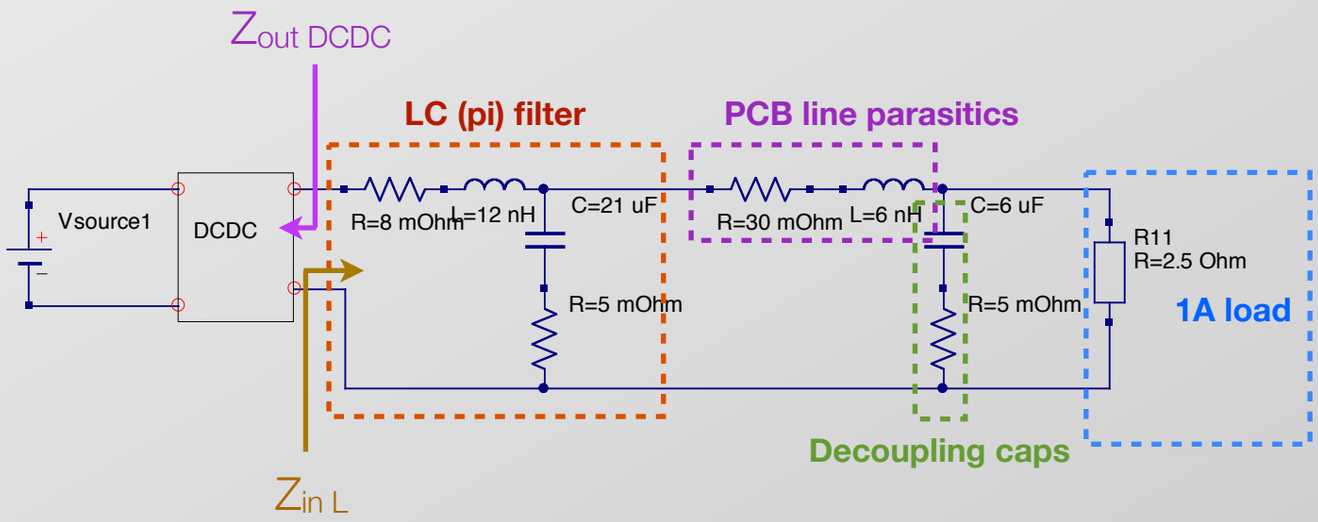
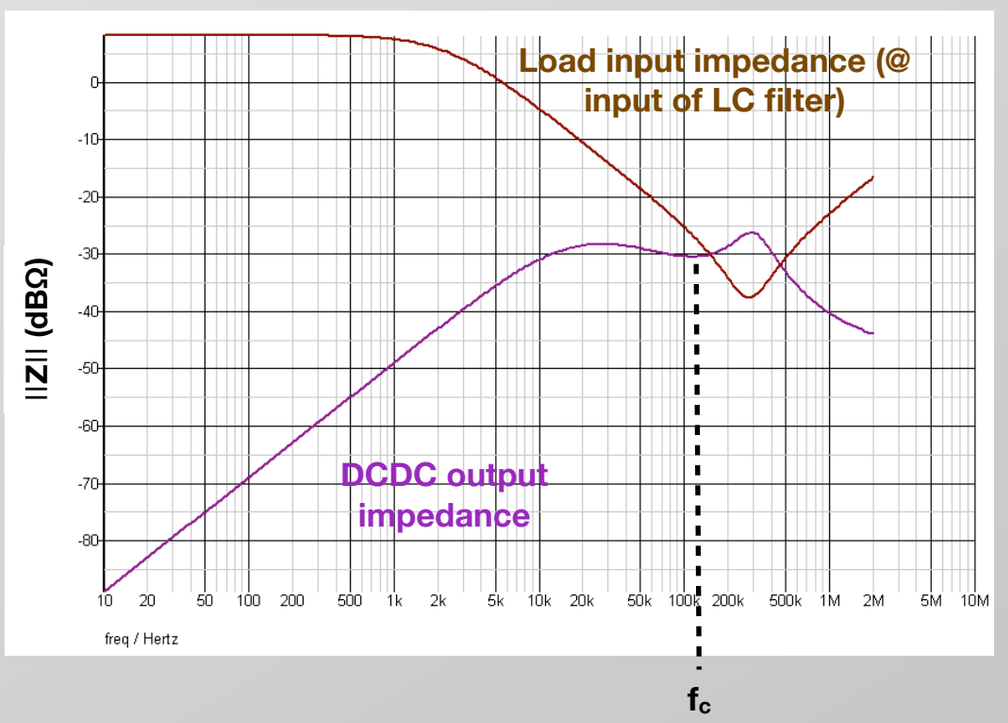
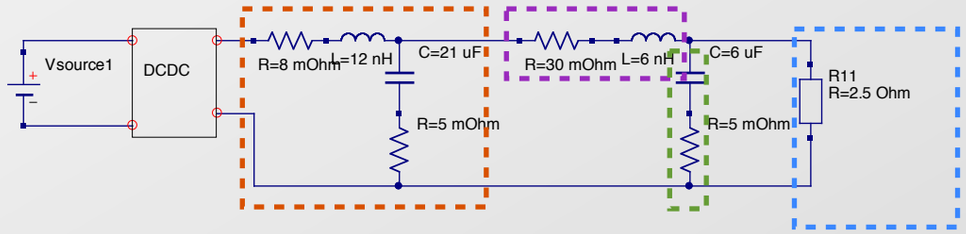




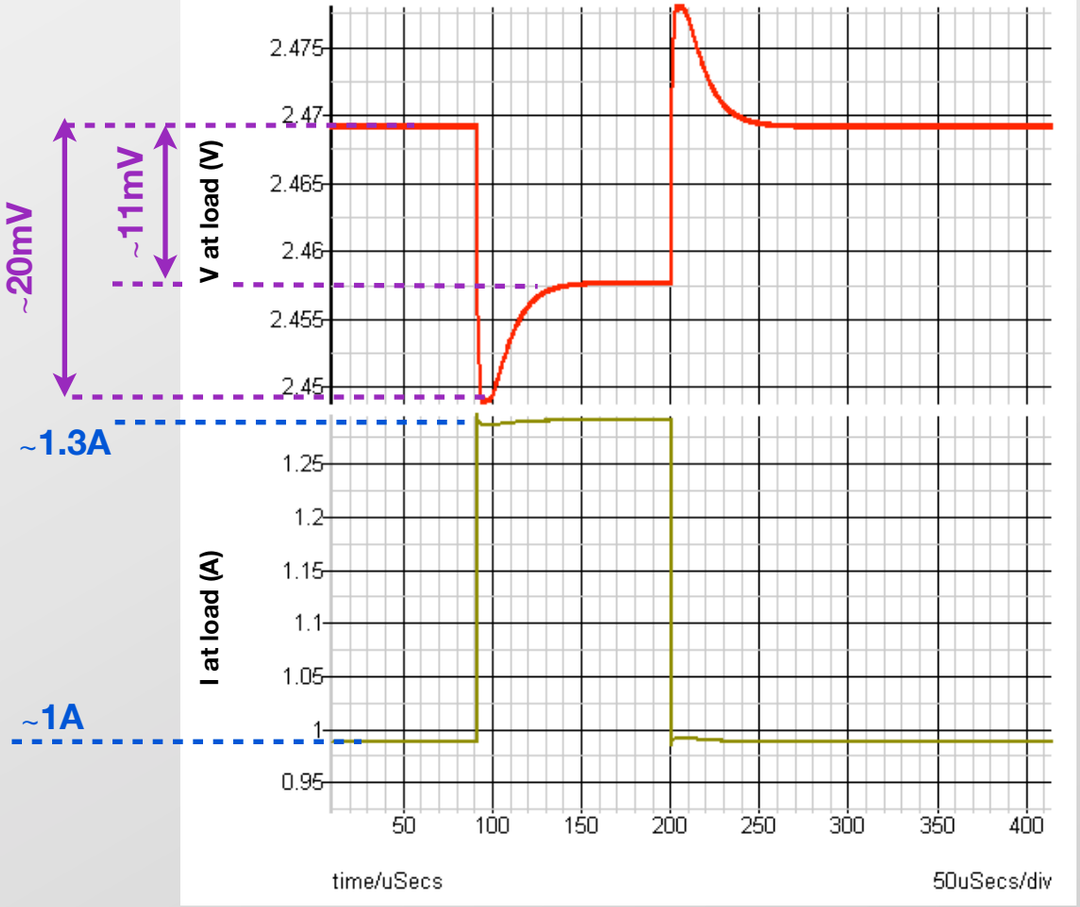


Test case 1: DCDC on FE module

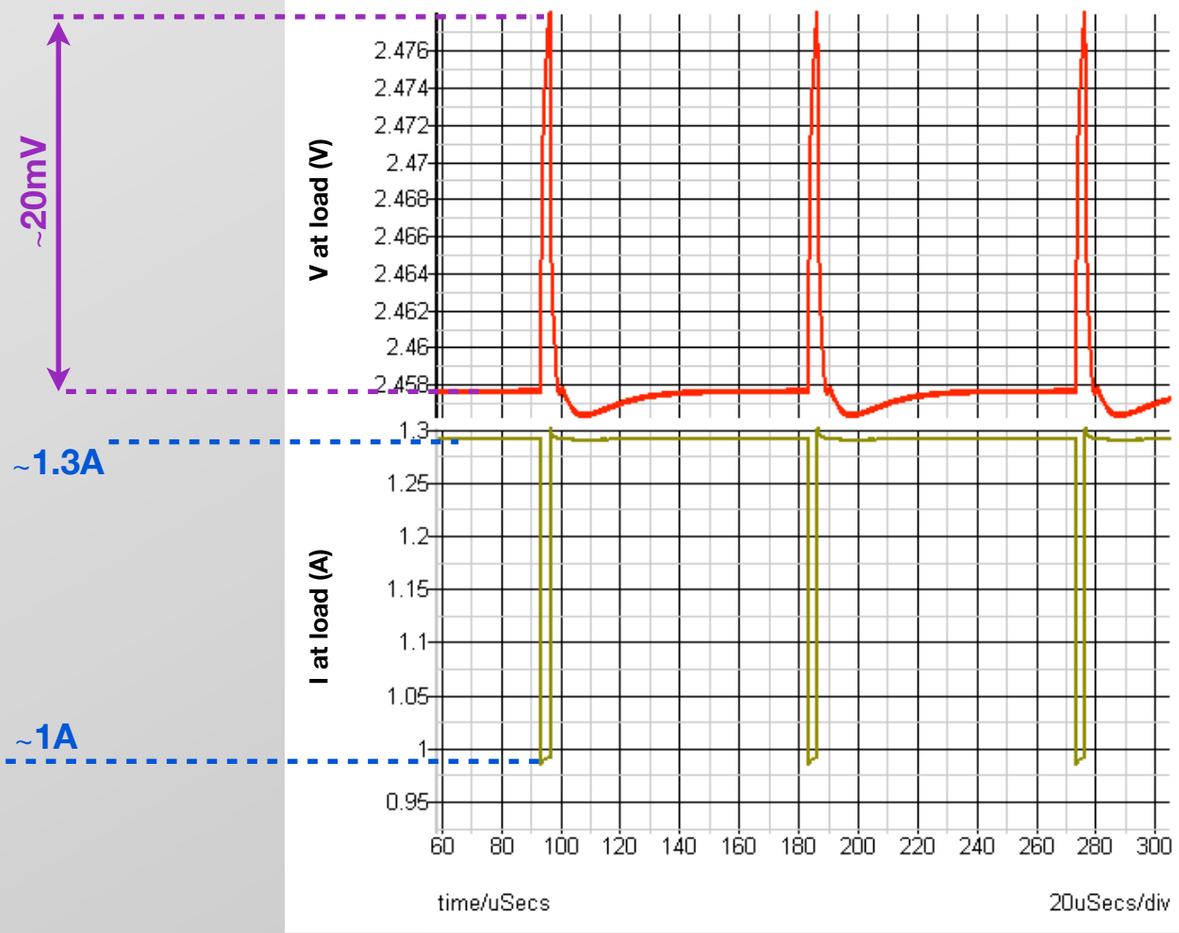
- Example load transients (1->1.3A). Voltage and current measured across the load resistor



2 transients

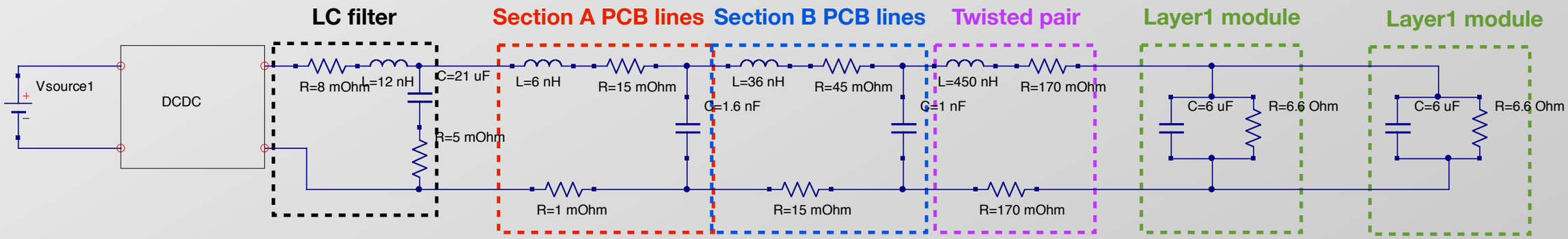


Orbit-gap-like transients (3us gaps with 90us period)



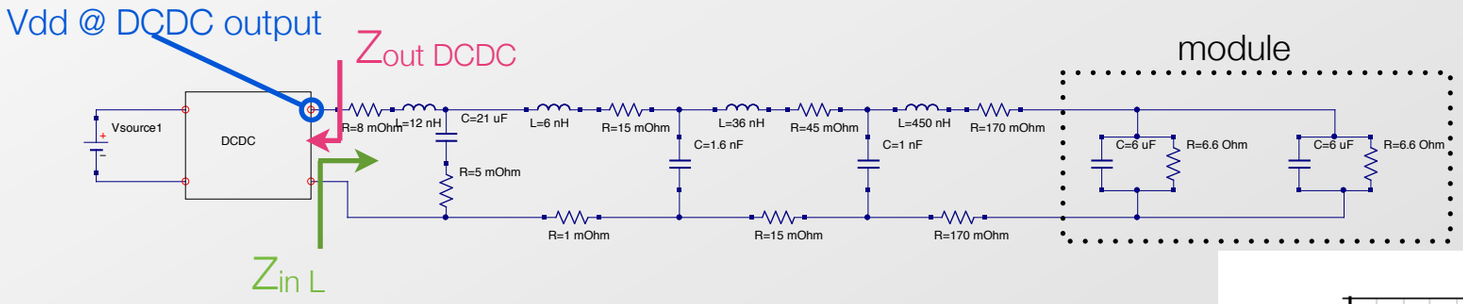
Test case 2: CMS pixel upgrade phase 1

- DCDCs are sitting about 2m away from the modules
- Precise characterization of line impedances not yet available, but best current estimates have been used (thanks to K.Klein and W.Karpinski)
- Example computation for worst-case load transient: 2 modules of Layer1 (current from 1 to 2.8A in 100ns)

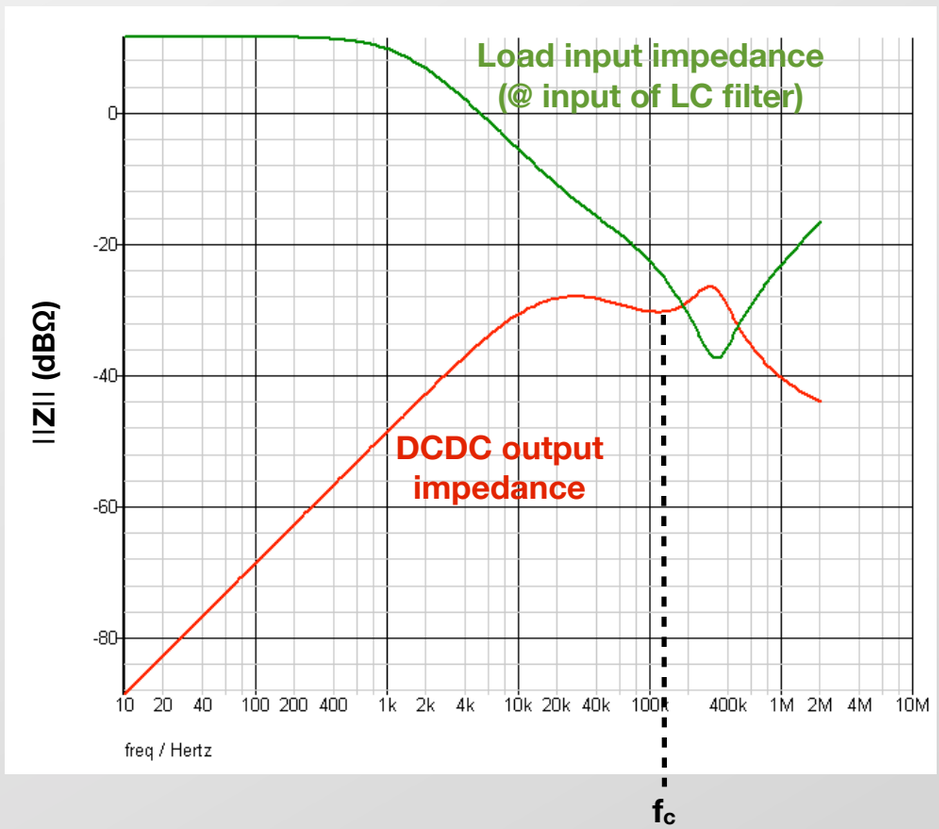


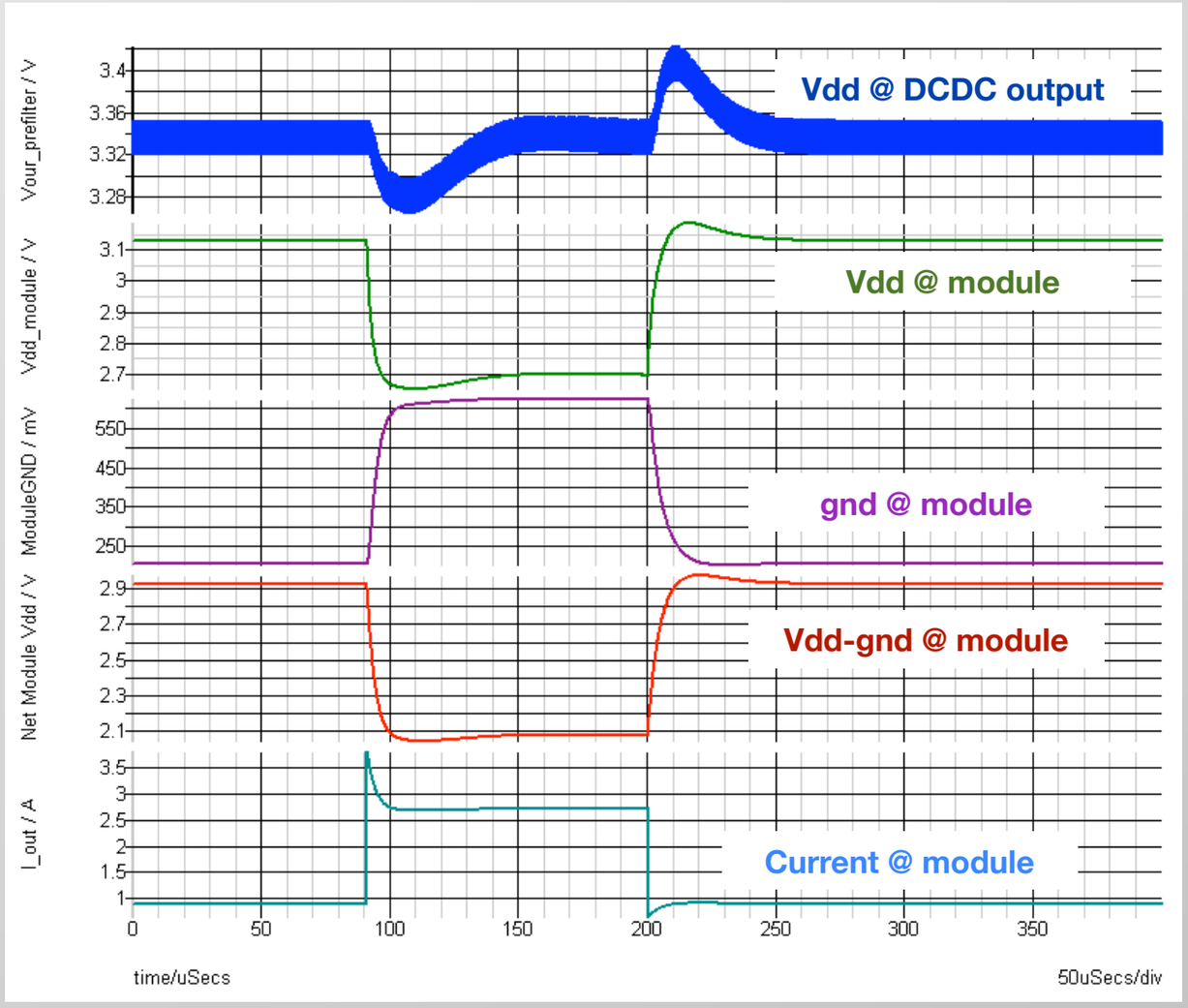
Test case 2: CMS pixel upgrade phase 1

- Simulation results for AC (impedance comparison) and load transients



Transients 1A -> 2.8A ->1A in ~1ns





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- *Effect of the input filter impedance*
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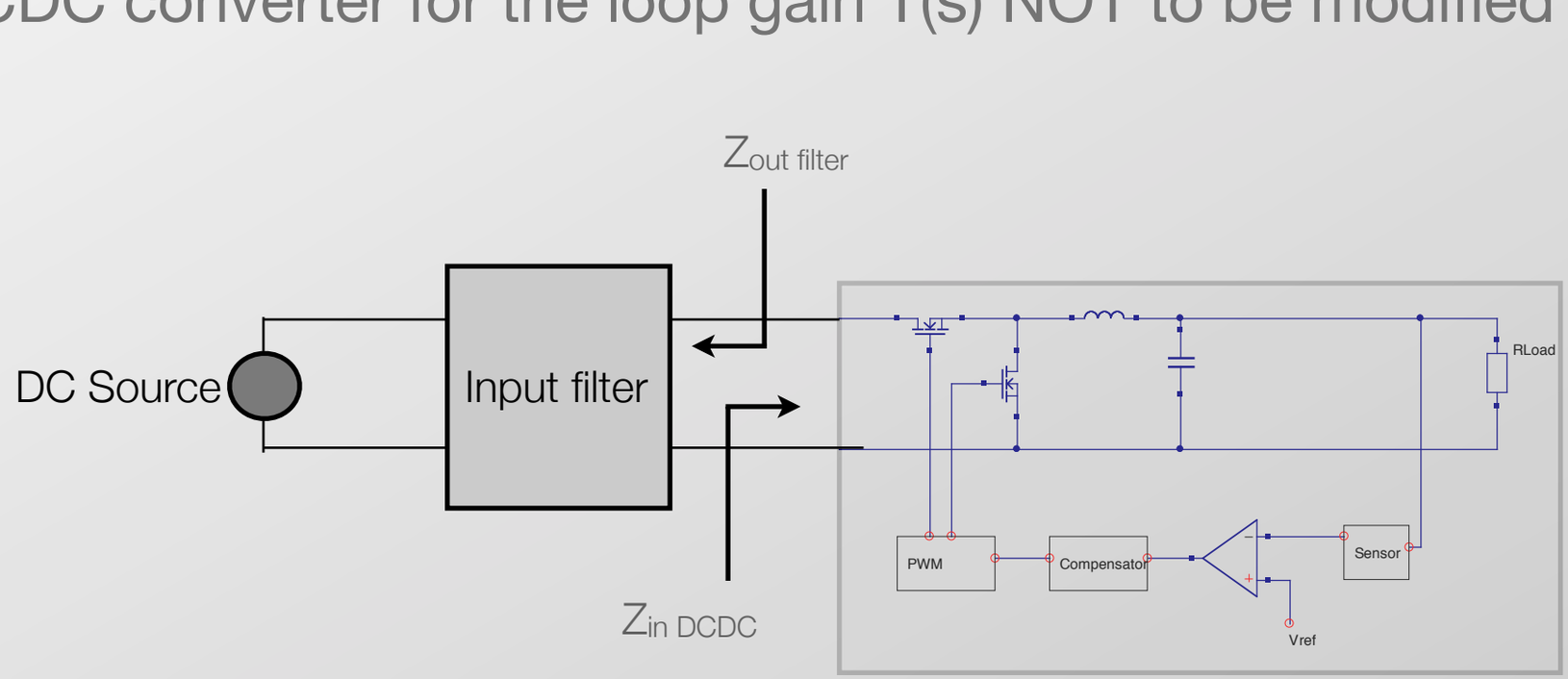
Input filter effect on converter's Loop Gain

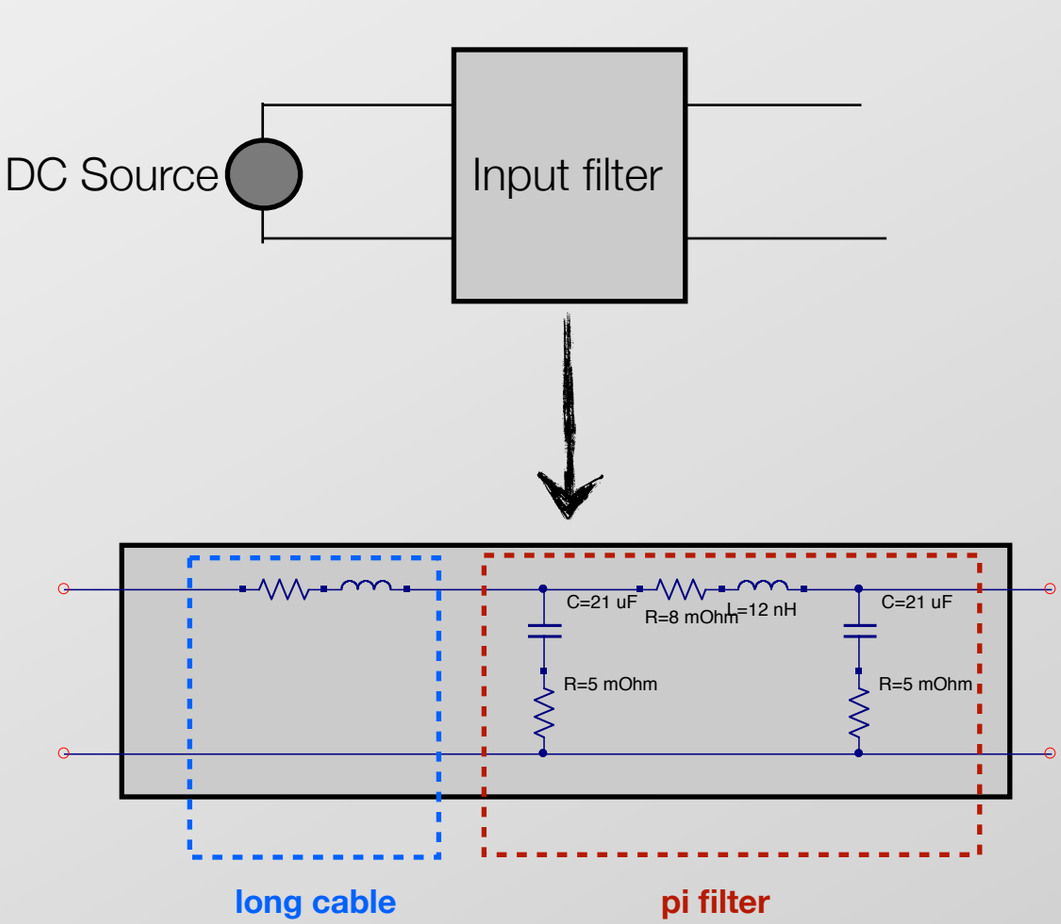
- So far the input voltage was provided by an ideal source
- Anything making the source non-ideal (R,L,C) can be seen as an input filter
- As before, there is a condition involving the impedances of the filter and DCDC converter for the loop gain T(s) NOT to be modified by the filter



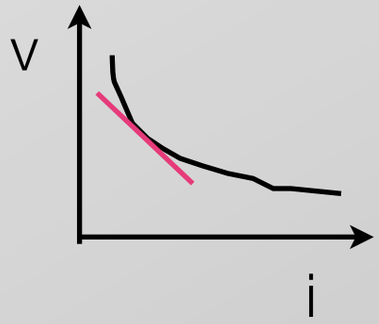
For the buck converter, this condition can approximately be expressed as $Z_{out\ filter} << Z_{in\ DCDC}$

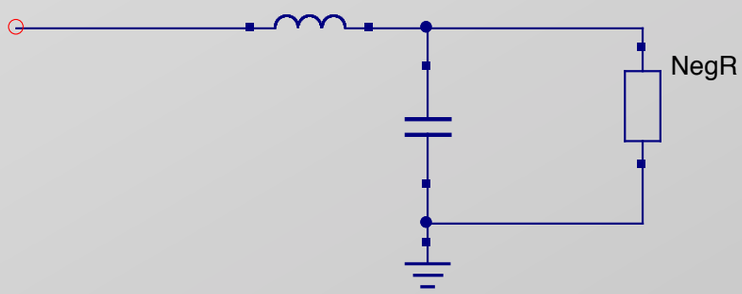
Typical input filter

- The input pi filter is part of it, with the addition of L and R of the cables from the PowerSupply (in our configuration, very long cables)
- An additional important complication is the presence of an equivalent negative impedance at the input of the converter



DCDC is a constant power load. Ideally
$P_{in}=P_{out}=P=vi \Rightarrow v=P/i$
Therefore at the input
$R_{in}=dv/di=-P/i^2=-v/i$

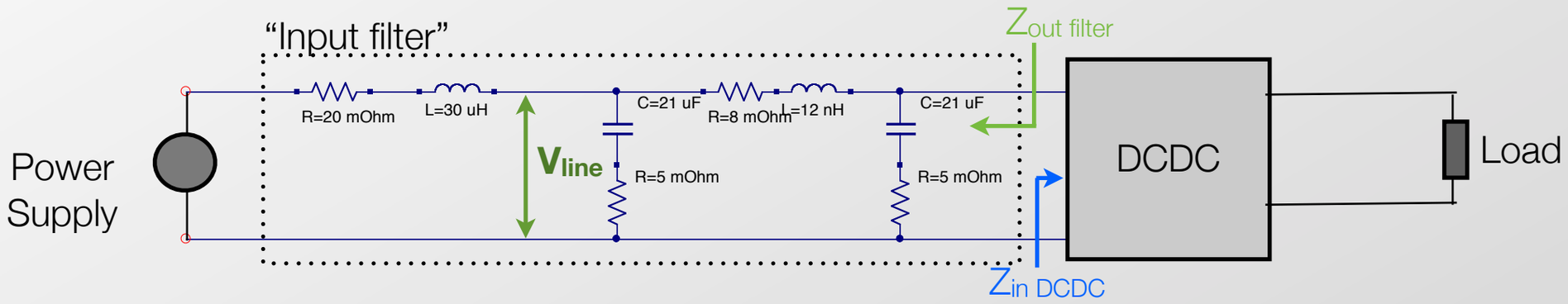


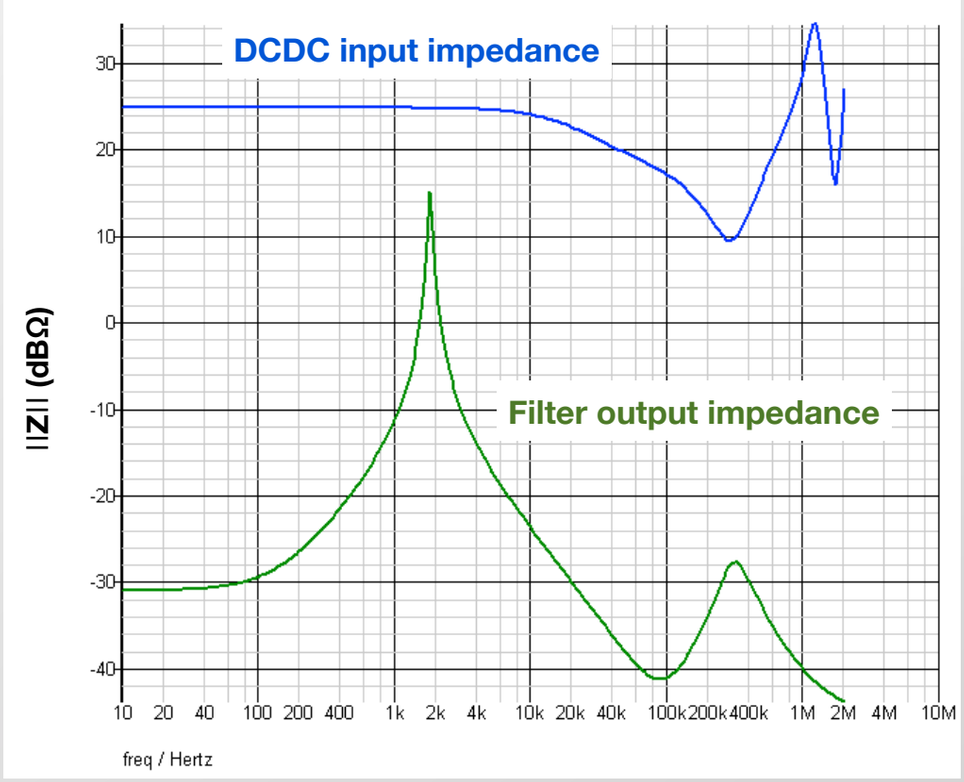


The LC of the filter might lack damping because of the negative resistance. The input node might oscillate

Example input filter 1

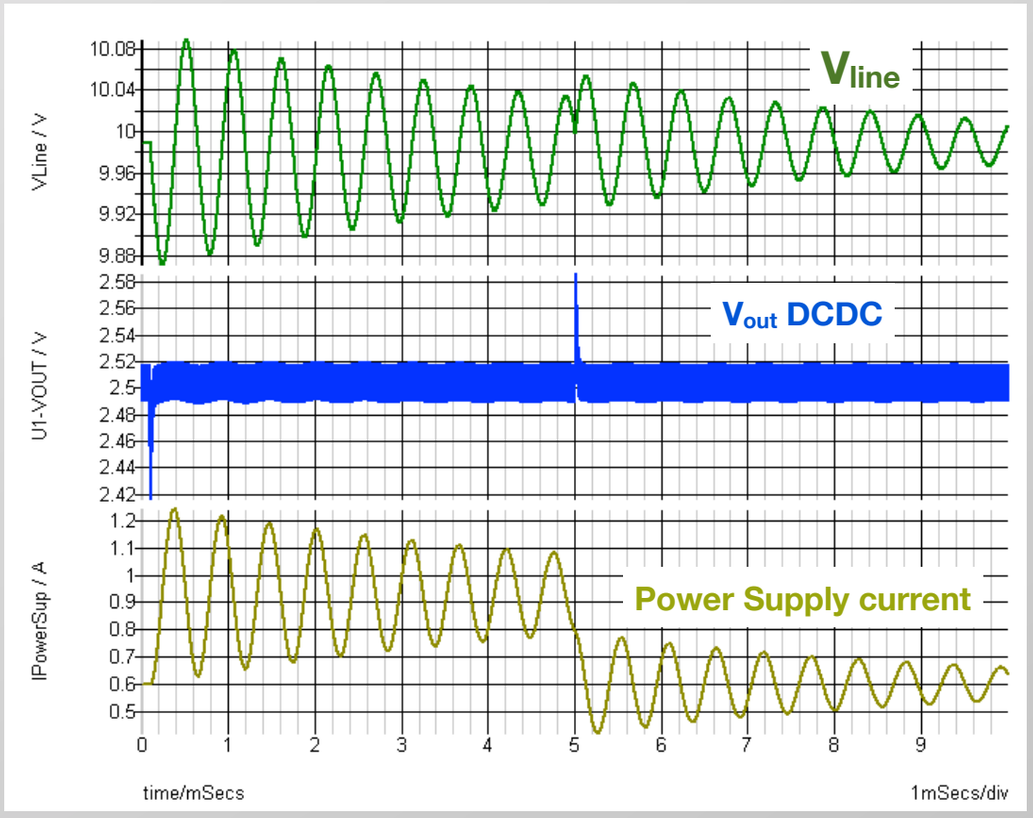
- Cable with high L and very small R (very little damping)





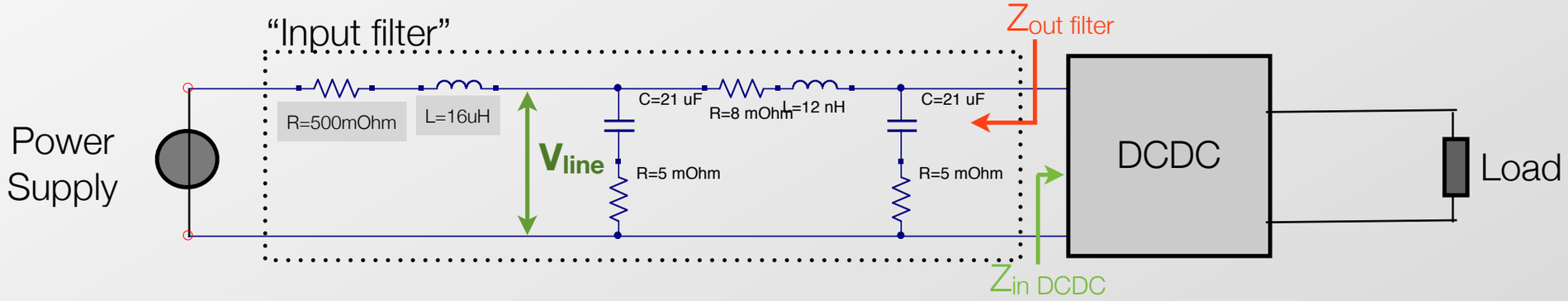
T(s) of the DCDC not modified, but large LC peak

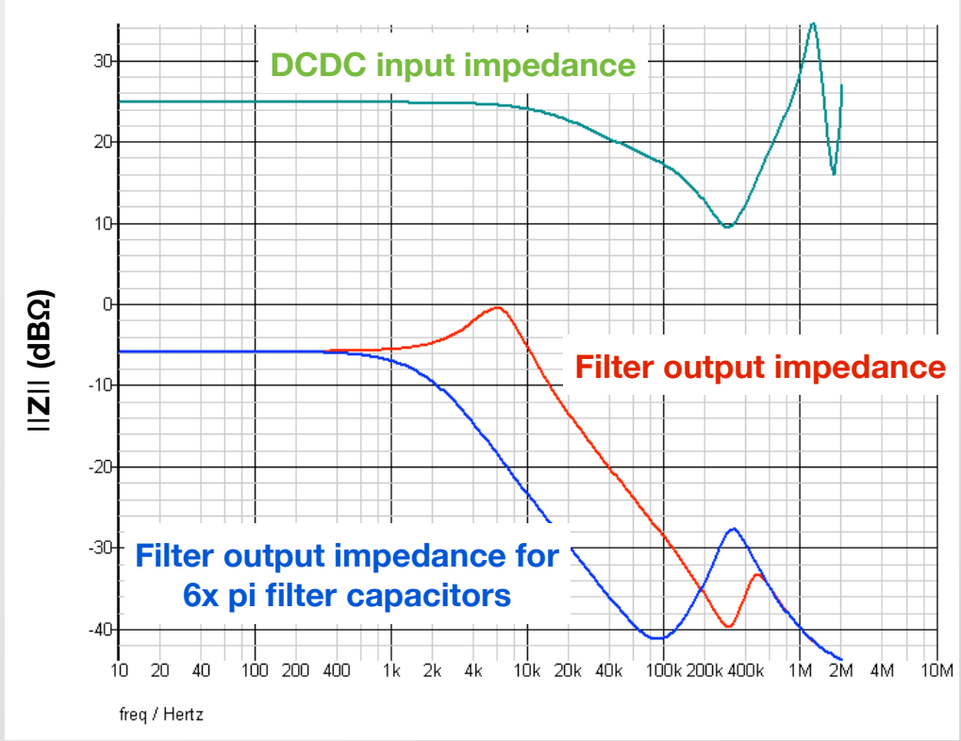
2 load transients (1A -> 2.8A -> 1A)



Example input filter 2

- Cable with high L and large R (much closer to real life)

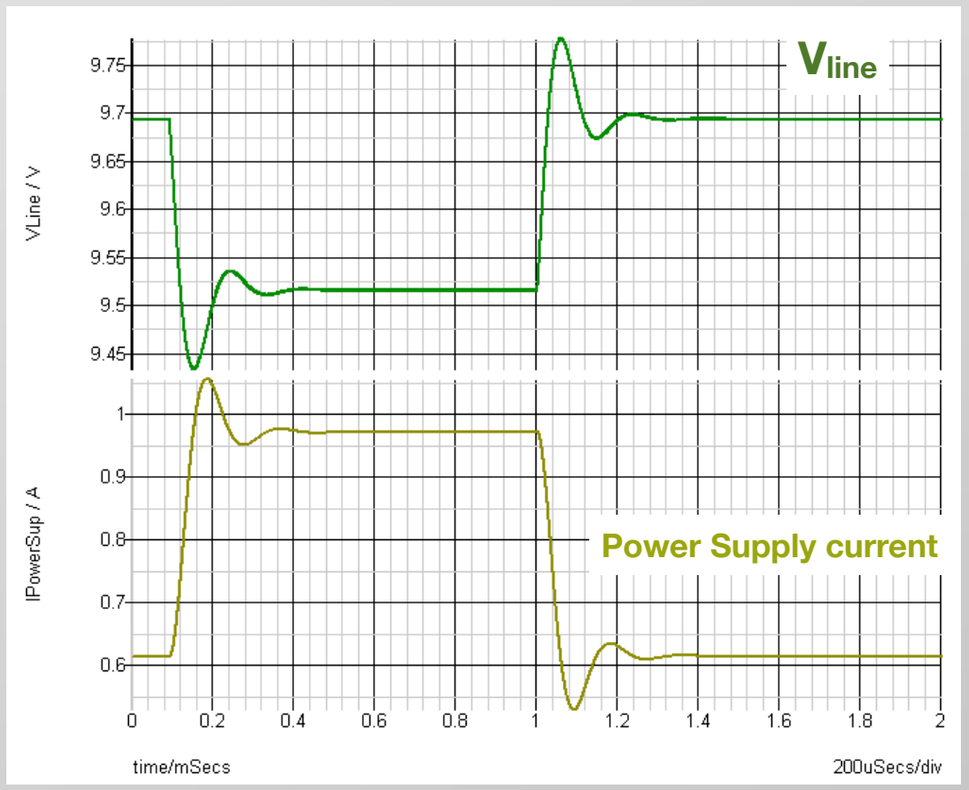




T(s) of the DCDC not modified

$Z_{out\ filter} << Z_{in\ DCDC}$

2 load transients (1A -> 2.8A -> 1A)



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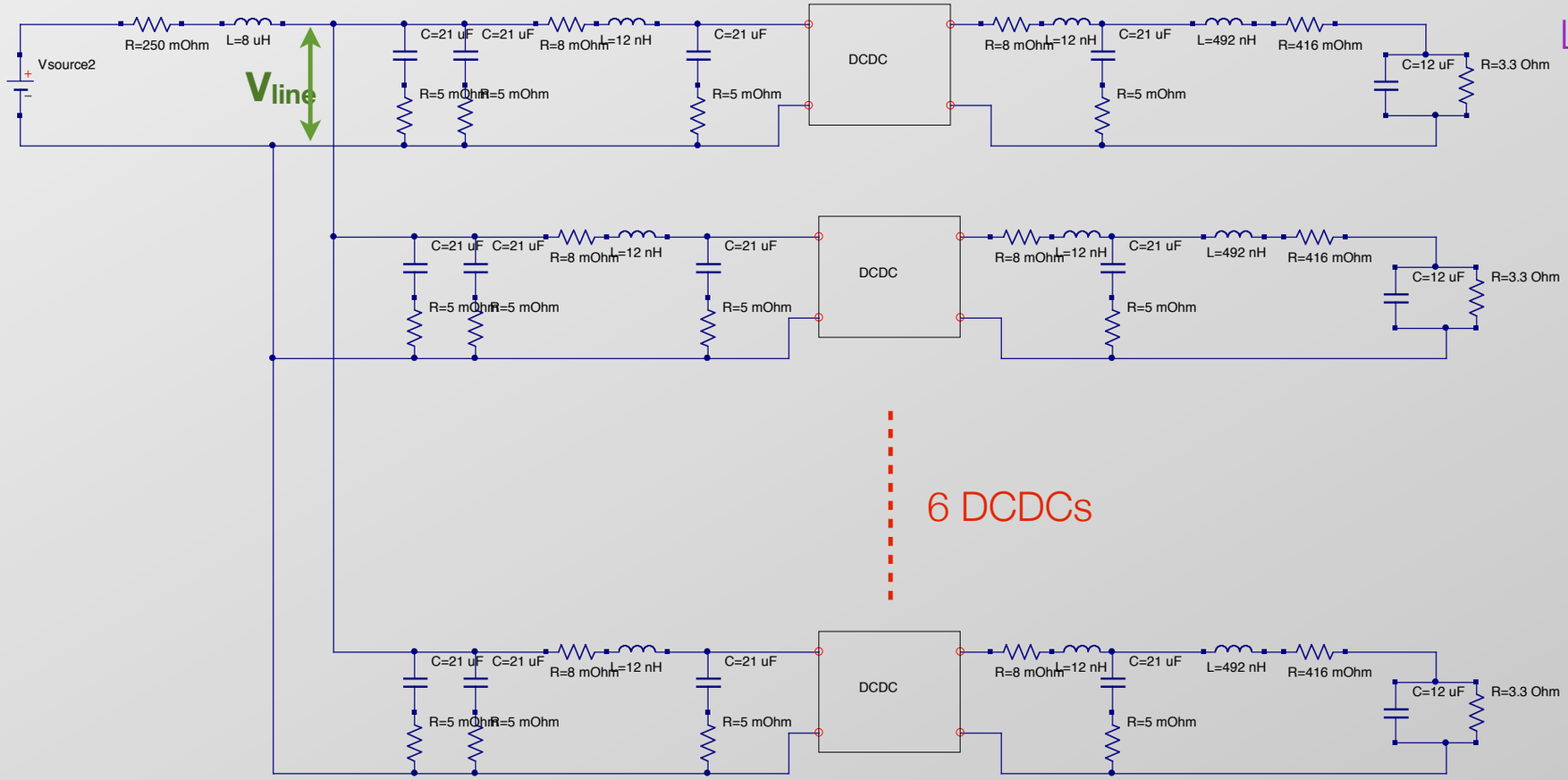
Case study: CMS pixels upgrade phase 1

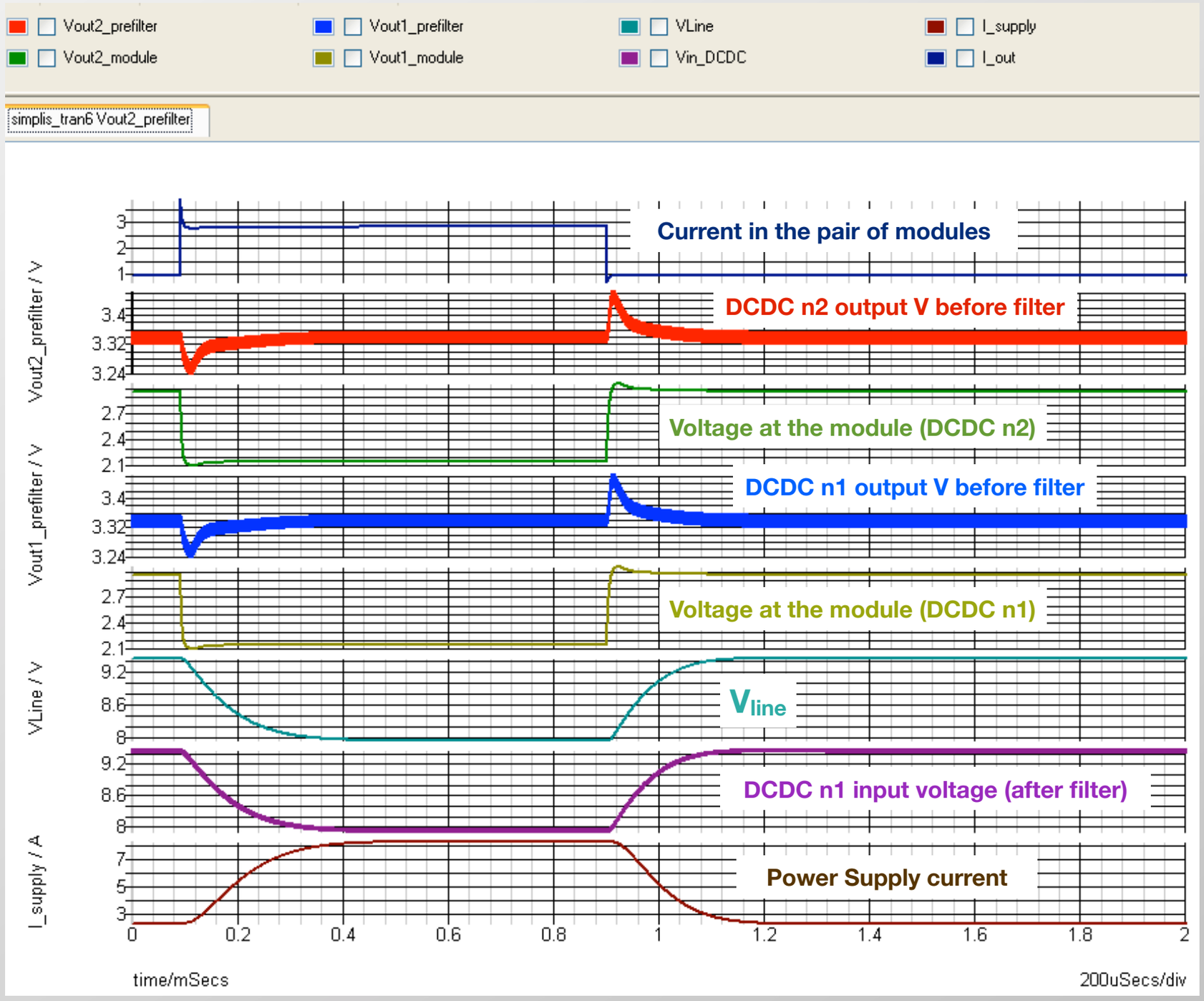
- The full distribution scheme (with ideal PS) is studied, using the best available estimates
- As case study, and to have the maximum current transient, a specific (unreal) configuration is chosen: 1 PS channel powering 6 DCDCs belonging to Layer1 (2 modules powered by each DCDC)



Load transients for each DCDC
1A -> 2.8A -> 1A

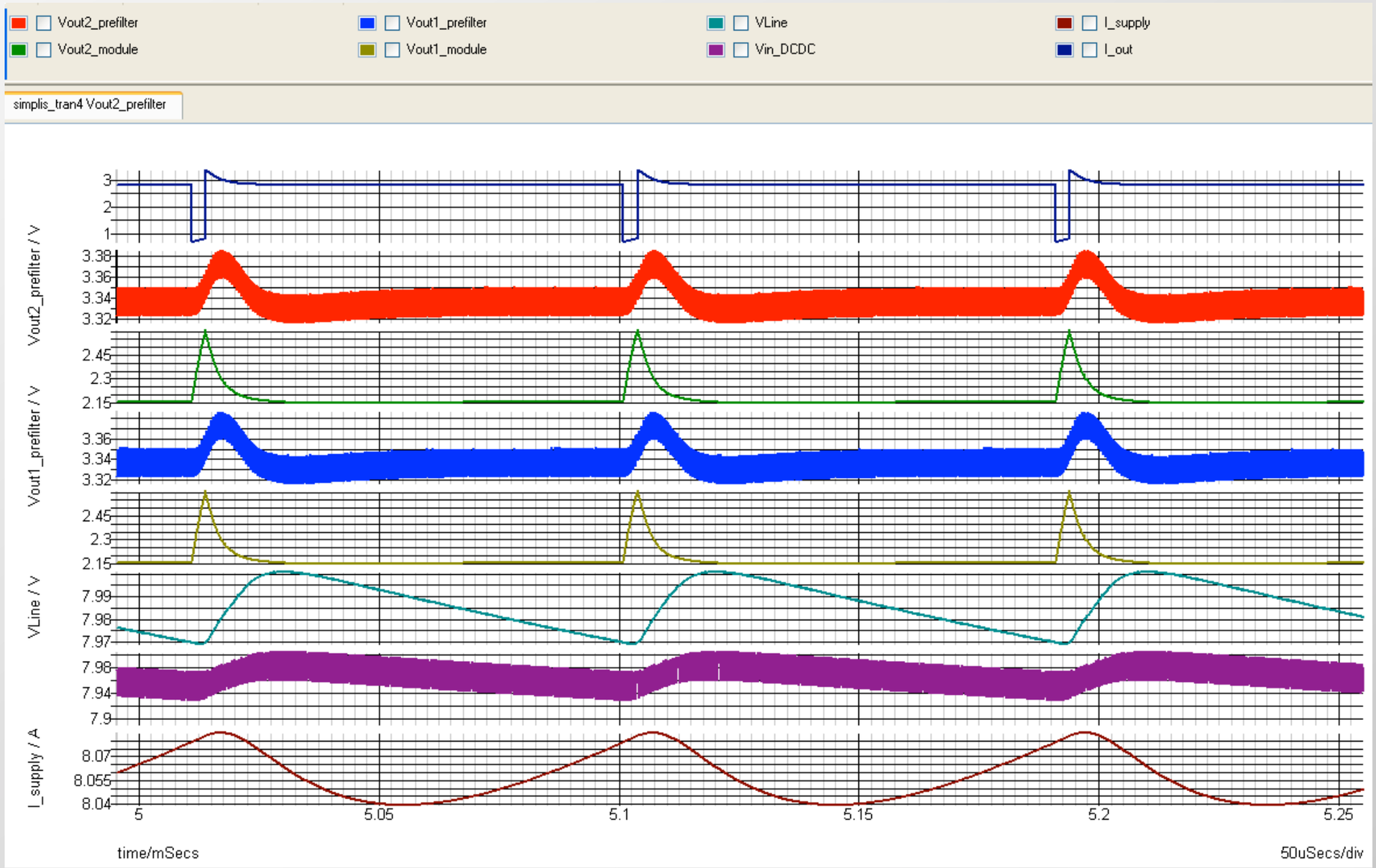
Two load transients

- Each module pair instantaneously (NOT in 100ns as in reality) changes current from 1A to 2.8A, then back



Orbit-gap simulation

- Current in each module pair drops to 1A (from 2.8A) for 3us every 89us, then goes back to 2.8A



Current in the pair of modules

DCDC n2 output V before filter

Voltage at the module (DCDC n2)

DCDC n1 output V before filter

Voltage at the module (DCDC n1)

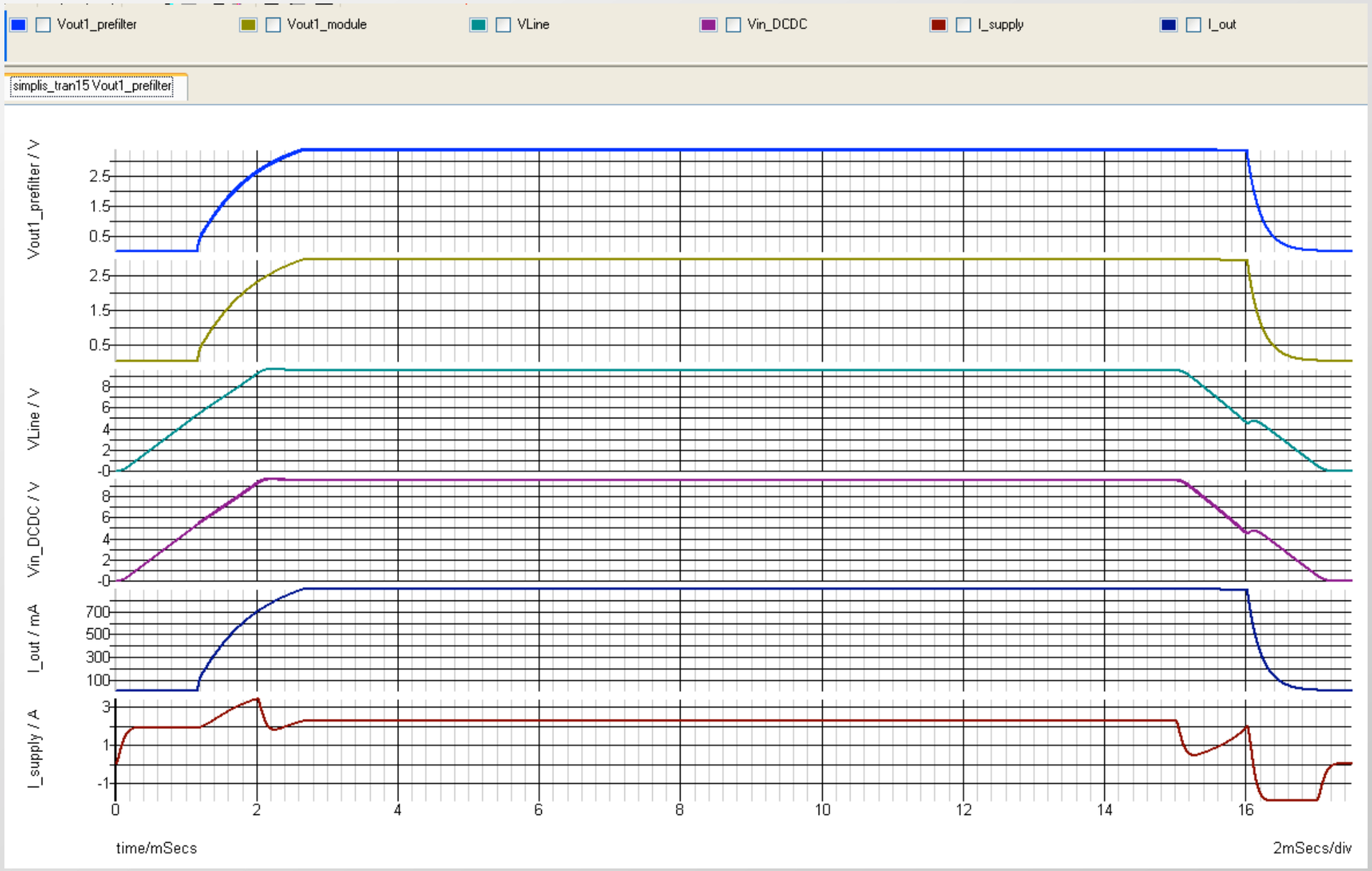
V_{line}

DCDC n1 input voltage (after filter)

Power Supply current

Power-on & power-off of full PS channel

- Voltage ramp from the PS (rise & fall time 2ms) to turn-on and -off all 6 converters loaded with an equivalent 1A current



DCDC n1 output V before filter

Voltage at the module (DCDC n1)

V_{line}

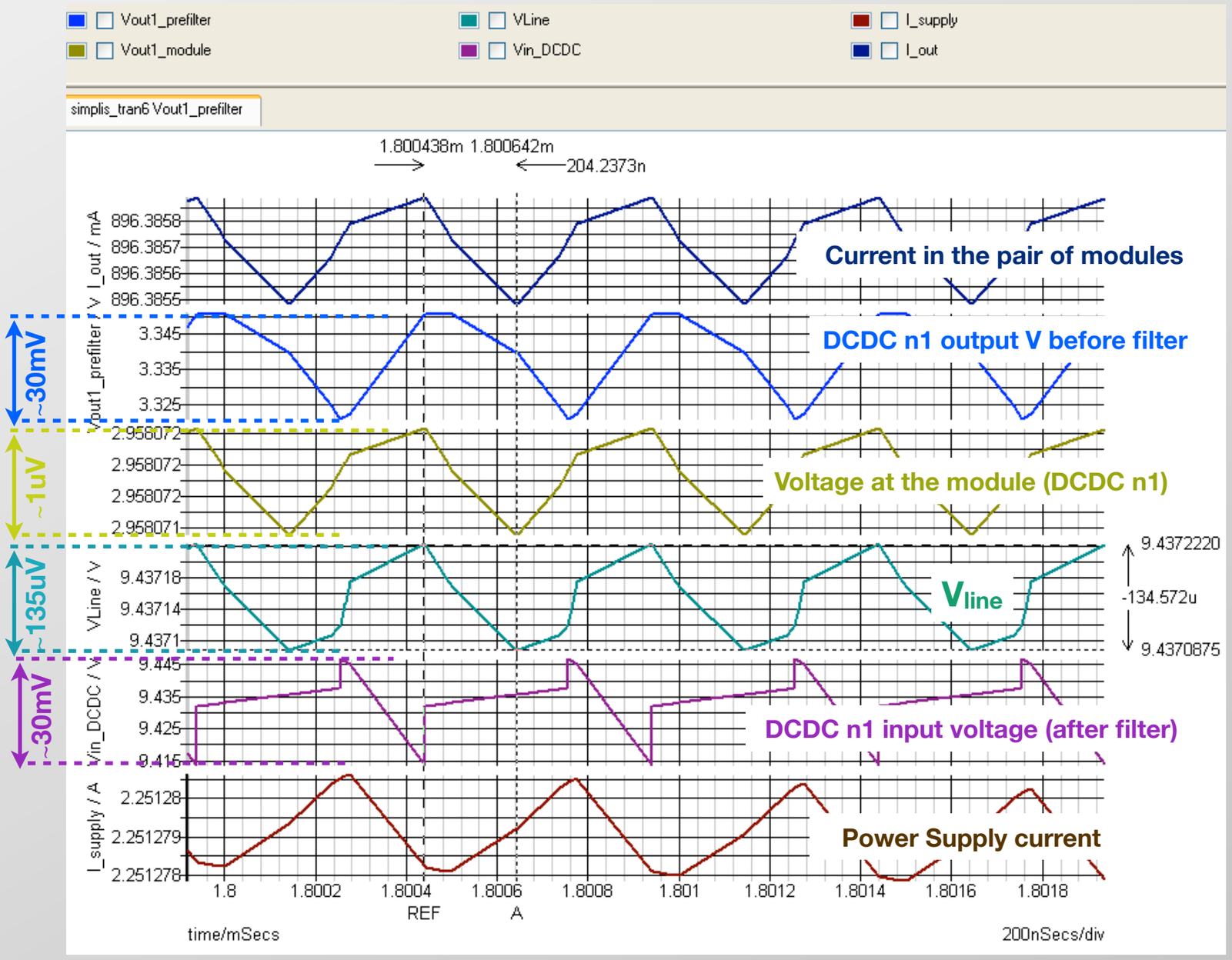
DCDC n1 input voltage (after filter)

Current in the pair of modules

Power Supply current

Voltage ripple on the line

- In this simulation, all 6 DCDCs switch at 2MHz in phase (practically this might never happen)
- The peak-peak voltage ripple induced on the line (V_{line}) is limited well below 1mV (effect of the input pi filter: before the filter it is 30mV)
- At the module, this is of the order of 1uV



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Conclusion

- The stability of detector systems embedding POL DCDC buck converters has been studied
  - The addition of real impedances at the output and input of the converter might influence the gain loop of the converter, with consequences on the converter's stability
  - Due to the negative impedance of the DCDC, the lumped input LC filter might be undamped and oscillations might be observed

- In the explored range of parameters for input and output impedances, based on available estimates, no sign of instability or oscillation has been found

- The developed simulation tools, based on the characteristics of the ASMI4 POL buck, can be used to study specific systems during the development phase and help finding and fixing possible problems