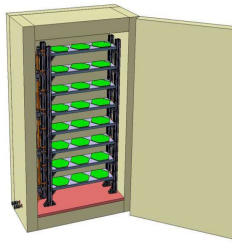
# Using Kria modules for the CMS HGCAL Hexaboard testing system

By

Mehmet Alp Şarkışla (Presenter)
Kıvanç Nurdan

**TÜBİTAK - Bogazici University**

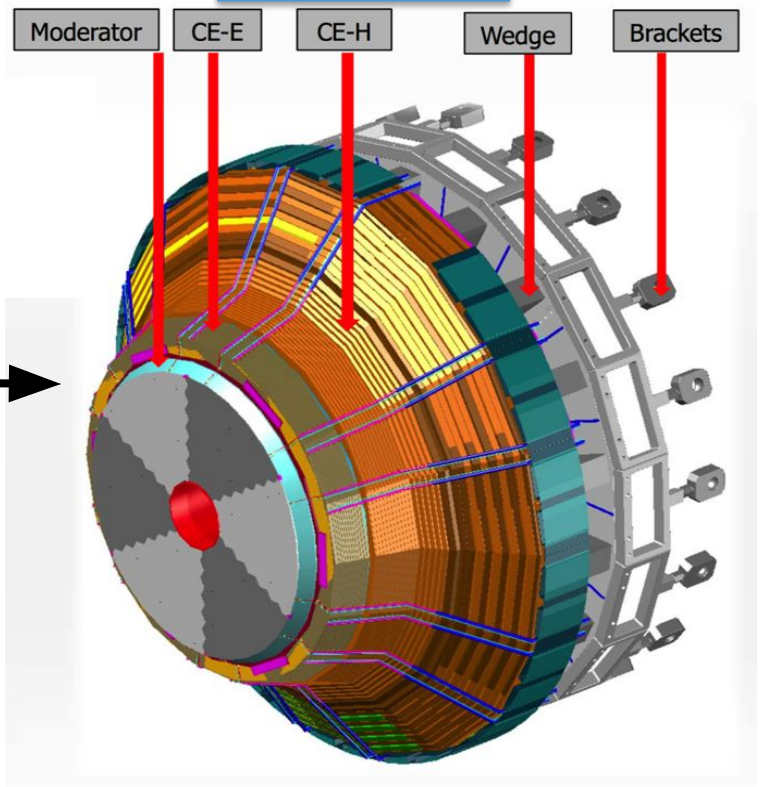


24/05/2023

# CMS HGCAL Experiment

Present CMS endcap calorimeters

HGCAL design

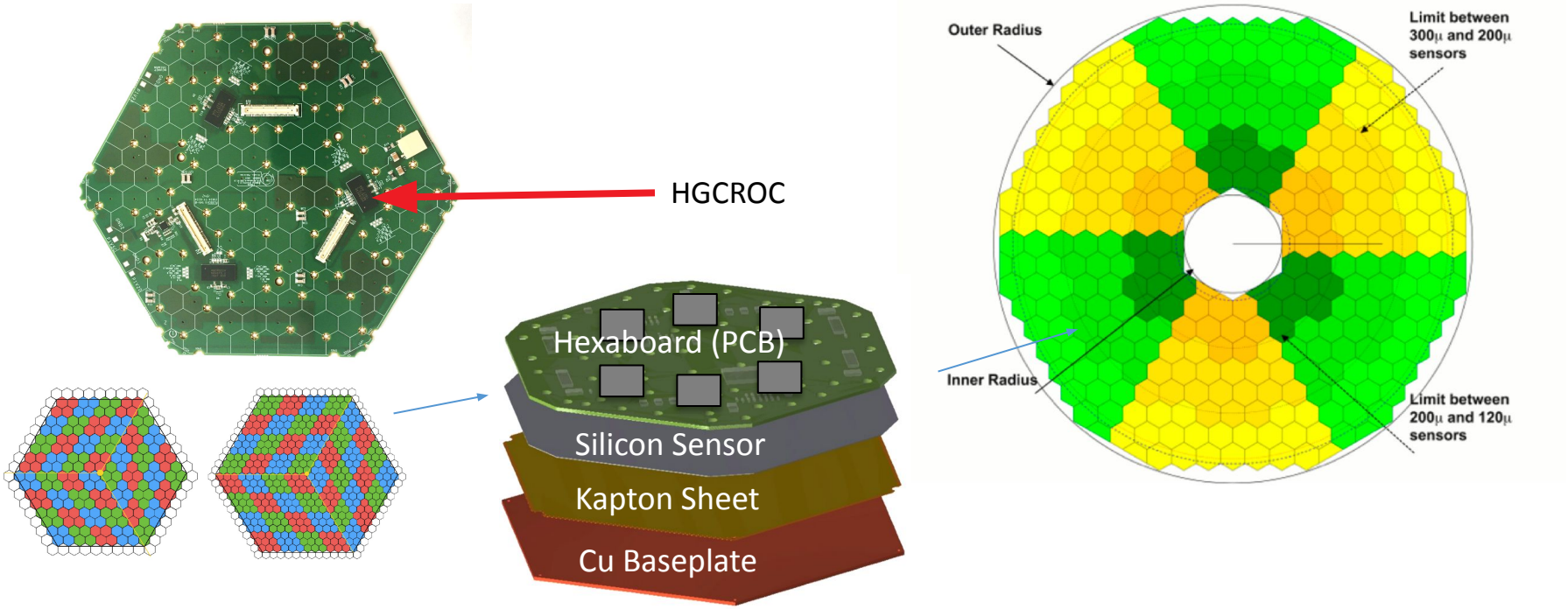



Concept: **remove** complete endcap calo. system and **replace** with HGCAL

CMS internal nomenclature: Calorimeter Endcap (CE), divided into CE-E and CE-H

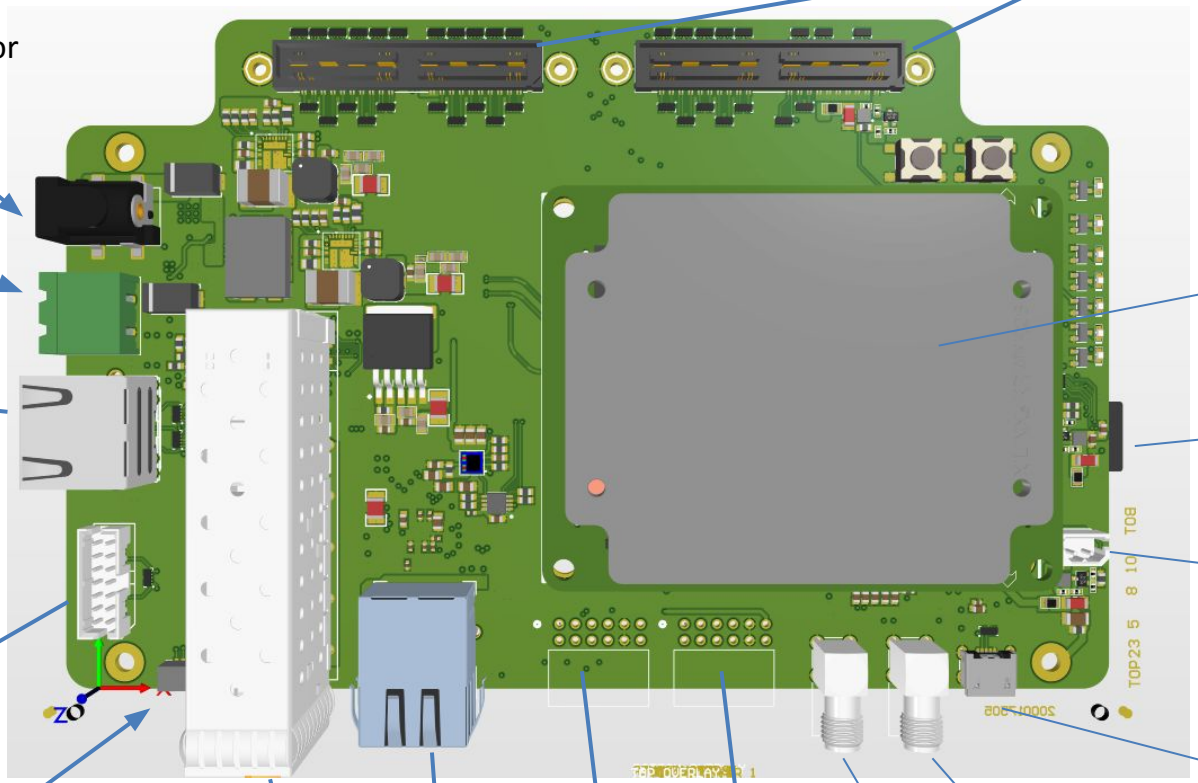
# Hexaboard (Silicon Module to be tested)

- Hexaboard contains ROCs (Read out chips) which also needs  be tested.
- Comes with many shapes and sizes
- Needs to be tested in -40 degrees
- Signals:
  - Enable and reset
  - Power and High Voltage
  - 12 trigger e-links ( 1.28Gb/s per channel) (output)
  - 12 DAQ e-links (1.28 Gb/s per channel) (output)
  - 2  e-links for CLK and TTC ( 320 Mb/s) (input)
  - 3 Slow control configuration and monitoring  I2C signals ( 80 Mb/s) (bi-directional)

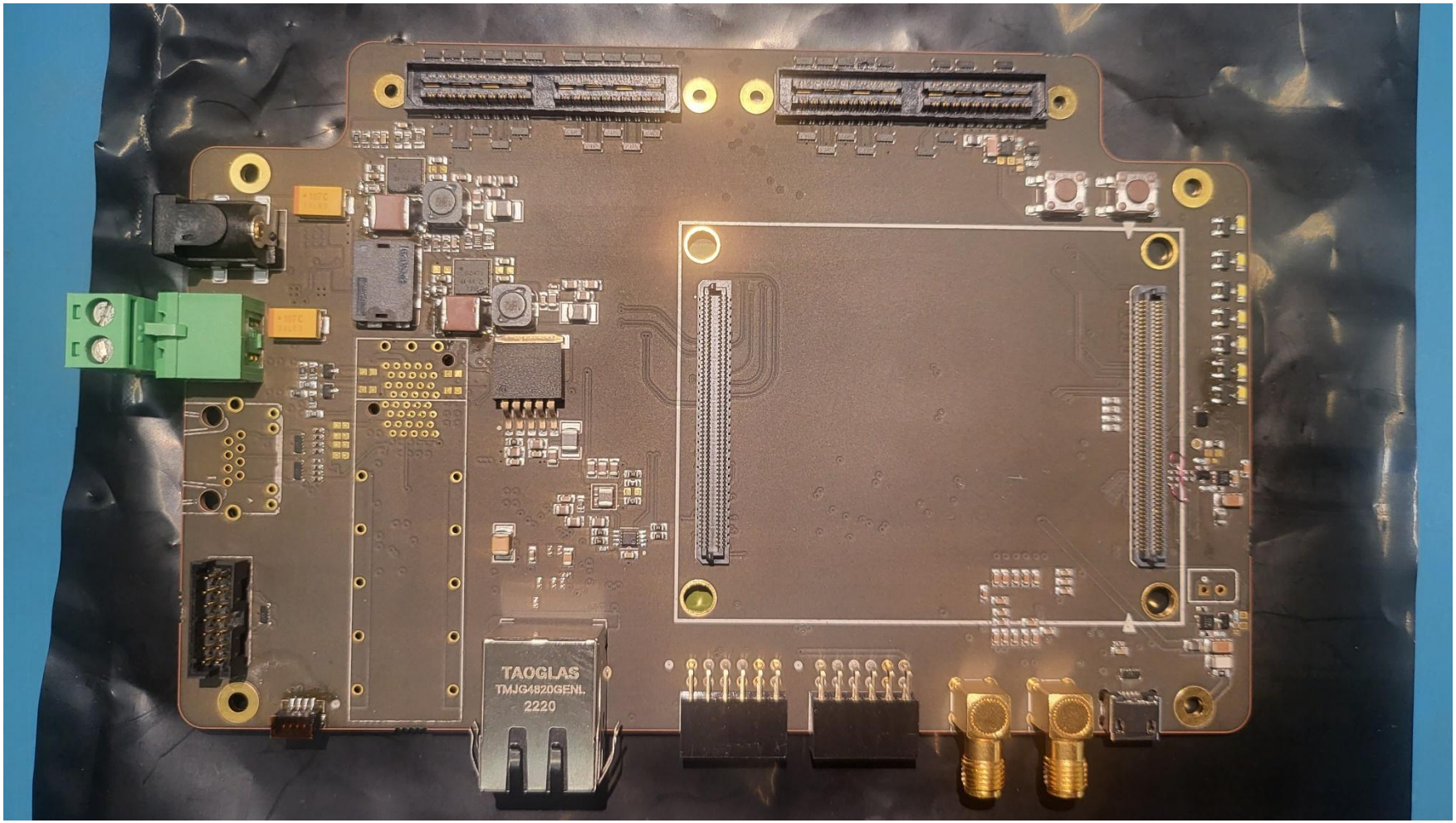


# Hexacontroller (Hexaboard/HGCROC Tester)

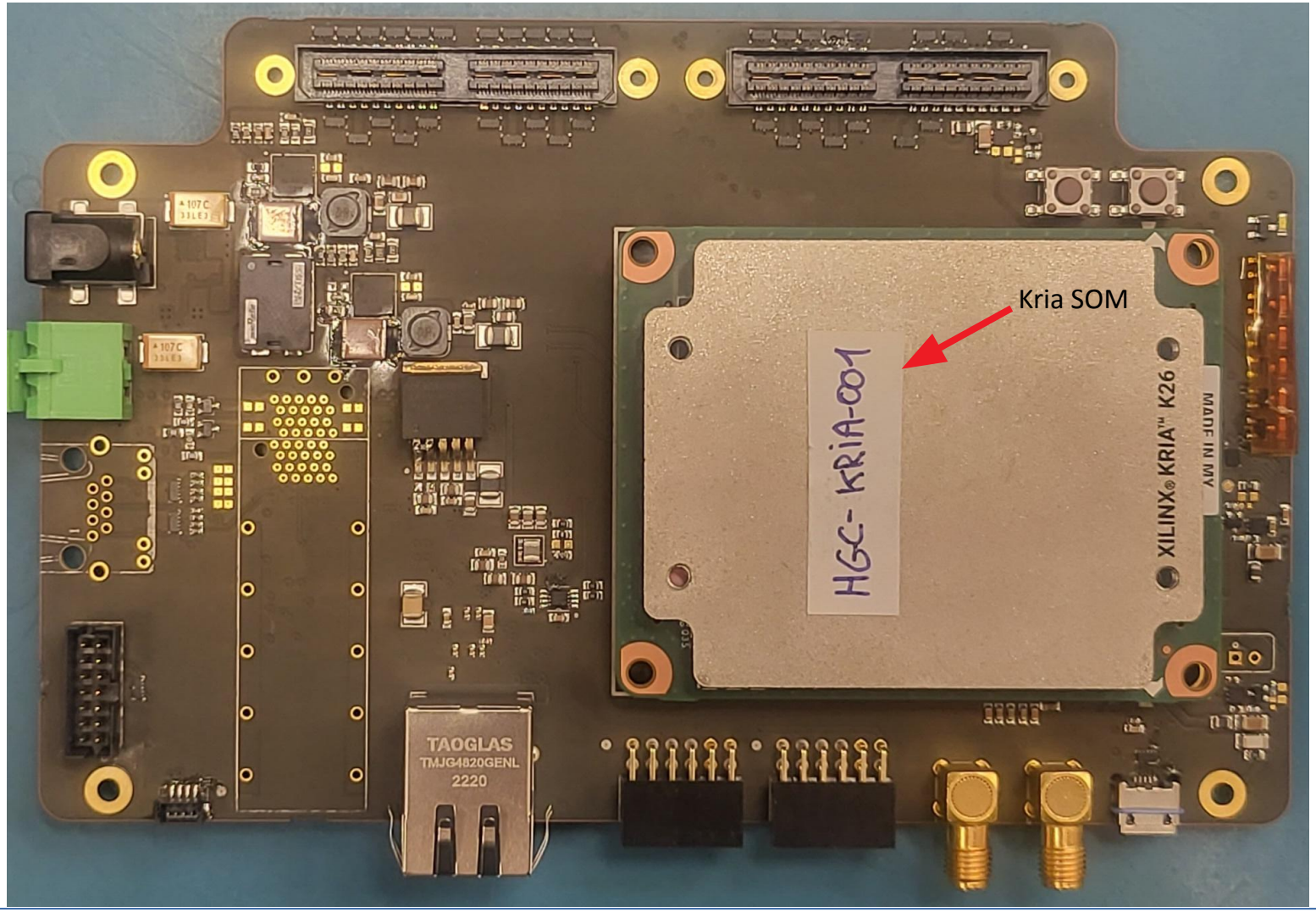
- Reverse polarity and over current  protection has been added for main power regulator.
- All external connectors will be protected with ESD/TVS protection diodes.
- All power outputs will be protected with hot swap switches that can be turned on/off by software.



# HexaController with components:



# HexaController with SOM:



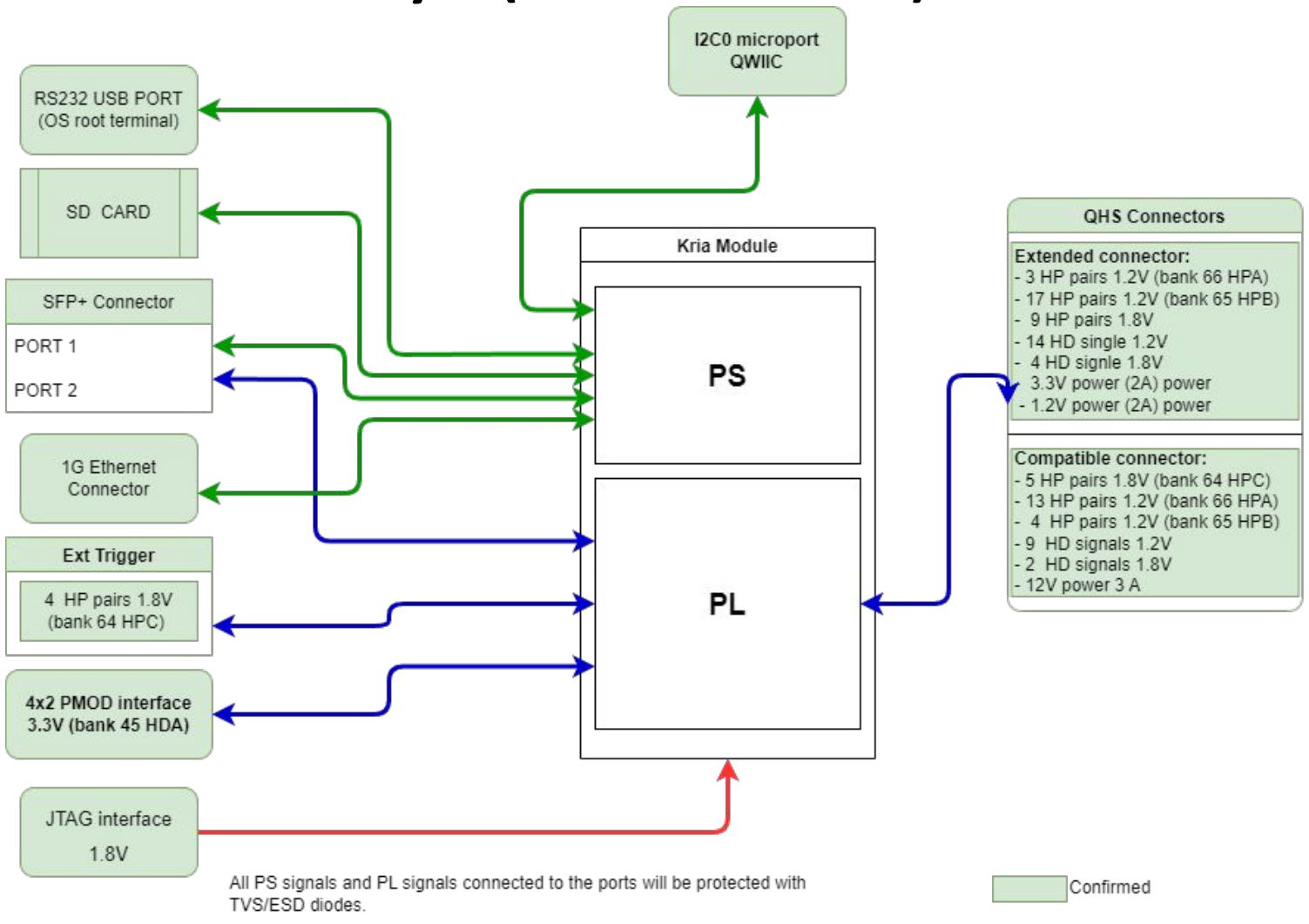
# Kria SOM (System on Module)

- Zynq Ultrascale+ MPSoC FPGA, Quad-core Arm® Cortex® A53
- Memory
  - **4 GB DDR4 RAM**
  - 16 GB eMMC
  - 512 Mb QSPI
- Two 240 pin Connectors for User Configurable I/O
  - High Speed:
    - PCIe® Gen2 x4
    - 2x USB3.0
    - SATA 3.1
    - DisplayPort
    - **Gigabit Ethernet**
    - **SFP+**
  - MIO
    - 2x USB 2.0
    - **2x SD/SDIO,**
    - **2x UART**
    - 2x CAN 2.0B
    - **2x I2C**
    - 2x SPI
    - **4x 32b GPIO**

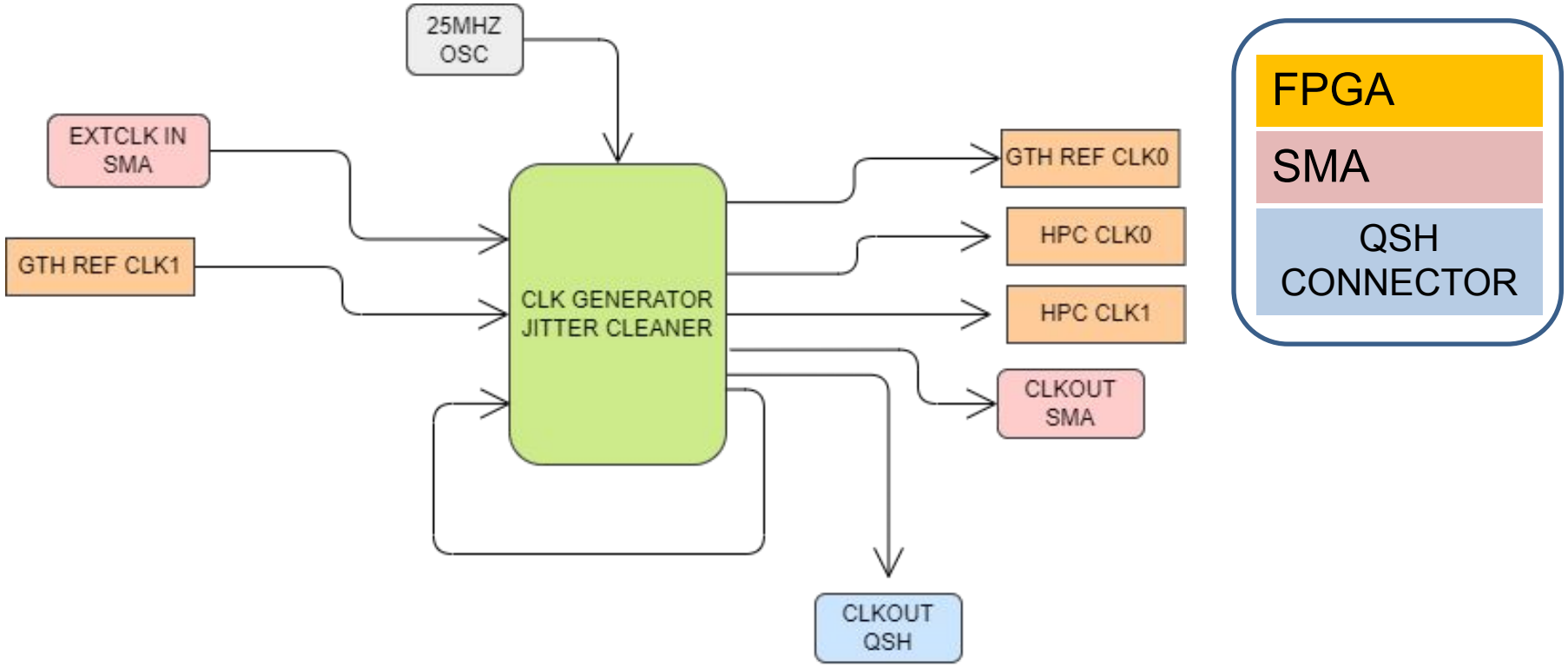
# Tested interfaces:

| TEST | STATUS |
|---|---|
| JTAG access | DONE |
| SDCARD & JTAG boot with custom boot file (FSBL, u-boot, dev-tree, ALMA 9 OS) | DONE |
| UART (Serial Terminal) as boot terminal | DONE |
| MAC address read from EEPROM using I2C. | DONE |
| On boot FPGA configuration | DONE |
| Ethernet connectivity | DONE |
| QWIIC interface | DONE |
| QSH adaptor connectivity test | DONE |
| PMOD connectivity test | DONE |
| SFP+ cage loopback test | DONE |
| Access to debug bridges via Xilinx Virtual Cable | DONE |

# Connectivity (SOM side)

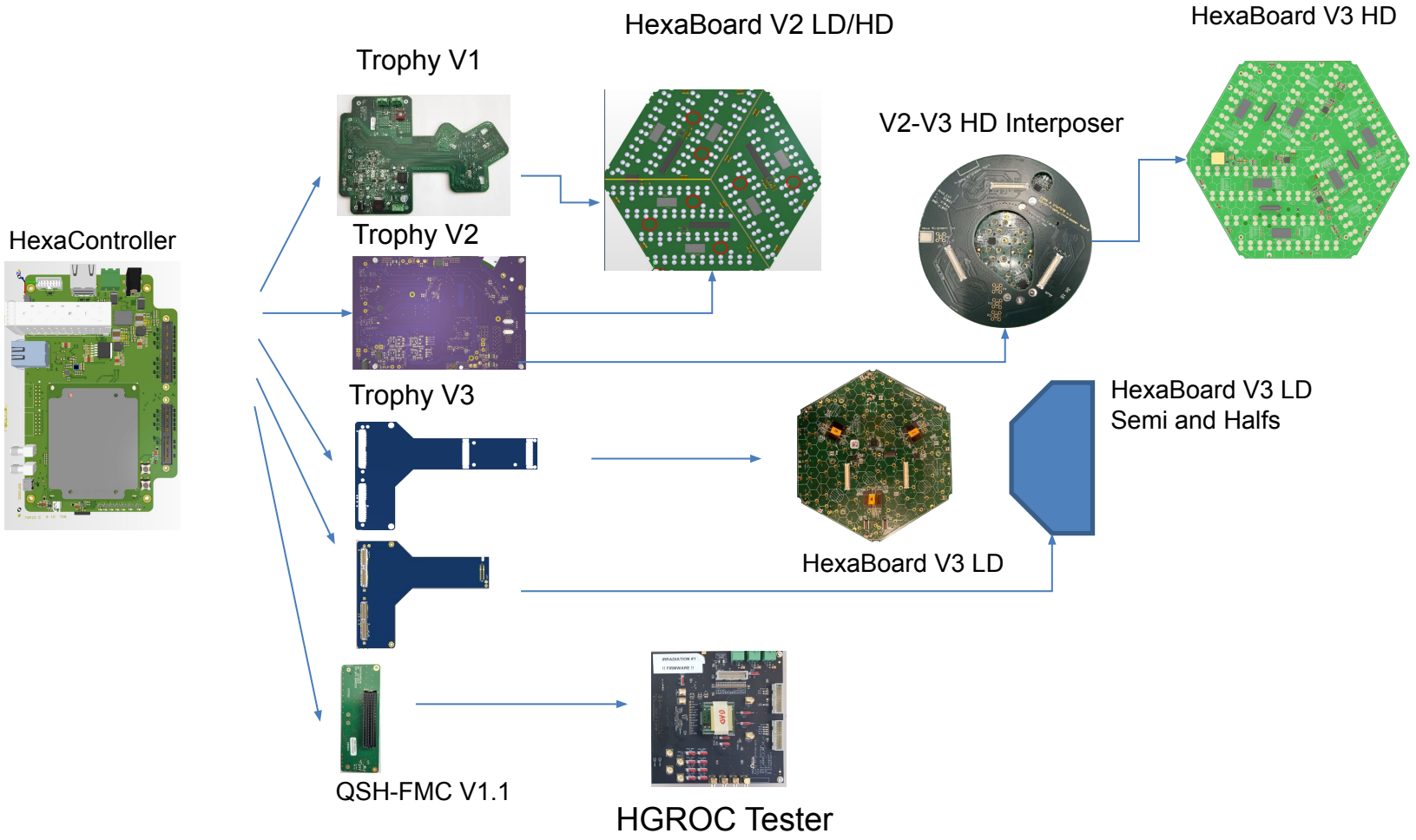


# Clock Generation (ZL30274 microchip)

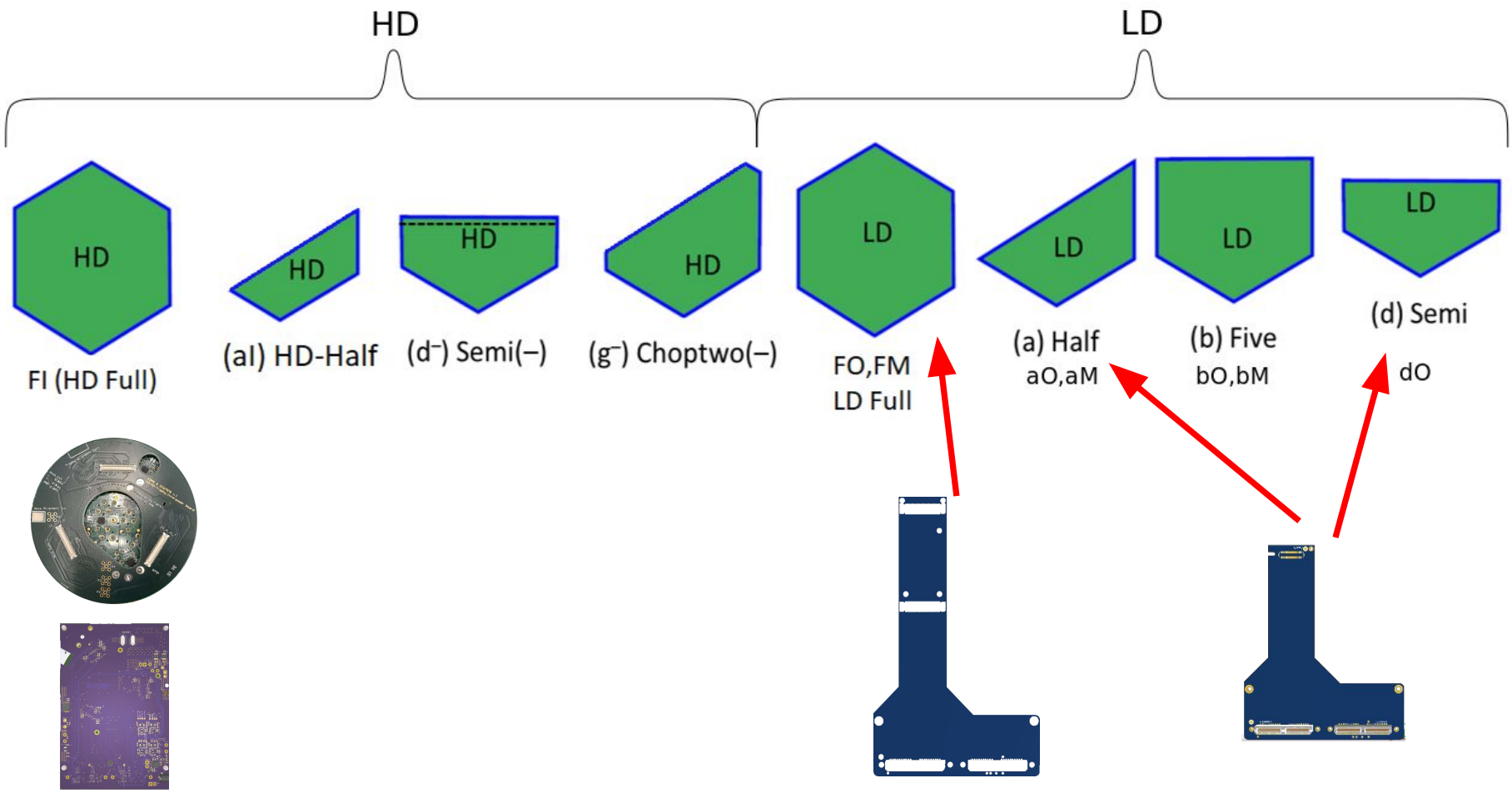


# CMS HGCAL Hexaboard testing system

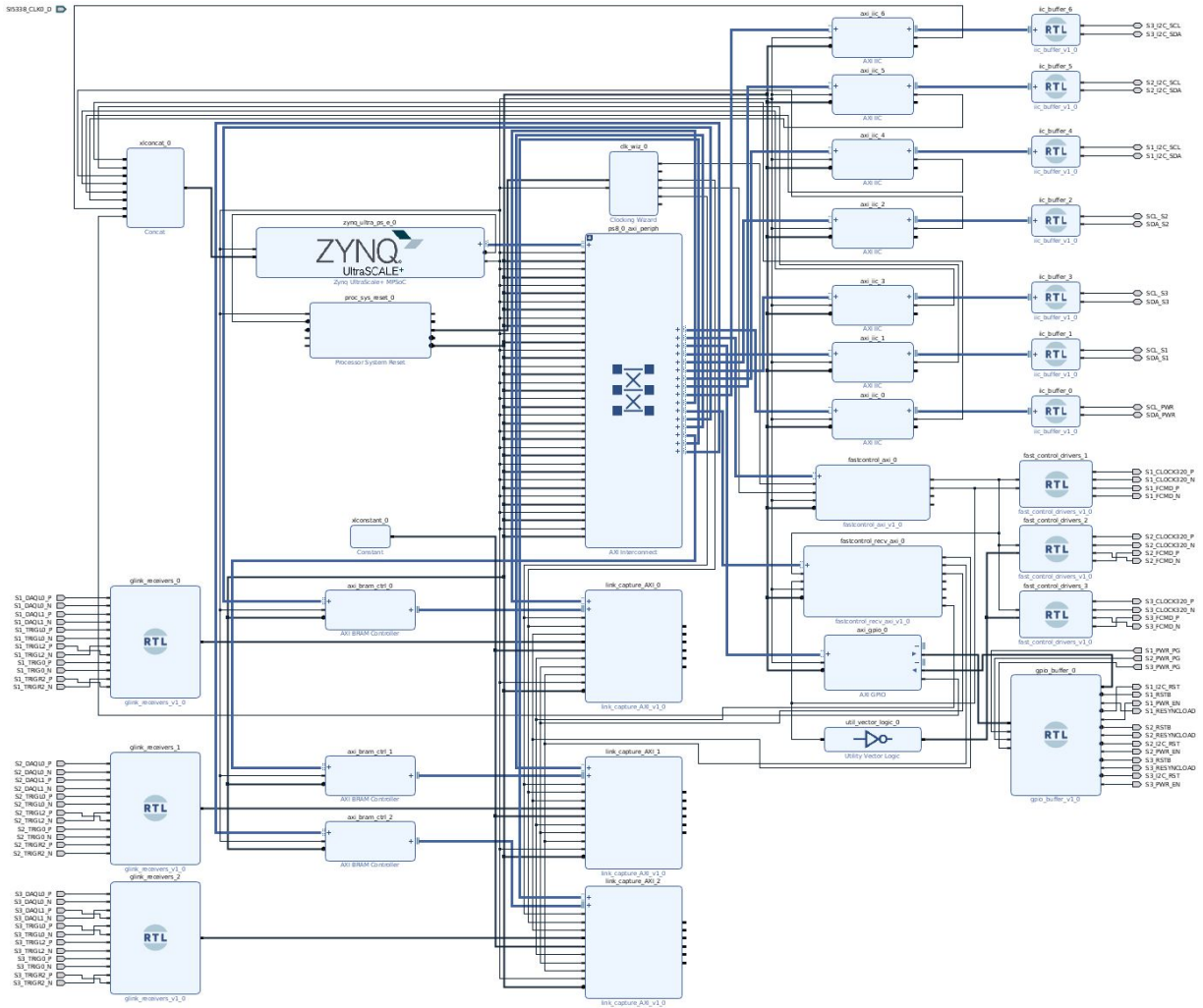
# Usage (QSH Adapter Boards)



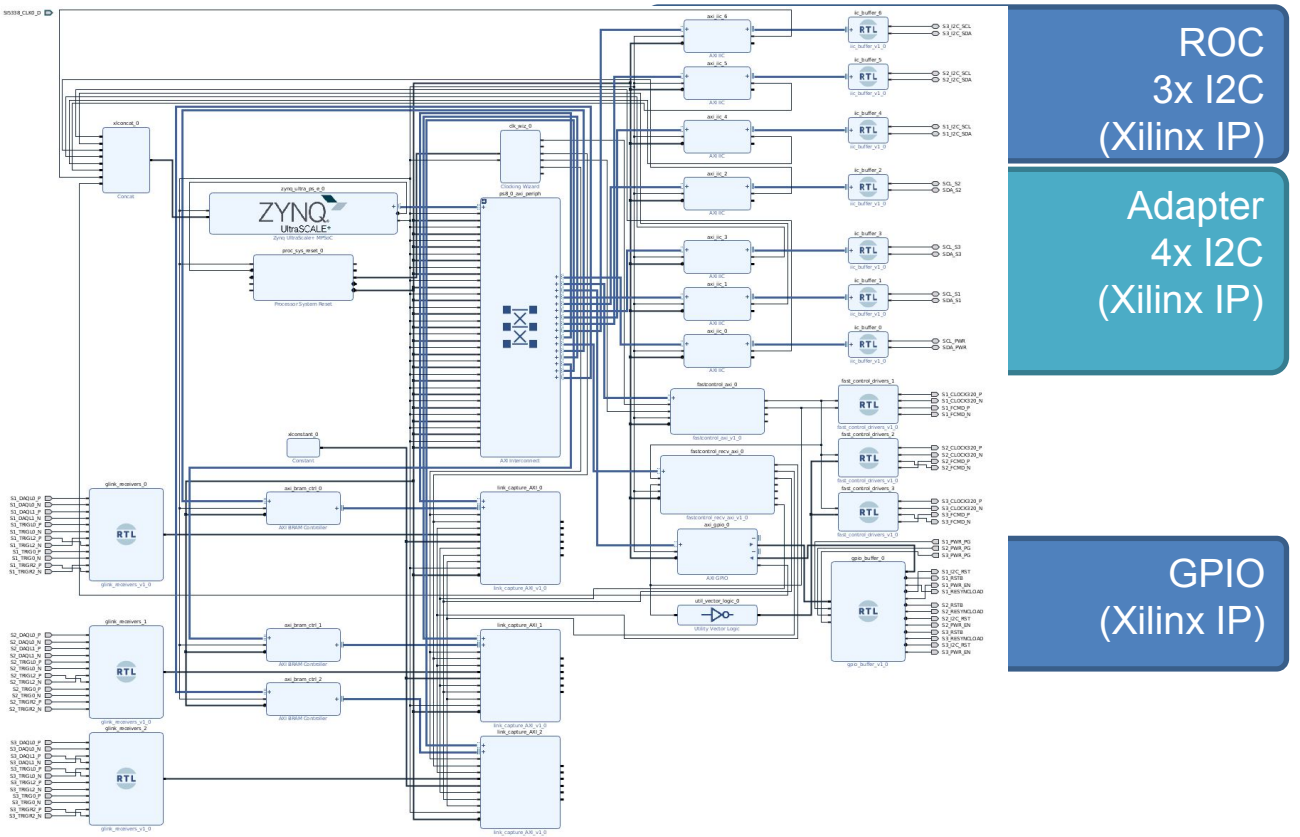
# Hexaboard types and adapters:



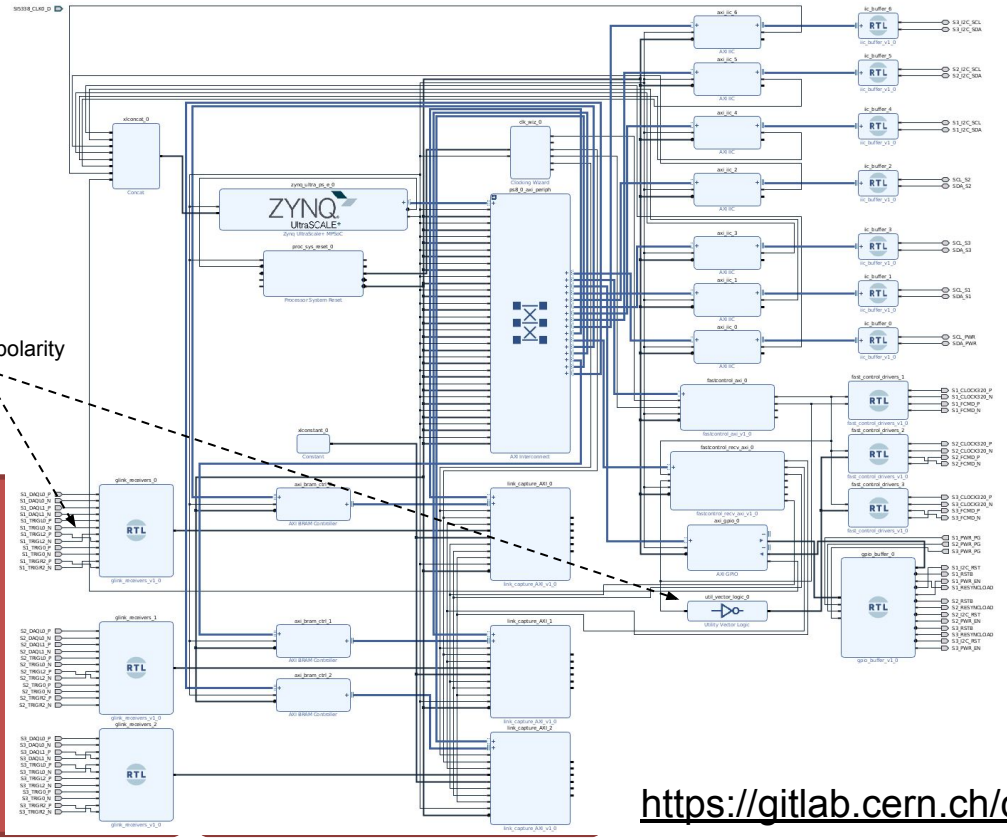
# Example Hexaboard testing Firmware



# Firmware – slow control (configuring and monitoring)



# Firmware – fast control (sending action commands)

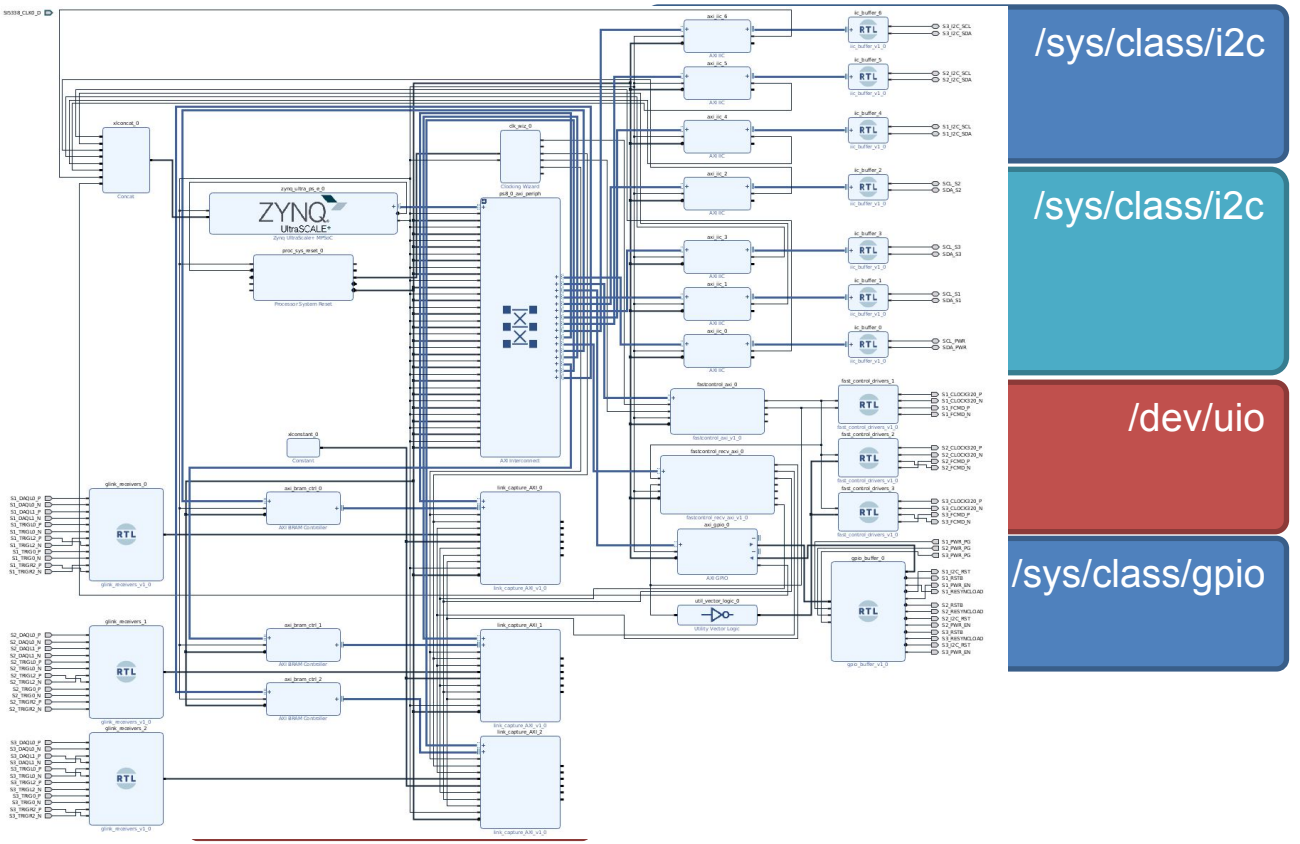



ROC
3x 6x 1.28 G

Clock and fast commands (Tileboard IP)

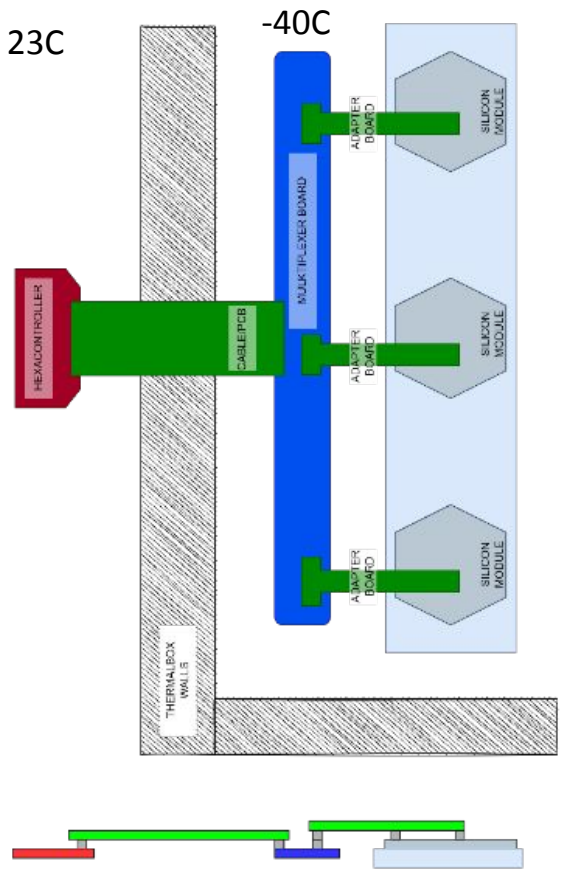
https://gitlab.cern.ch/cms-hgcal-firmware

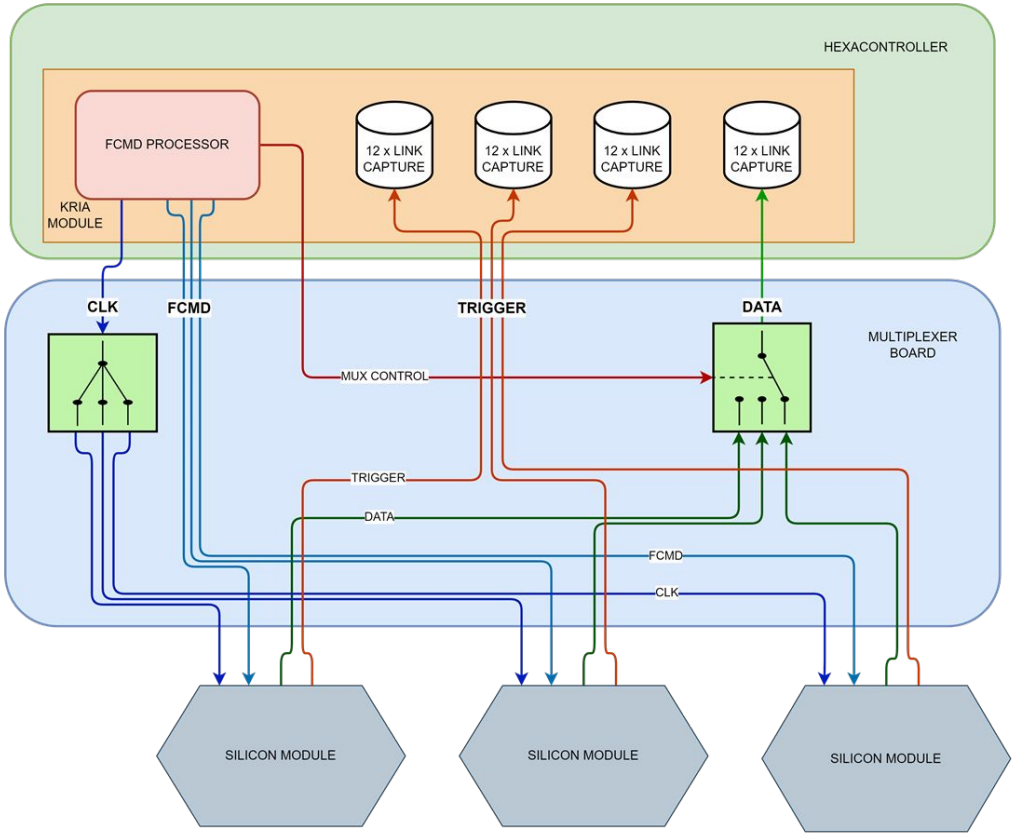
# …as seen from Linux



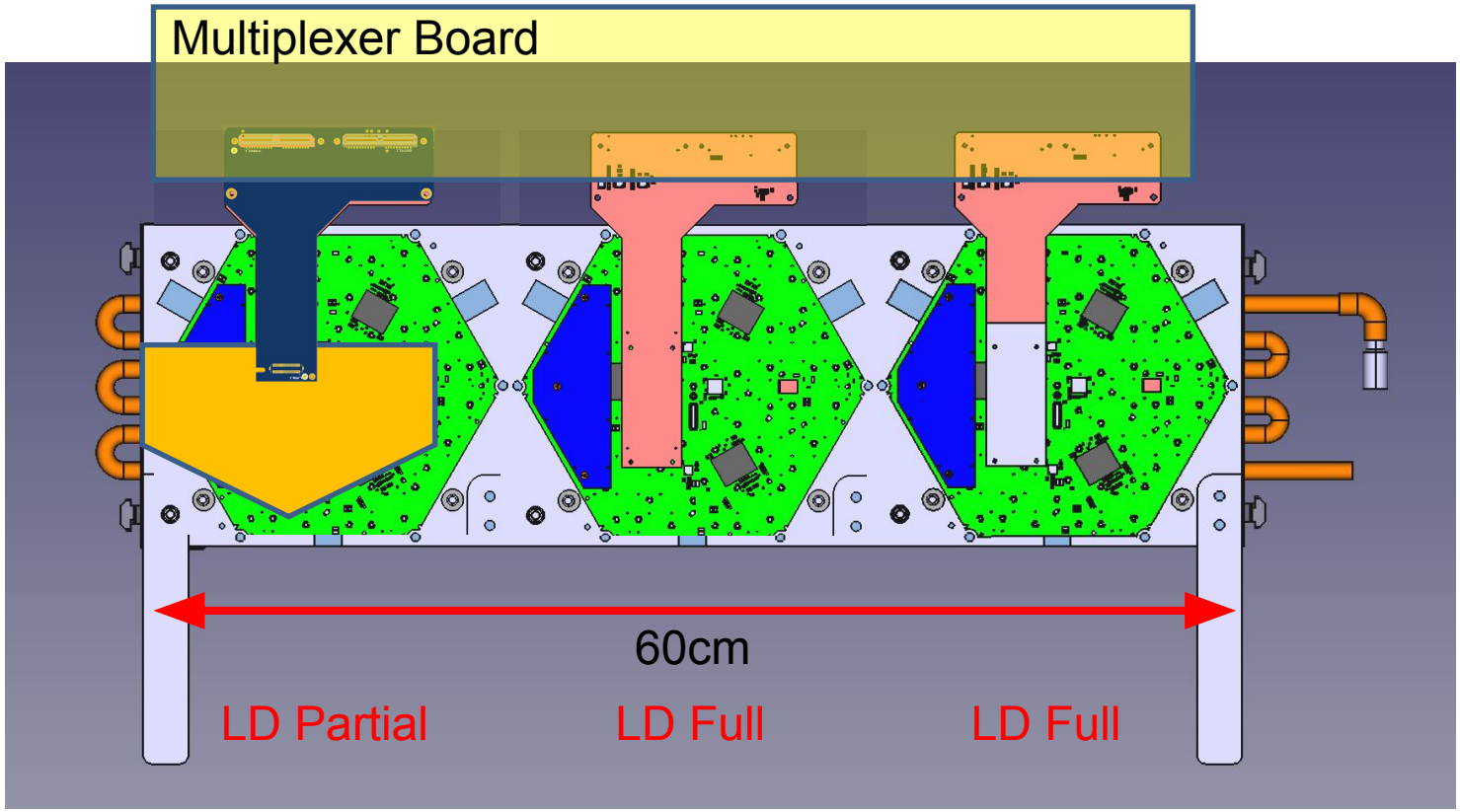
# Hexacontroller with 3 Hexaboards

- Each Data/Trigger line represents 12 signal pairs
- Clk/FCMD lines are single signal pairs.
- MUX control line represents  2 signals for selection of 1 out of 3 .



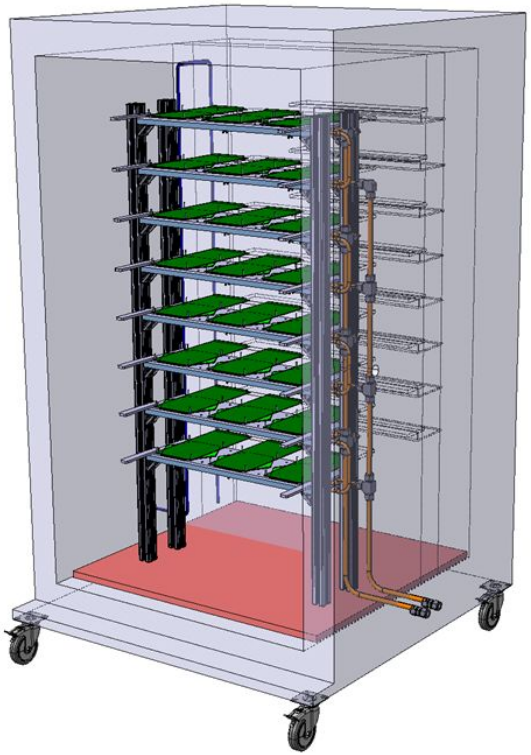



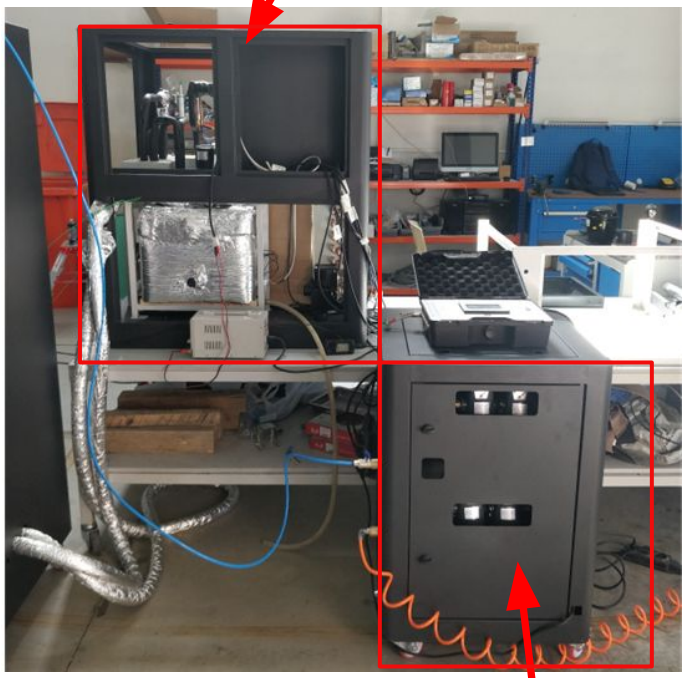
# Cooling plate (Cold Plate) (Mechanical)



# MULTI MODULE TESTER (Mechanical)

A thermal chamber with possibility of testing 24 Full HD/LD silicon modules has been designed.



# MULTI MODULE TESTER (HIGH LEVEL)

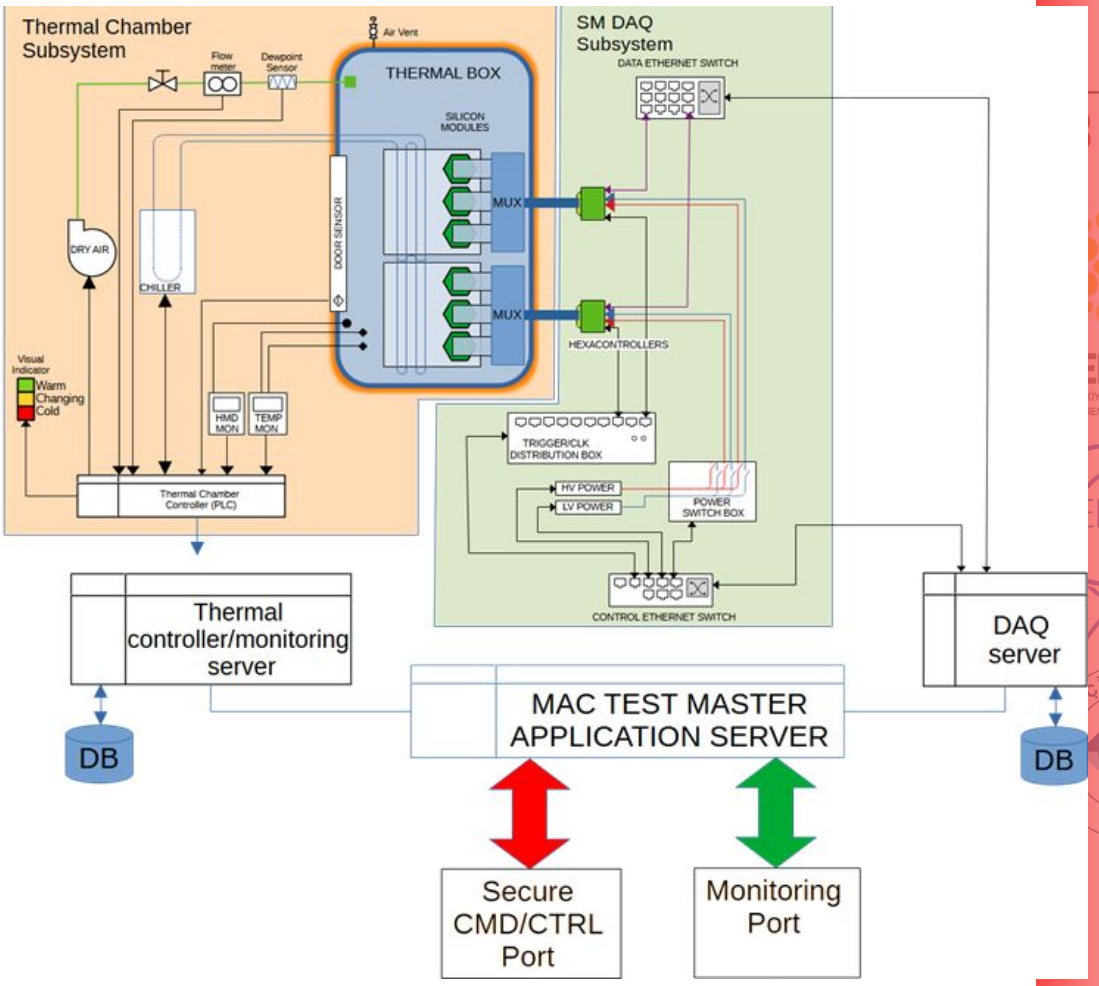
Consists of two major subsystems:

Thermal Chamber

- Chiller controller
- Dry air controller
- Sensors: Thermal and humidity

SM DAQ Subsystem;

- SOC FPGAs: for capturing high speed data
- DAQ server/controller: for evaluating results



# Conclusion

- HGCAL Detector is a state of the art, cutting edge engineering effort.
- Silicon Modules are the main building blocks of HGCAL.
- We are developing Silicon Module qualification and production level test systems.
- Hardware firmware development is ongoing.
- Using Kria as a System-on-Module (SOM) simplifies the focusing on essential design elements.

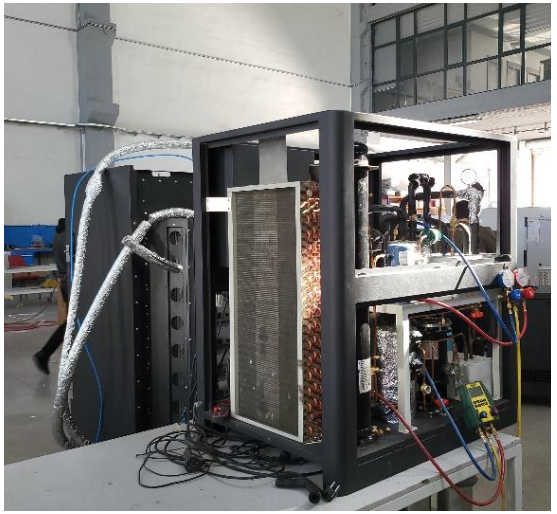
**Thank you**

**Questions?**

# BACKUP

# Current Status of the Thermal Chamber

# Parts of the Thermal Chamber

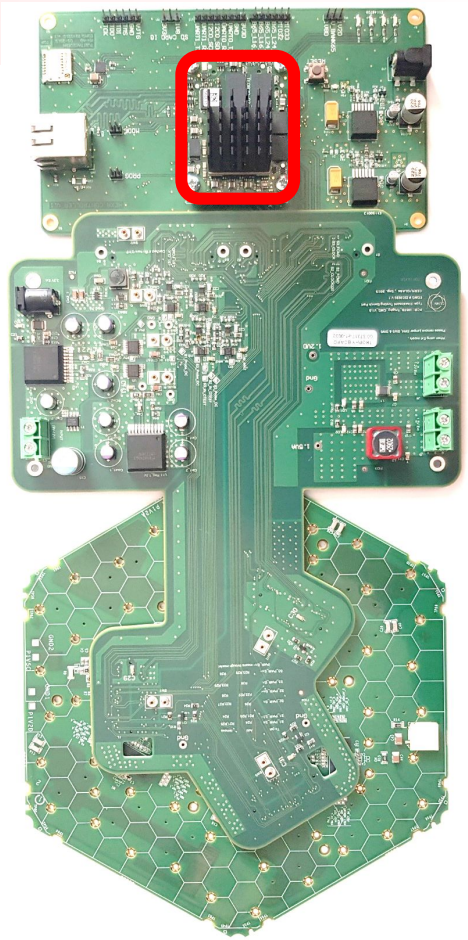


CHILLER ( Left and Right)

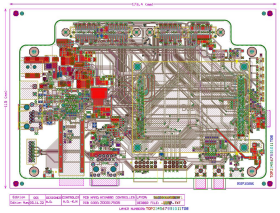
DRY AIR SYSTEM

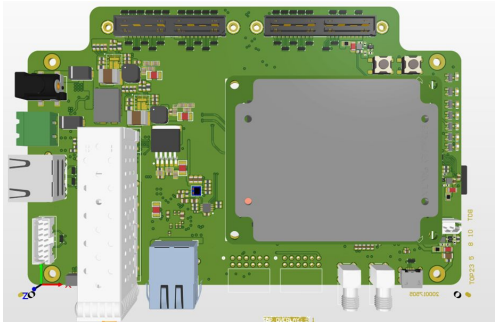
# Software

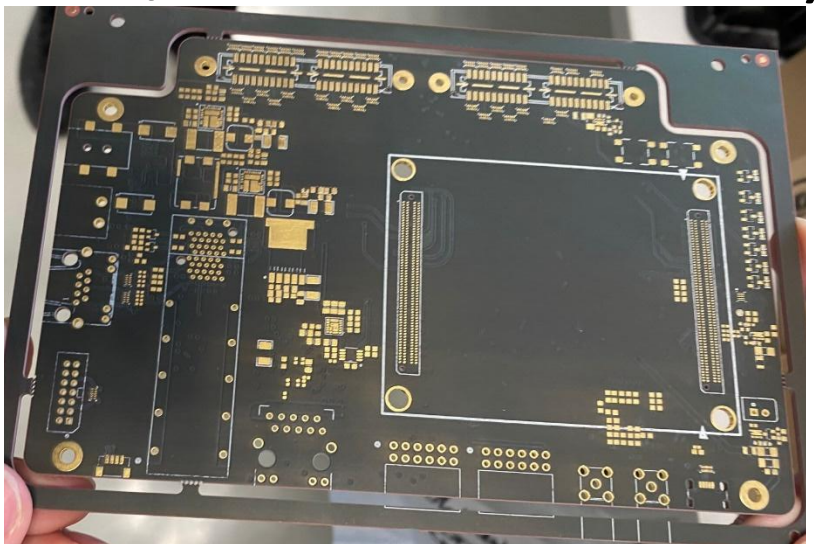
- **Xilinx Ultrascale+ (Trenz TE0820) module running standard CERN CentOS Linux**:
  - FSBL+u-boot+kernel from Petalinux
  - FPGA firmware (bit+dtbo) with overlays
- All test and control software **running on module**:
  - **Standard kernel drivers** (I2C, GPIO, UIO)
  - **ROC I2C software** being ported from KCU
  - **uHAL package** being ported to AXI-over-UIO
- **Focus up to now on validating Hexaboard design and ROC sanity for first module production.**
  - Pedestal and other analysis to come.



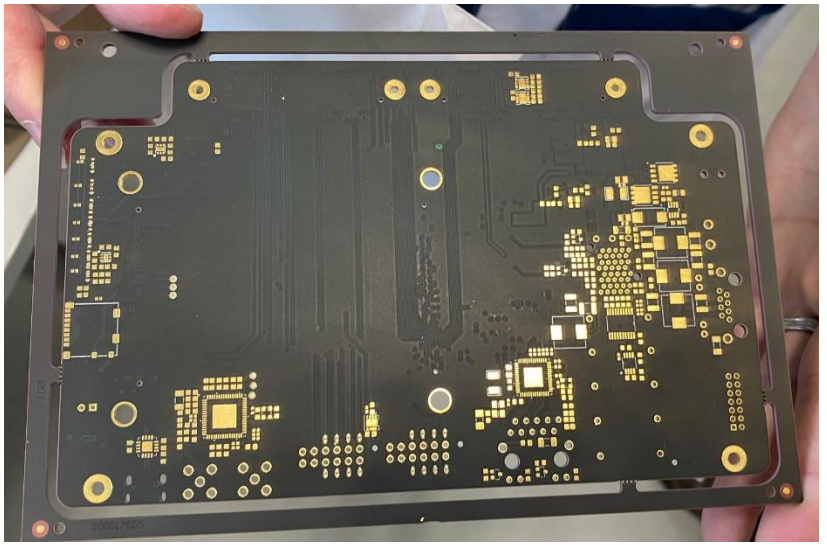
# HexaController (Hexaboard/HGCROC Tester)



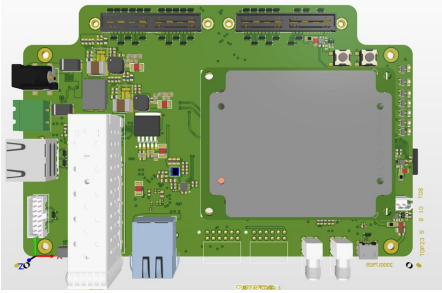




- Single PCB for testing is produced (in CERN workshop)



# What is New with V2.0:



## More protection:

- Reverse polarity and over current protection has been added for main power regulator.
- All external connectors will be protected with ESD/TVS protection diodes.
- All power outputs will be protected with hot swap switches that can be turned on/off by software.

## More IO:

Hexaboard IF:

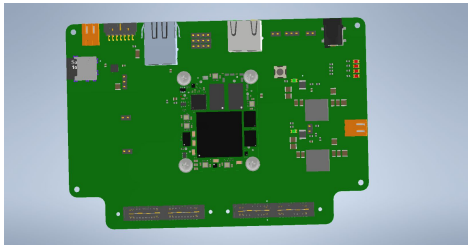
- 1.2V – 1.8V
  - 23 Single
  - 37 Differential
- 1.8V
  - 6 Single
  - 14 Differential

51 Differential I/O

29 Single Ended I/O

Other Interfaces:

- 4 x Differential signal on RJ45 connector.
- External Clock Input/output with SMA connector
- 2 x PMOD (8 single ended )
- QWIIC (I2C) interface



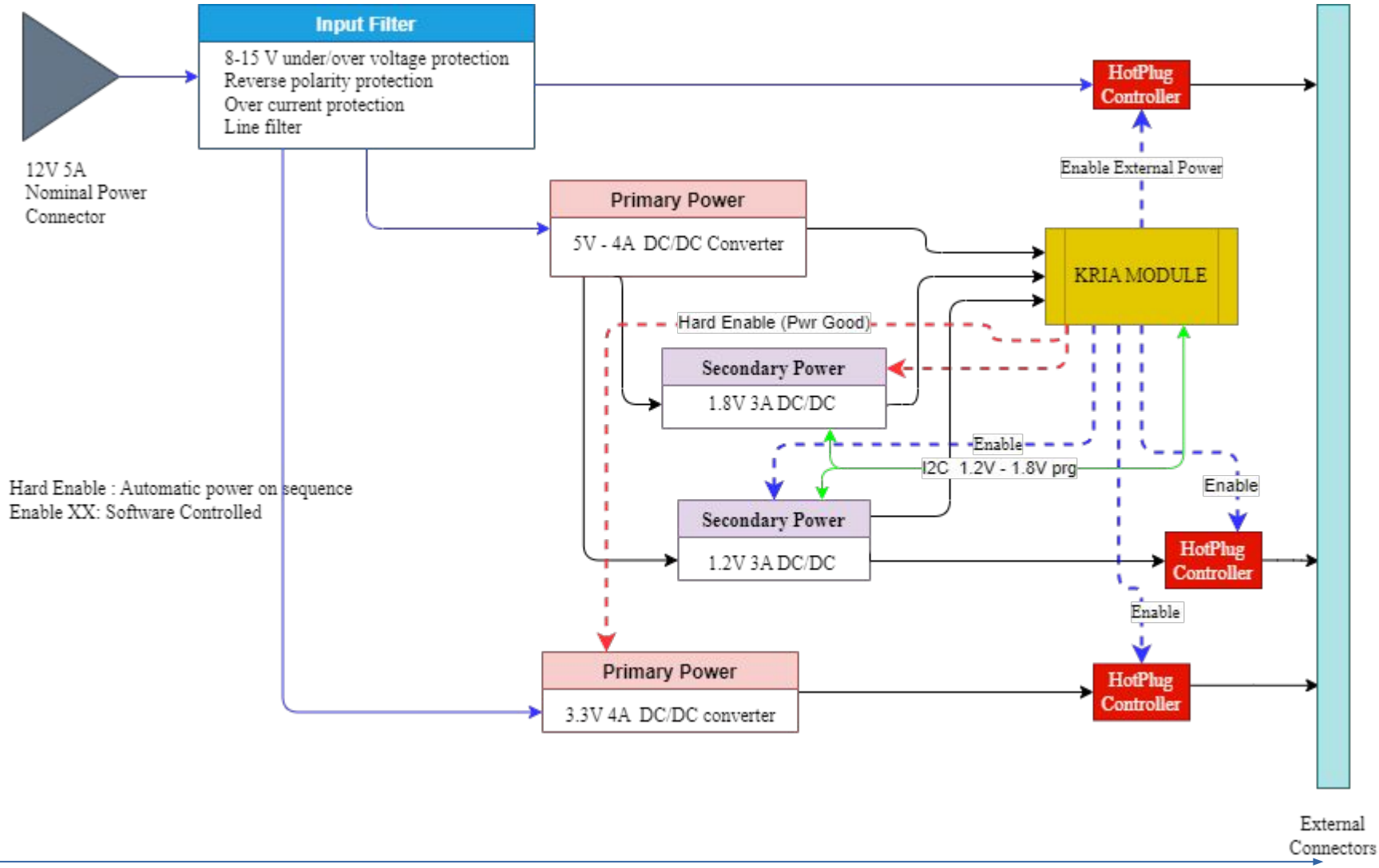
Hexaboard IF (95 IO)

- 31 low speed single ended I/O
- 30 high speed differential I/O ( 3x4 data + 3x4 trg + 3 clk320 +3 fcmd )

Trigger IF: (8 IO)

- 4 x Differential signal on RJ45 connector.

# KRIA Power Distribution



# Conclusions & Discussion :

HexaController V2.0:

- The new Hexacontroller 2.0 is almost ready for electrical testing.
- The electronic components to build more Hexacontrollers are available for the moment
- The necessary firmware and support scripts will be produced for hexacontroller V2.0
- This design will enable us to test up to 3 full HD  silicon modules in parallel.

HB Trophy Adapter Boards:

- More adapter boards shall be prepared for testing HD Hexaboard partials
- Multi module test adapter  shall be built for Silicon Modules
- Operability with the tileboards ?