Device Structures: planar and 3D

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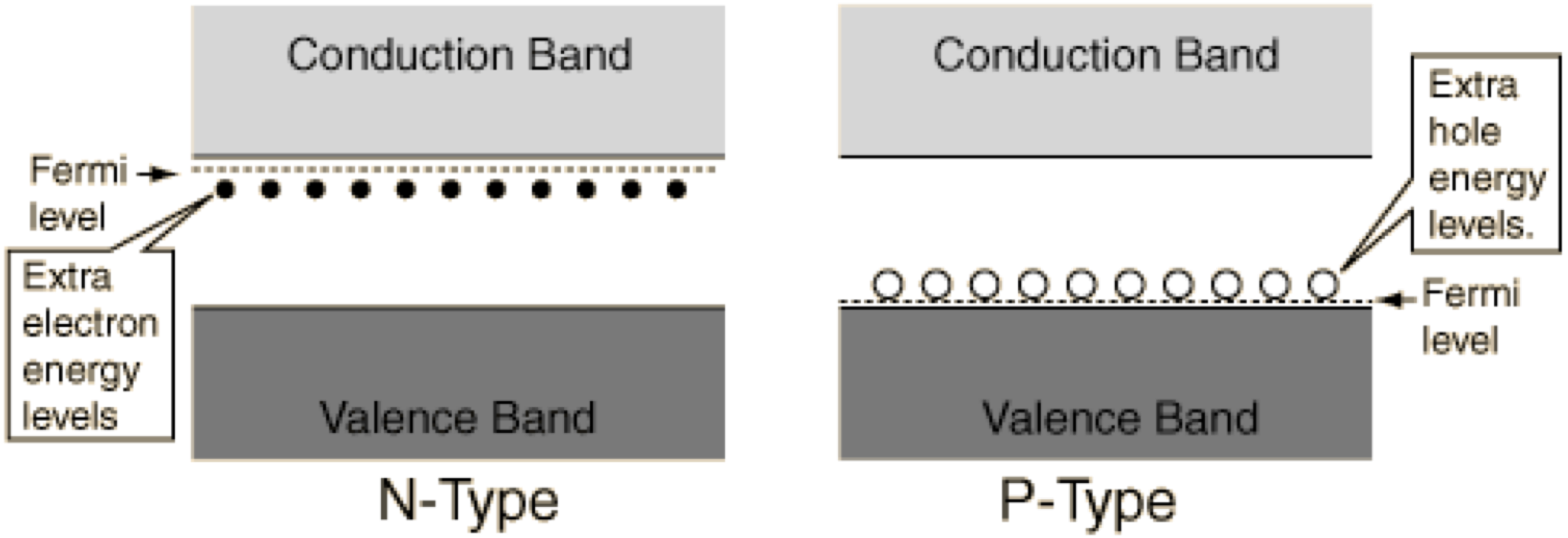
Semiconductor sensors basics [1]

Doping:

- Impurities are introduced to displace Si- Fermi level
  - Donors: dopants adding free e in the conduction band (group V, P)
  - Acceptors: dopants adding holes in the valence band (group III, B)
- N – type: excess of e^- in the conductive band
- P – type: excess of h^+ in the valence band



Semiconductor sensors basics [1]

PN- junction:

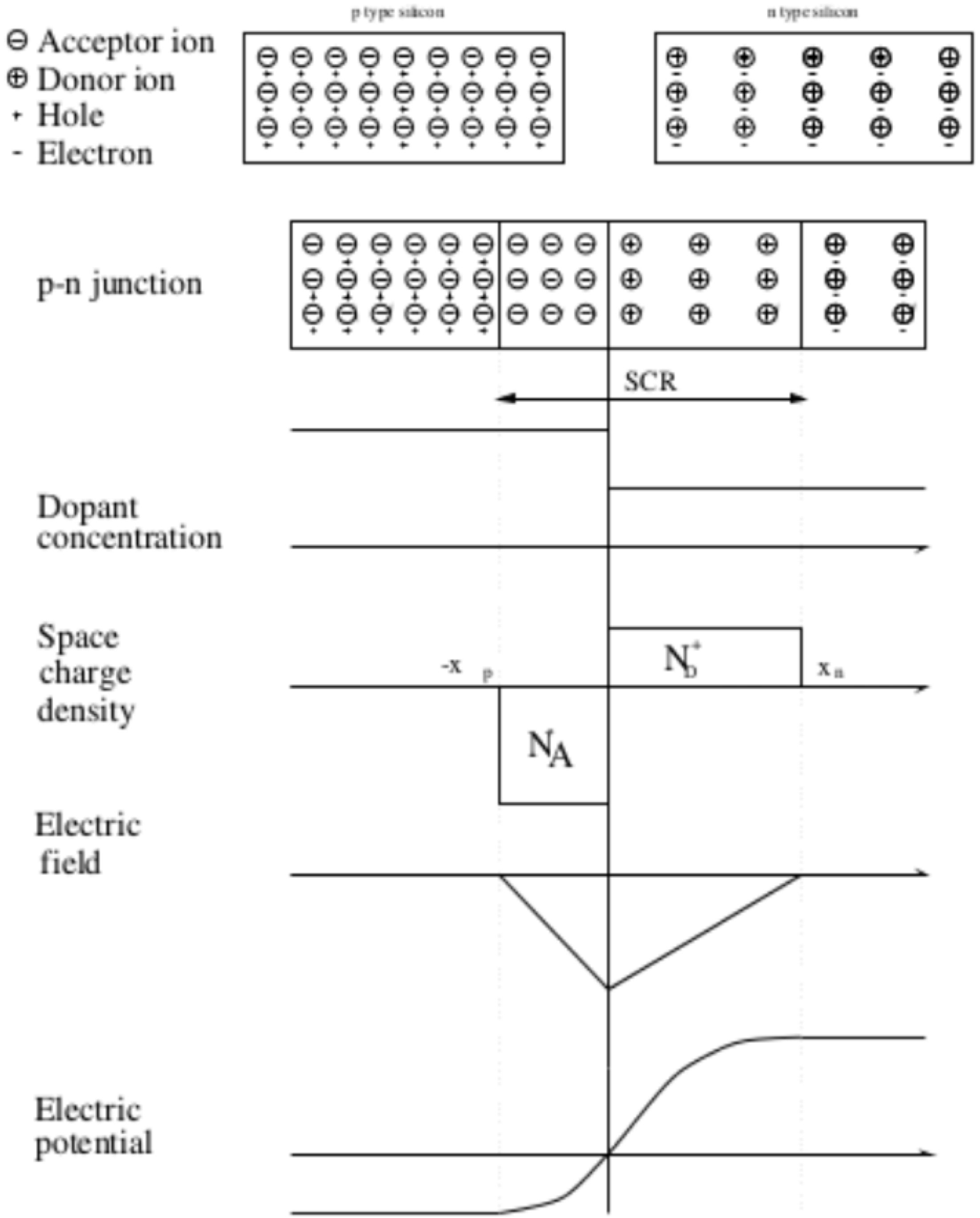
- The gradient of e^- and h^+ densities causes diffusion and carriers recombine until the diffusion stops
- An electric field is created because now part of the p-type has a net negative charge and the opposite occurs to the n- type

$$V_{bi} = \frac{e_0}{2\epsilon_{Si}\epsilon_0}(N_D X_n^2 + N_A X_p^2)$$

Intrinsic pn- junction buil-in potential (~0.5-1V)

Applying electrical neutrality $N_A X_p = N_D X_n$

$$|N_{eff}| = N_D - N_A$$

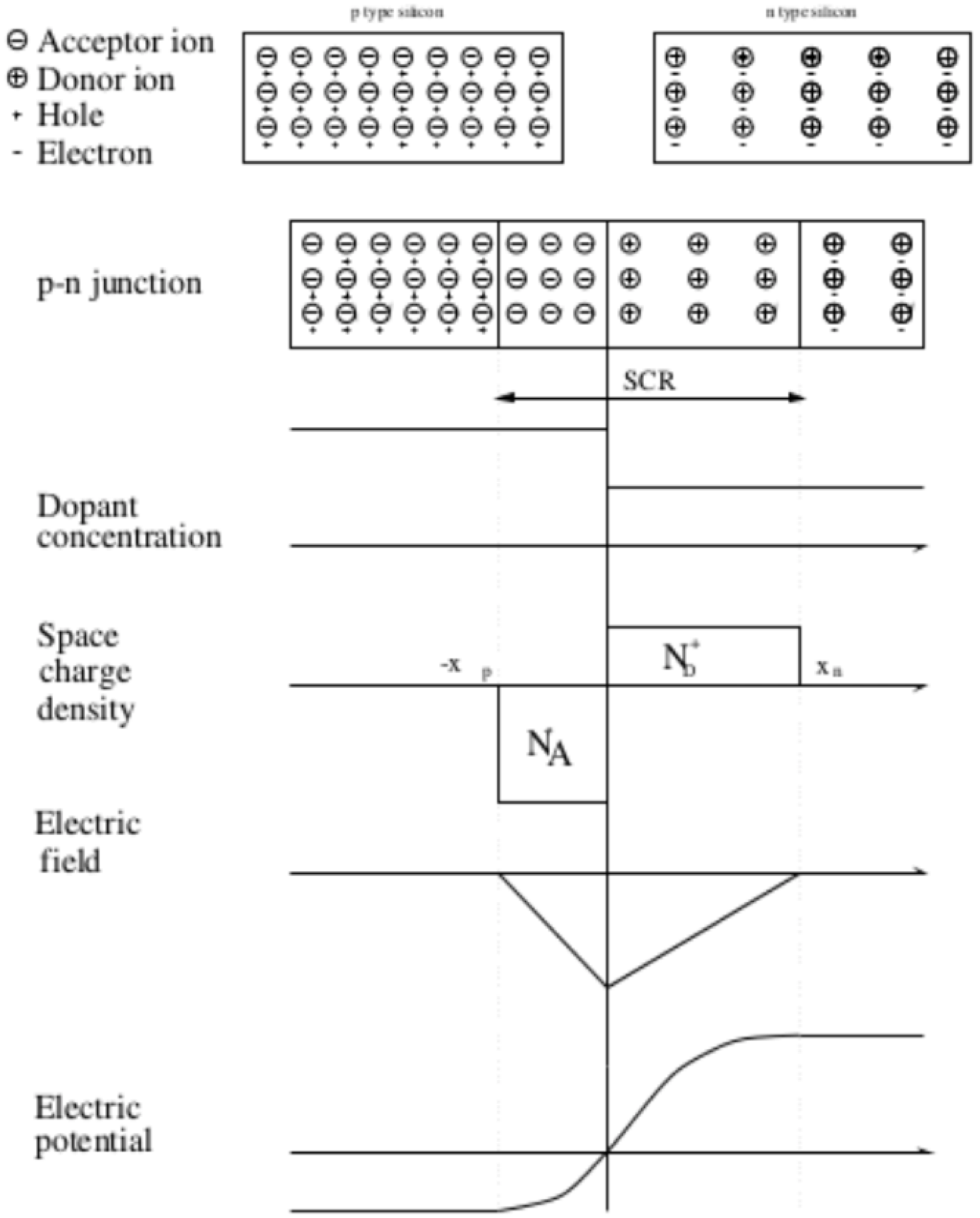


Semiconductor sensors basics [1]

- The area created is called Depletion area and is an area with low carriers concentration ~100 carriers/cm^3, while in p or n type ~ 10^{10} carriers/cm^3.

Depletion width
$$W = \sqrt{\frac{2\epsilon_{Si}\epsilon_0}{e_0}\frac{V_{bi}}{|N_{eff}|}}$$

- To extend that area an external bias (V_{bias}) can be added with the same polarity than the V_{bi}



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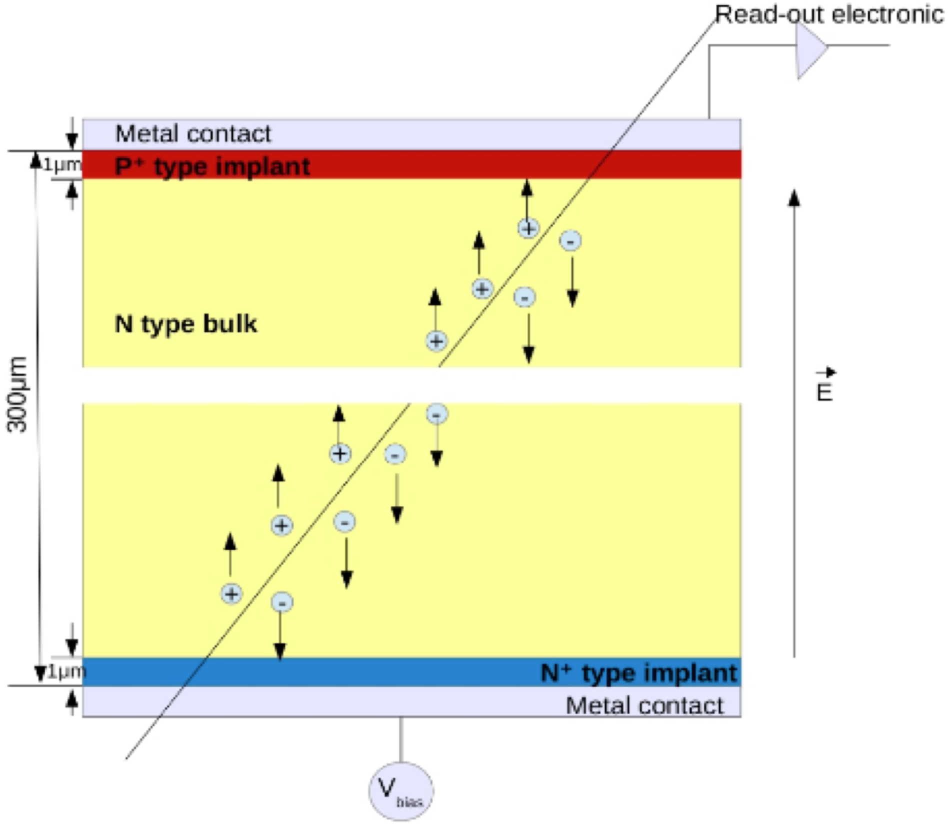
Semiconductor sensors basics [2]

- Silicon diode:
    - PN-junction
    - Ohmic contact to avoid a 'Schottky contact'
    - External voltage (V_{bias}) on top of the built-in voltage to make depleted area bigger ($V_{bias} >> V_{bi}$)

$$W(V_{bias}) = \sqrt{\frac{2\epsilon_{Si}\epsilon_0}{e_0 \cdot |N_{eff}|} V_{bias}}$$

- The Voltage needed to fully deplete the device is called full depletion voltage (D=distance between electrodes):

$$V_{FD} = \frac{e_0 N_{eff} D^2}{2\epsilon_{si}\epsilon_0} (\propto D^2)$$



Q1: Why do we choose Si? Can we build the same devices with other semiconductors? Which ones for what applications?

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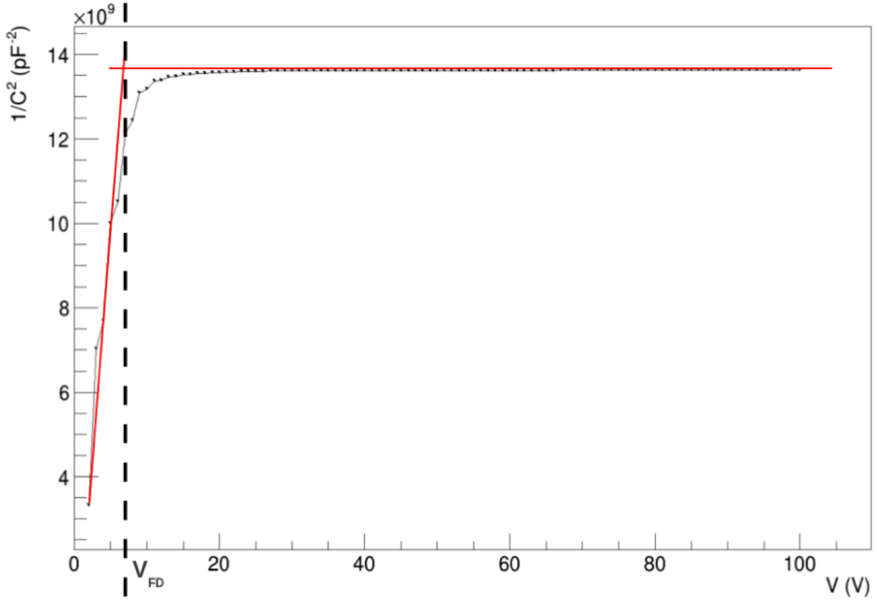
Semiconductor sensors basics [2]

- For practical reasons, the most used magnitude is the capacitance:

$$\frac{1}{C^2} \propto \begin{cases} V_{bias} & \text{if } V_{bias} < V_{FD} \\ D^2 & \text{if } V_{bias} \geqslant V_{FD} \end{cases}$$



- Signal generation:
  - Free carriers in movement (Ramo's theorem):
    - Thermal generation (energy gap small)
    - Electromagnetic radiation (γ- absorption)
    - Charged particles. Bethe-Bloch Formula → MIP, 89 e/um
  - Amplifier + ADC (analogue to digital converter)

Q1: Why do we choose Si? Can we build the same devices with other semiconductors? Which ones for what applications?

Semiconductor sensors basics. Noise [2]

- The position resolution is determined by the signal-to-noise ratio. To minimising the noise is always beneficial.
- Noise due to have carriers in movement (I) :
  - Thermal noise: noise due to the thermal fluctuations of the carriers: $i_n^2 = \frac{4kT}{R}$
  - Low frequency noise: inversely proportional to the frequency. Carriers get trapped in crystal defects and then released with a time constant τ :
$$i_n^2 \propto \frac{1}{f}$$
  - Shot noise: is a consequence of the carriers charge discreteness and it generates time dependent fluctuations in the current $i_n^2 = 2eI$

In general, the sensor leakage current will contribute with shot noise, resistors with thermal noise and the input transistor contributes with two components, shot and low frequency noise.

- Any noise before the amplifying chain, will get amplified together with the signal.

Semiconductor sensors basics. Noise [2]

- The total noise of a detector system measured as ENC (Equivalent Noise Charge) at the input of the amplifier is given by adding noises due to the leakage current ENC_i, parallel resistors as thermal noise ENC_{th}, resistors in series in the circuit ENC_S and the noise due to the preamplifier frequency response ENC_{pa}

$$ENC_{tot}^2 = ENC_i^2 + ENC_{th}^2 + ENC_S^2 + ENC_{pa}^2$$

$$ENC_i^2 \propto I_{leak,a} \cdot \tau \quad ; \qquad ENC_{th}^2 \propto \frac{T \cdot \tau}{R_b}$$

$$ENC_S^2 \propto \frac{C^2 \cdot R_s}{\tau} \quad ; \qquad ENC_{pa}^2 \propto A(f) \cdot C^2$$

τ = peaking time, C = Capacitance at the input of the amplifier, A(f) = low frequency noise term

- A high peaking time increases the leakage current contribution to the noise but decreases the one due to serial resistors. Regarding the detector and its characteristics, one should reduce their leakage current, the series resistance and the total capacitance and increase the bias resistor resistance.
- $C \propto 1/d^2$, d= distance between electrodes

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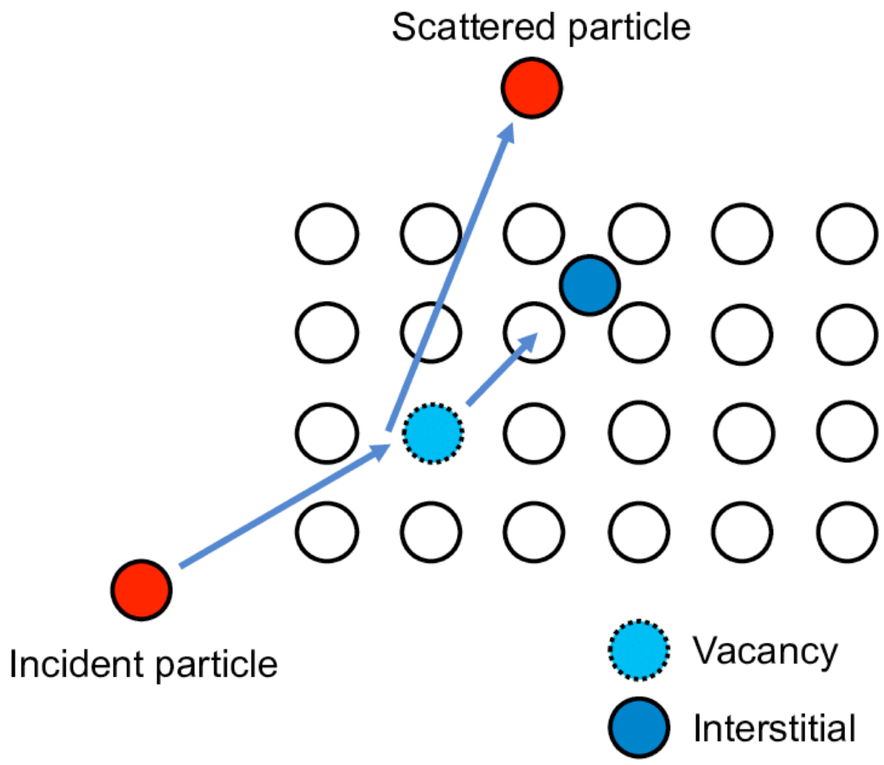
Radiation damage effects in silicon detectors [2].

**Radiation damage dedicated lectures for more in-deep understanding*

- Semiconductor detectors can be exposed to radiation that induce defects in their crystalline structure:
  - Introducing new energy levels:
    - Acting as a **dopant** if it close to one band
    - As an e-h generator if it is very deep on the band
  - *Frenkel pair* is formed when one atom is displaced creating an *interstitial defect* plus a *vacancy*. With enough energy absorbed can create clusters of defects.
    - Frenkel pairs have very high mobility at room temperature



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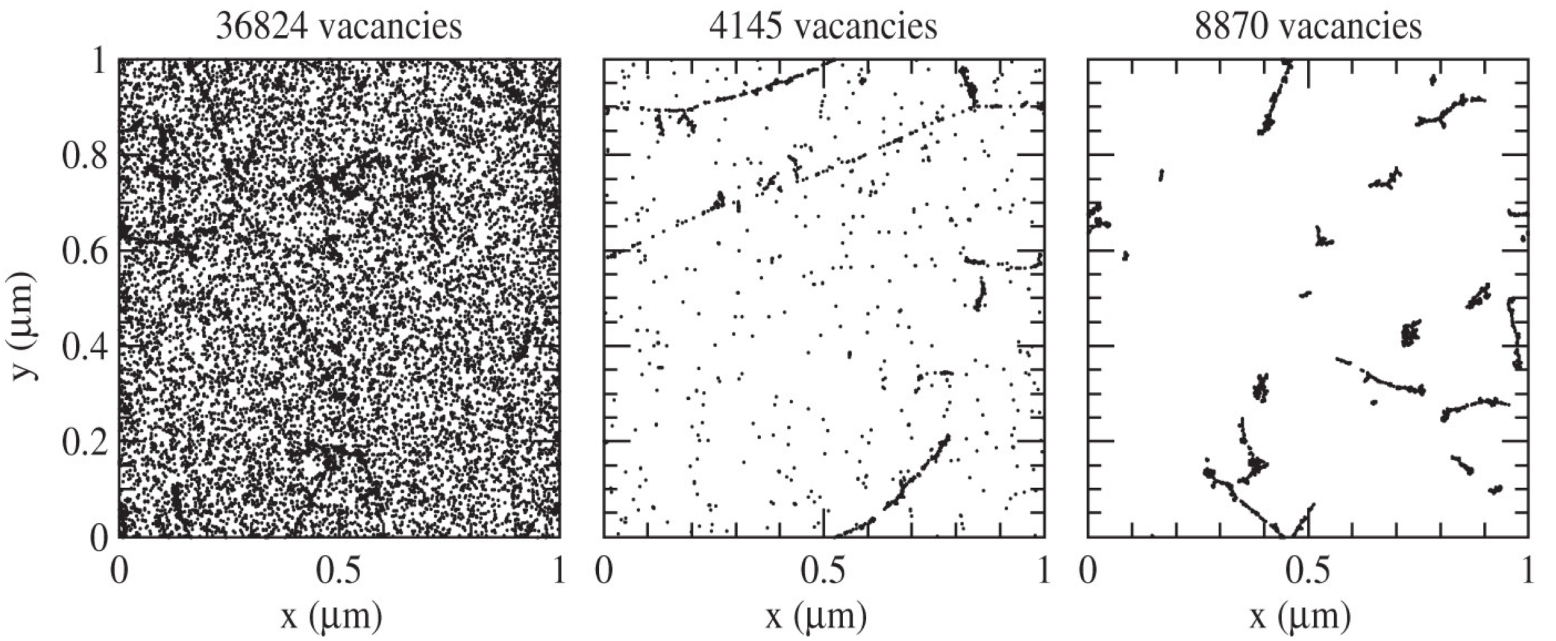
Radiation damage effects in silicon detectors [2].

**Radiation damage dedicated lectures for more in-deep understanding*

- The NIEL (Non Ionizing Energy Loss) model allows predicting macroscopic effects of radiation damage in silicon:
  - Assumes that bulk damage produced by ionizing radiation is proportional to the Non-ionizing energy lost by the particle through the sensor [6].



From [6]. Simulation of defects formation in silicon by different particles. Left: 10 MeV protons. Centre: 24 GeV protons. Right: 1 MeV neutrons.

Radiation damage effects in silicon detectors [2].

**Radiation damage dedicated lectures for more in-deep understanding*

- Radiation effects on the detector performance:
  - Leakage current. Defects can create free e-h pairs in the depleted area contributing to the leakage current. This effect is proportional to the radiation fluence and bias voltage:

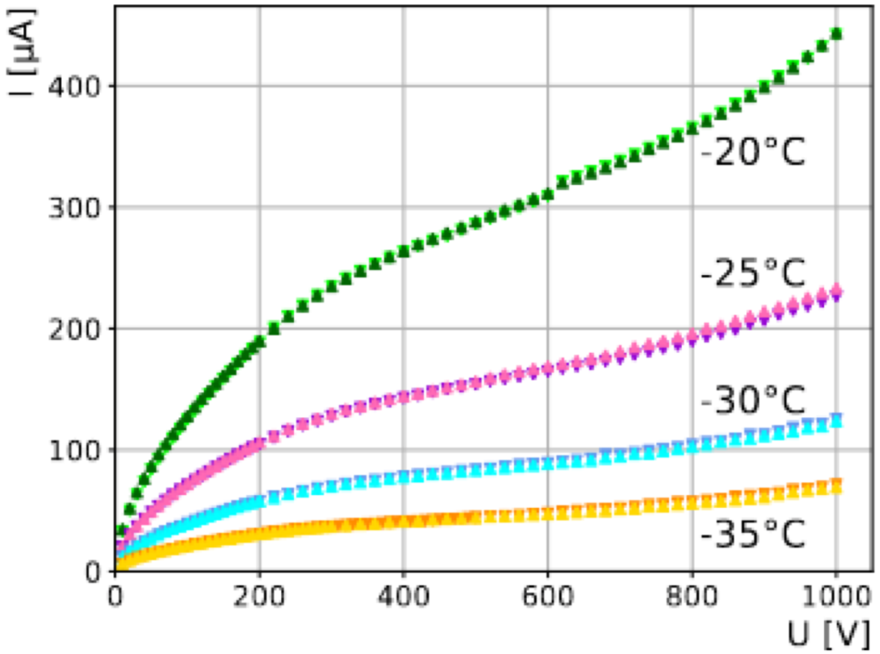
$$\Delta I_{leak}(\phi) = \alpha \cdot \phi \cdot V_{bias}$$

α = damage constant

    - Damage constant parametrisation in function of T and the annealing process can be found in M. Moll’s PhD thesis [7]

Annealing is a heat treatment that alters the material structure. It can be beneficial [7]

$\phi = 5 \times 10^{14}\ n_{eq}/cm^2$



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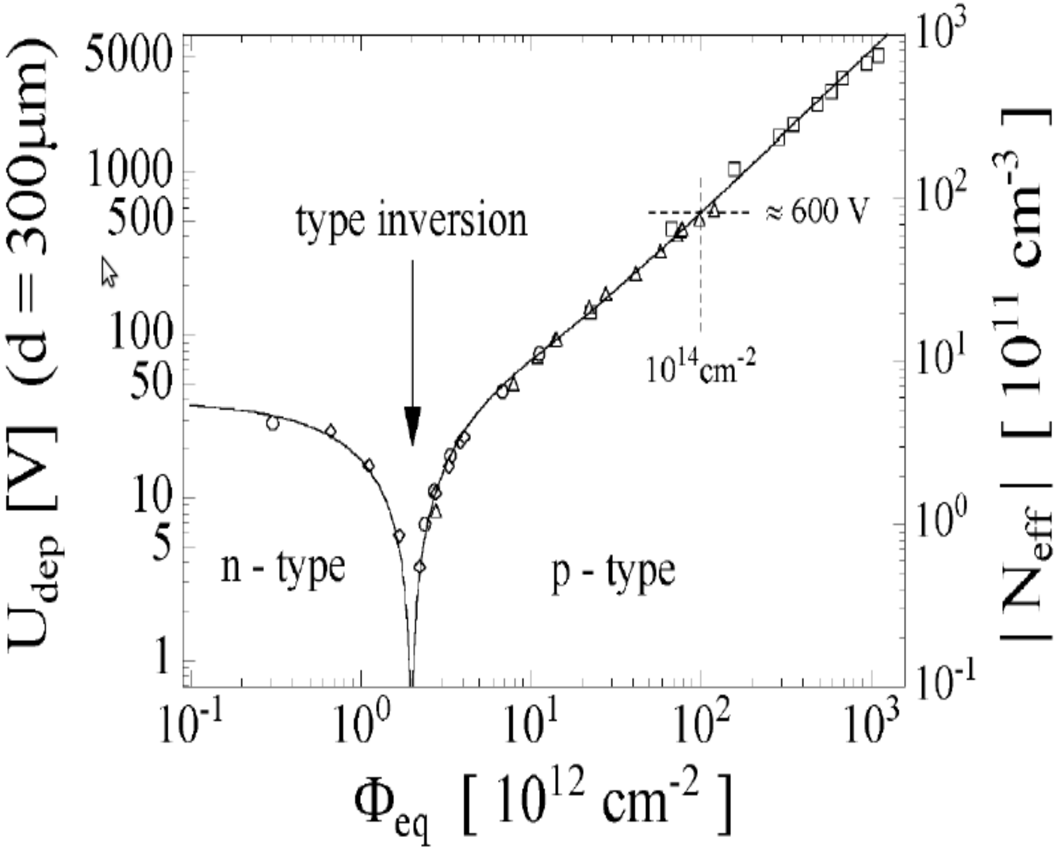
Radiation damage effects in silicon detectors [2].

**Radiation damage dedicated lectures for more in-deep understanding*

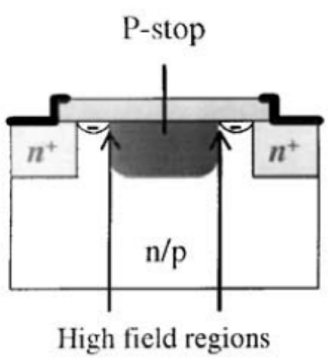
- Radiation effects on the detector performance:
  - **Depletion voltage.** $V_{fd} \propto |N_{eff}|$.
    - Radiation produces defects that can act as donors or acceptors and change the effective dopant concentration.
    - "donor or acceptor removal effect" [8], dopants are moved and deactivated
    - "type inversion" in n-bulk sensors. When the sensor is biased, deep defects will be activated close to the two implants, forming two separate junctions. The p-like defects will be activated close to the n+ region and viceversa [9].

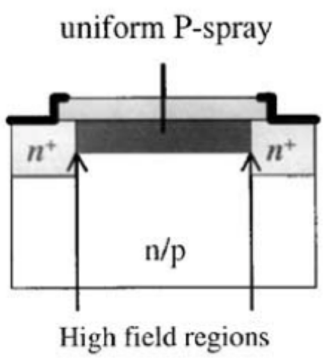


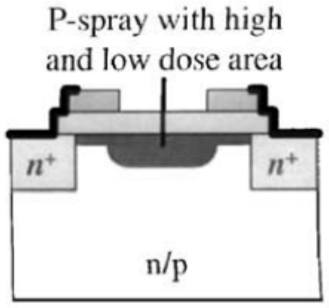
Radiation damage effects in silicon detectors [2].

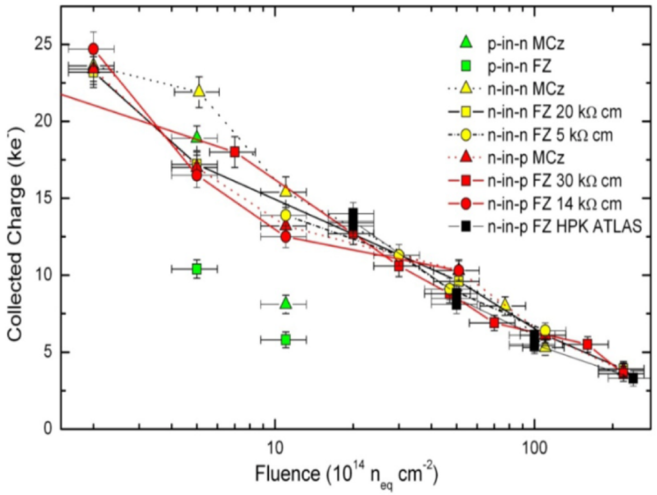
**Radiation damage dedicated lectures for more in-deep understanding*

- **Trapping.** Crystalline defects introducing energy levels with high capture cross section with re-emission time ∼ ms. Trapped charge is lost. **Charge collection reduced**. Signal degradation.
- **Avalanche charge multiplication**. Sensors showing a **very high charge collection** after high irradiation fluences. High value of $|N_{eff}|$ can create localised high $\boldsymbol{E}$.
- **Surface damage**. Defects on the passivation SiO_2 layers produce:
  - Oxide ionization: electrons escape and a positive charge on the layer, compensated by a negative charge in the bulk.
  - Creating **shorts between segmented electrodes**.
  - Two main techniques to compensate for that to adapt depending on the device and application [10]:
    - P-spray: adding a p-type layer between sensor bulk and passivation layers
    - P-stop: p-type silicon “barrier” surrounding the electrodes



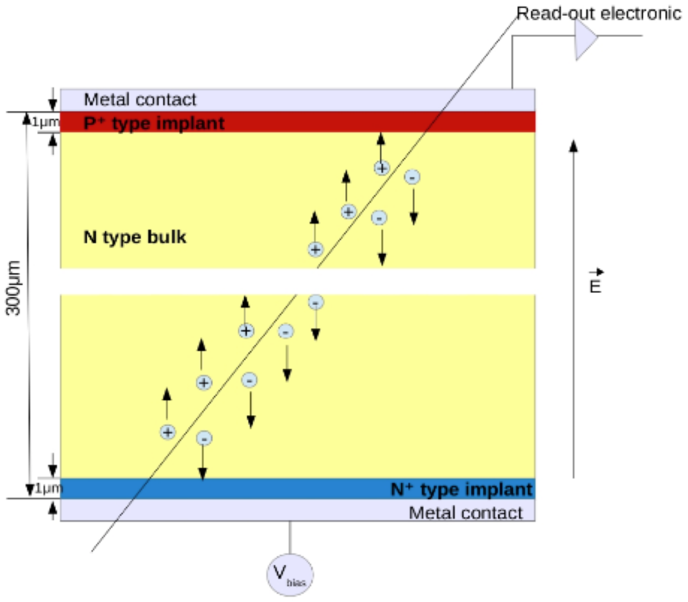


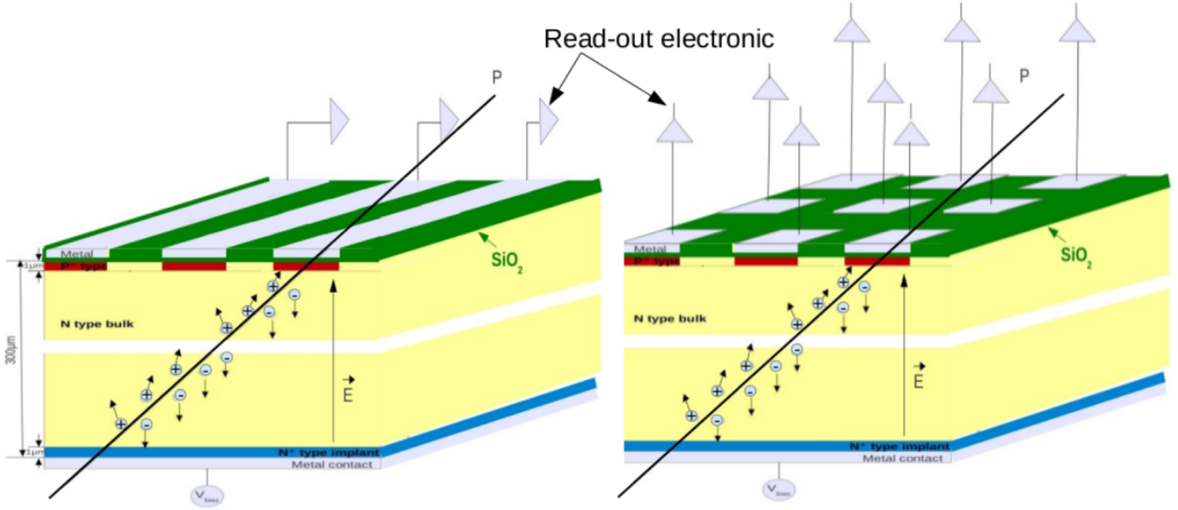




Position resolution[3]

- Position resolution is given by the size of the electrode (to first order):
  - Electrode size is also limited by:
    - Wafer size
    - Electronics bonding (interconnection technique)
  - Electrodes are segmented into strips or pixels (‘strixels’ also exist)
    - Sensors remains 100% efficient despite the gaps (field lines remain parallel until near the surface) provided:
      - $V_{bias} > V_{FD}$
      - Un-irradiated sensors
  - Segmentation in the junction side or the ohmic side
  - We talk about p-on-n, n-on-n, n-on-p sensors:
      - P-on-n: collect holes
      - N-on-n or n-on-p: collect electrons (higher mobility). P-type bulk avoid type inversion





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Position resolution[3]

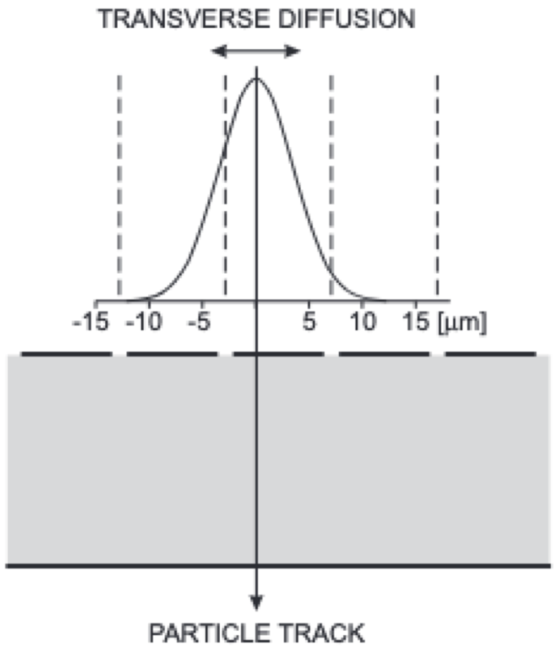
- Position resolution:
  - Diode → Pitch 'p'
  - Strip or pixel detector. Tracks randomly aligned with the strip, the difference between the measured and the real position have a gaussian distribution with the standard deviation:

$$\sigma^2 = \int_{-p/2}^{p/2} \frac{x^2}{p} dx = \frac{p^2}{12} \, ,$$

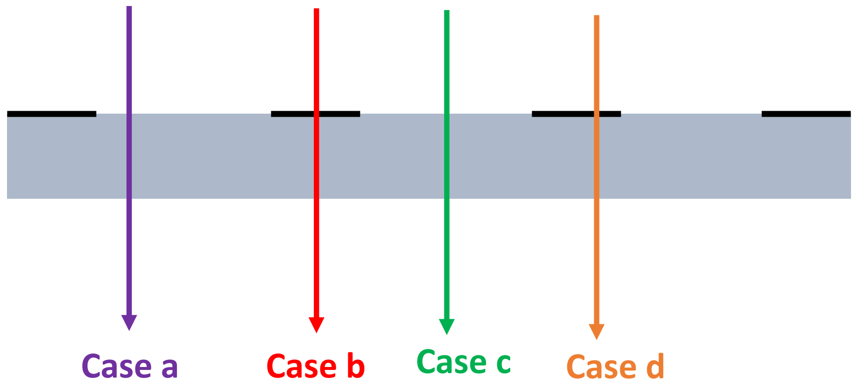
  - Transverse diffusion, thermal spread of the charges with an RMS width σ^2 = 2Dt:
    - D is the diffusion constant, proportional to the carriers mobility (=kTμ/e)
    - Using the average field approximation: $\boldsymbol{E}$ = V/d
    - t is the collection time, inversely proportional to the mobility t ~d/v =d/($\mu\boldsymbol{E}$) = d^2/(μV)
    - The transverse diffusion is independent of the carrier

$$\sigma_y = \sqrt{2Dt} \approx \sqrt{2\frac{kT}{e}\frac{d^2}{V_b}}$$

  - Charge sharing between electrodes also helps with resolution



Q2: what do you think is the effect of the transverse diffusion in the position resolution? Beneficial or detrimental?



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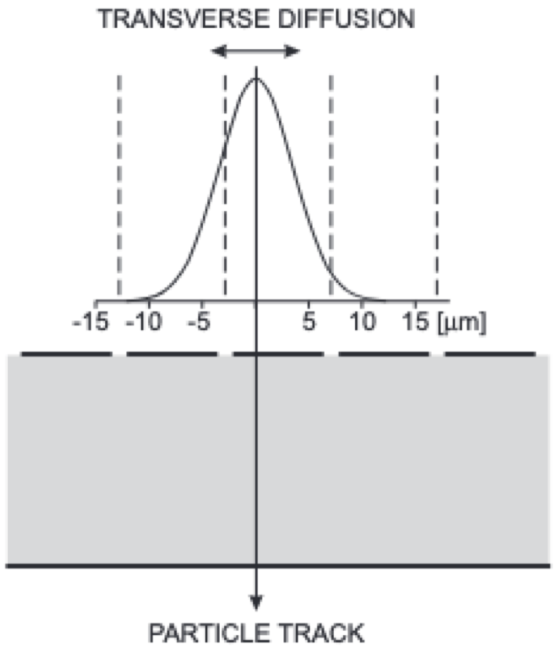
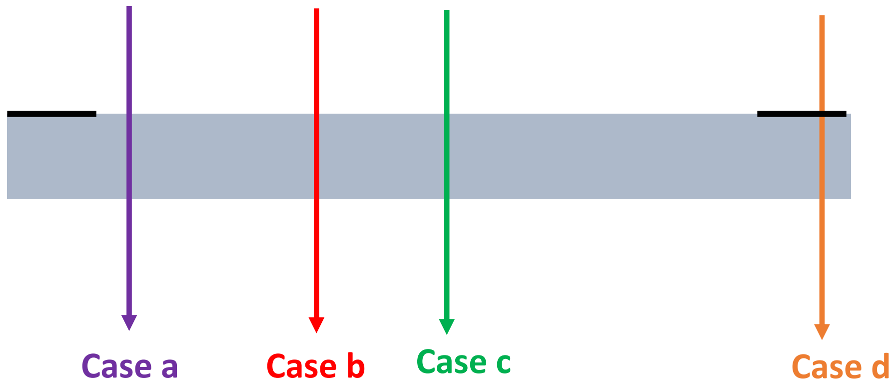


Q2: what do you think is the effect of the transverse diffusion in the position resolution? And on which circumstances is beneficial?



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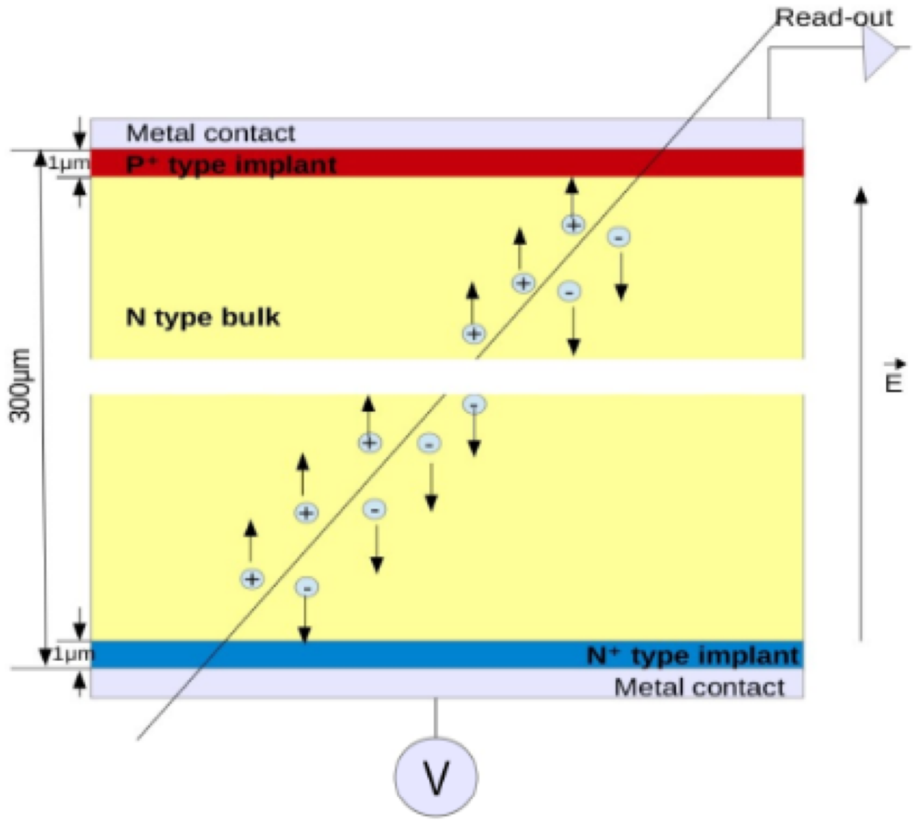
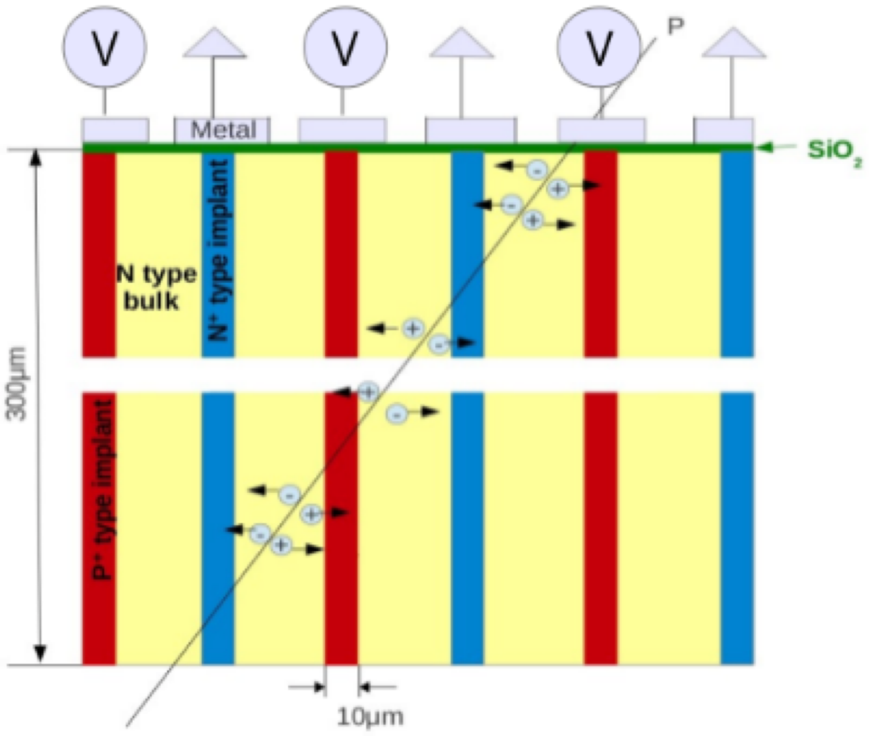
Devices structures [2]

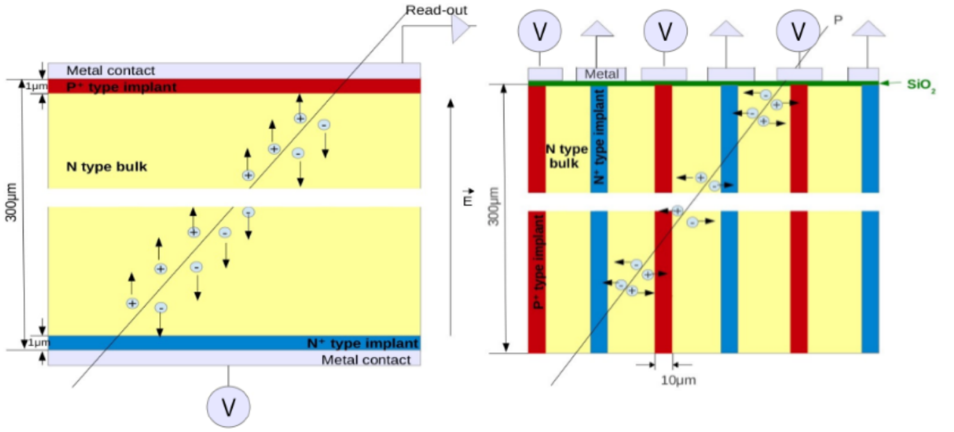
Q3: Any guesses on advantages and disadvantages from 3D sensors with respect to planar ones?

- Electrode position: Planar vs 3D (surface or embedded)
  - 3D sensors where proposed by S. Parker in 1997 [4]
  - They can be strip or pixel sensors





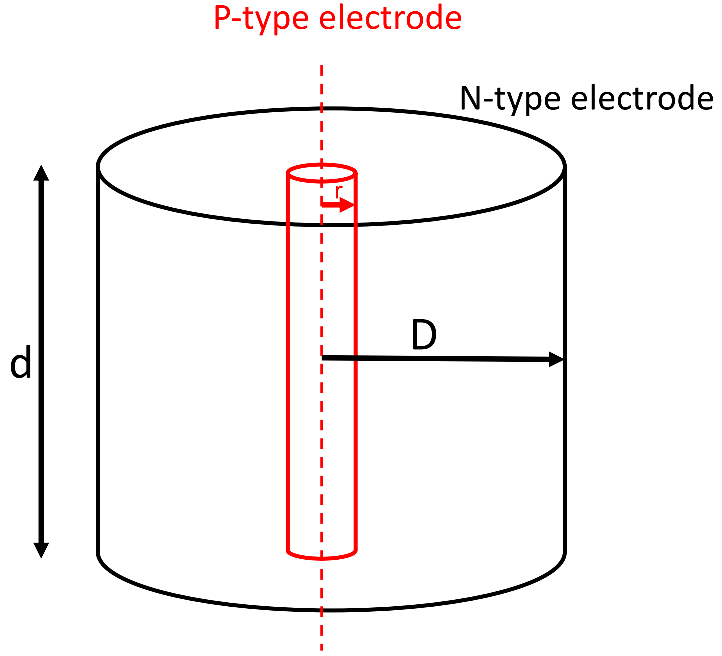
3D structures characteristics[2]



- In 3D devices, distance between electrodes no more limited by the sensor thickness.
- Full depletion voltage now is given by the coaxial approximation [11]:

$$V_{FD} = \frac{qN_{eff}}{2\epsilon_0\epsilon_{Si}}\left(D^2\left[ln(\frac{D}{r} - 0.5)\right] + 0.5r^2\right)$$

D = Electrode distance
r = column radii



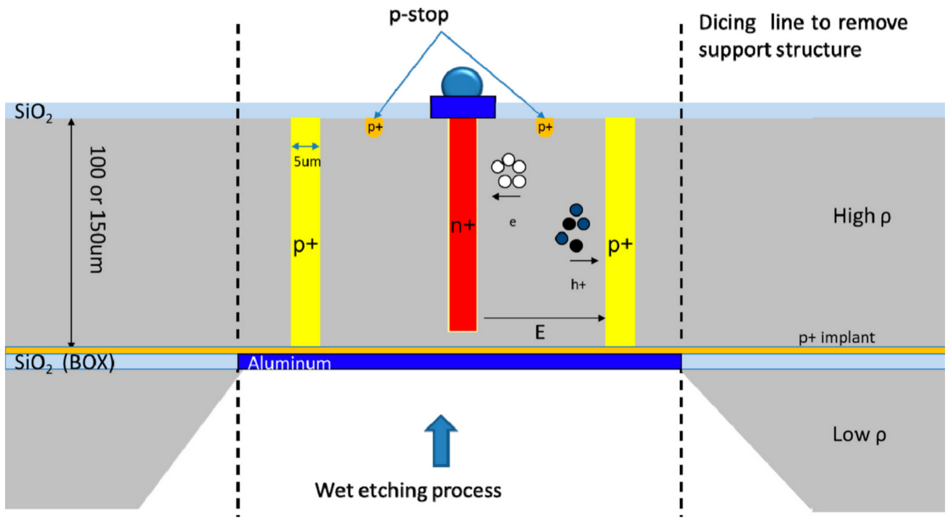
- Smaller V_{FD}
- Shorter distances to travel for carriers
- Input capacitance is higher then in planar → challenging for ROC

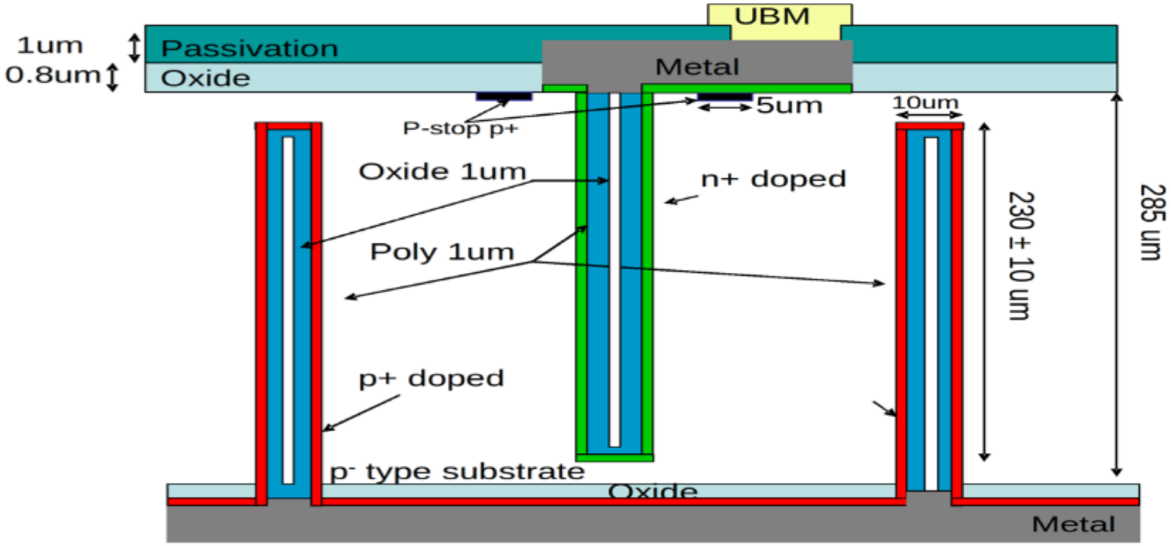
$$C = \frac{2\pi\varepsilon_0 d}{ln\left(\frac{D}{r}\right)}$$

- short collection distances, fast collection times and low depletion voltages

3D sensors fabrication [2]

- Single sided [5] or double sided [2] processing:
  - Double sided require less fabrication steps
  - Single sided allow to fabricate thinner sensors that require a support wafer



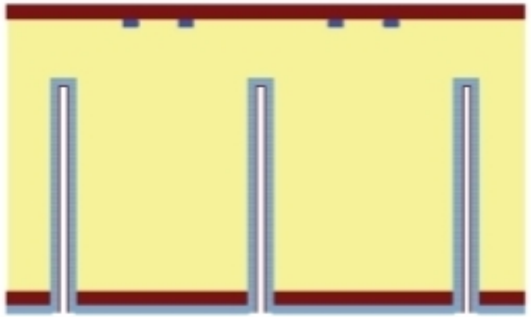


3D sensors fabrication [2]

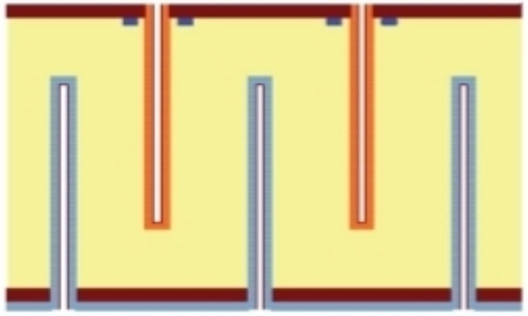
- Schematic of the fabrication process of double-sided 3D silicon detectors. The first step is the p-stop implantation, then the polysilicon deposition plus the Boron diffusion create the ohmic contacts and an oxide barrier is grown. The same process is followed to create the junction columns but diffusing Phosphorus instead of Boron. The last step is to metalize and passivate both sensor sides.
- Deep Reactive Ion Etching (DRIE)
- In single sided 3Ds you have to dope the two different types from the same side, adding some steps in the fabrication

High resistivity p-type silicon

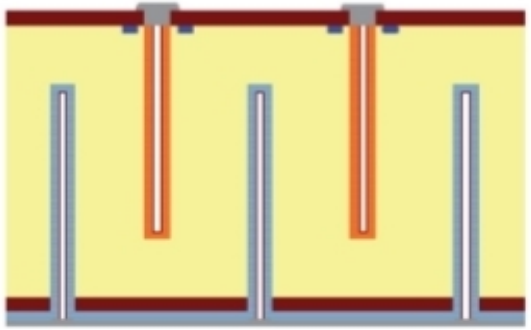
Boron implantation (p-stop insulation)



DRIE for p^+ holes
Polysilicon deposition + doping B
Sidewall diffusion + grown oxide



DRIE for n^+ holes
Polysilicon deposition + doping P
Sidewall diffusion + TEOS deposition



Metallization + passivation

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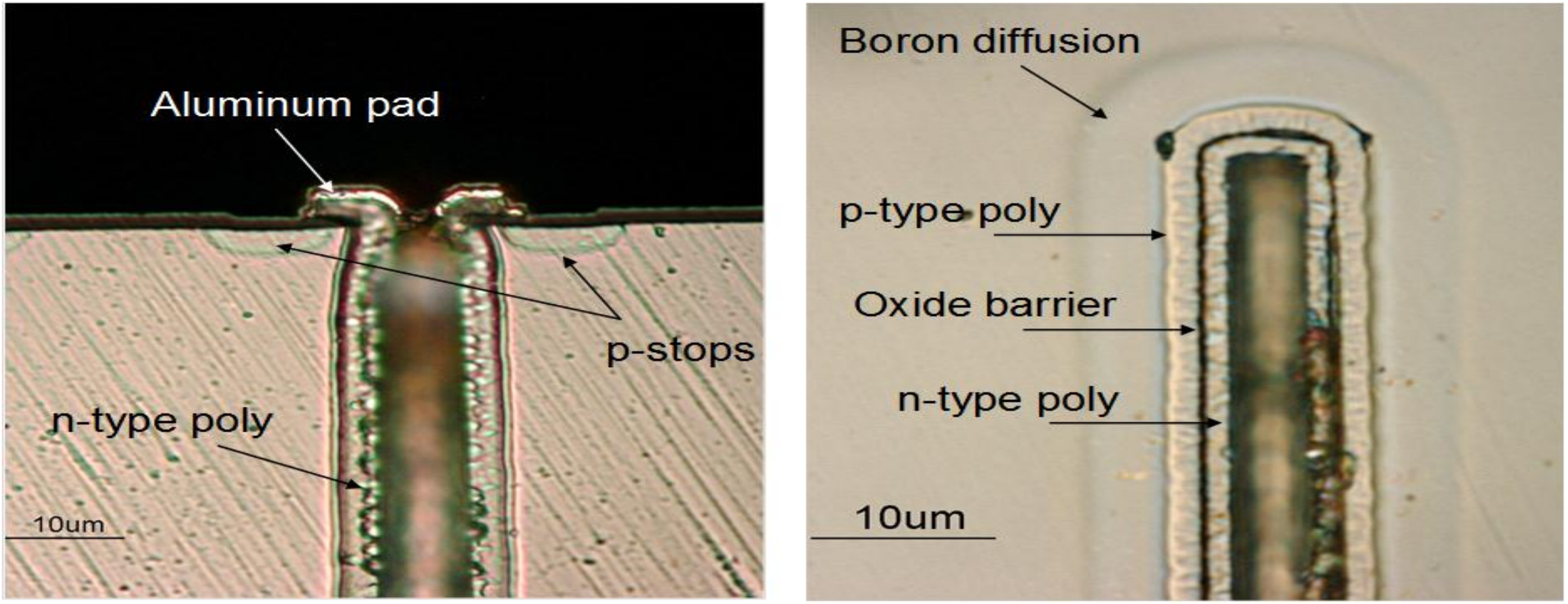
3D sensors fabrication [2]



- Microscope pictures of 3D pixel sensors. Left: n-column in p-type silicon bulk, the p-stop implantation and polysilicon layer for diffusion are visible. Right: p- columns (ohmic junction) where the Boron diffusion and the two polysilicon layers separated by an oxide barrier can be appreciated.

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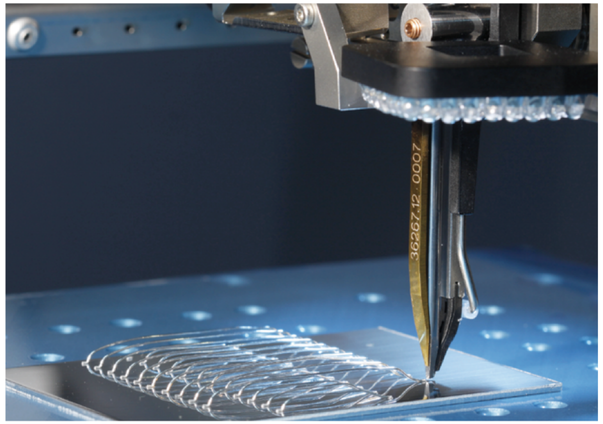
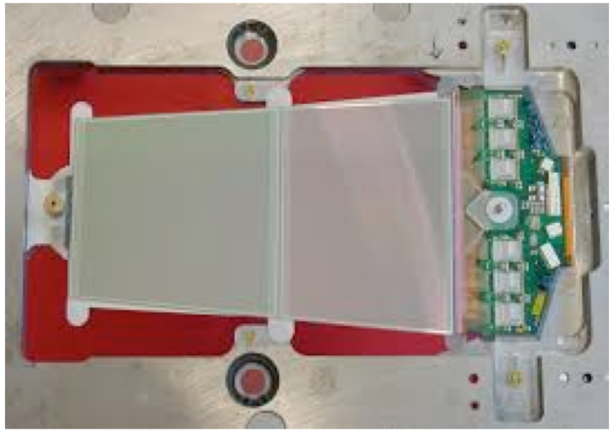
Hybrid detectors[2]

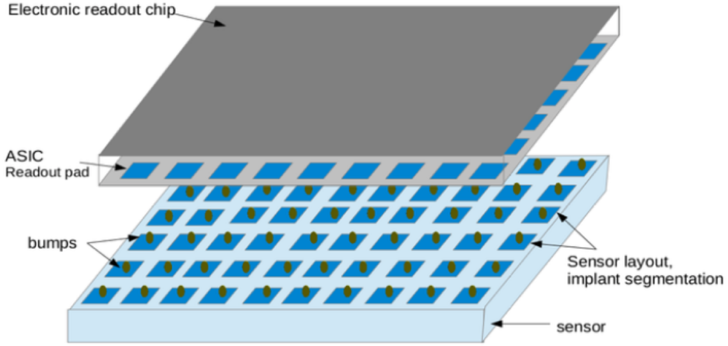
- Hybrid detector: sensor and Read-Out chip (ROC) are developed separately, an interconnection process is required:
  - Microstrips detectors → Ultrasonic wire bonding
    - Microstrip pitch must adapt to the electronics or a pitch adapter is required

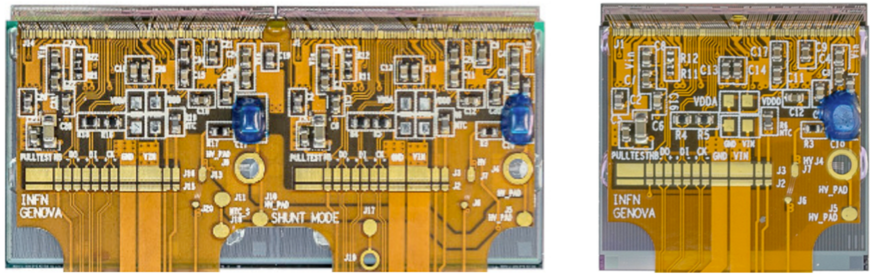




ATLAS-SCT strip module

  - Pixel detectors →bump bonding (electrochemical process) +wire bonding

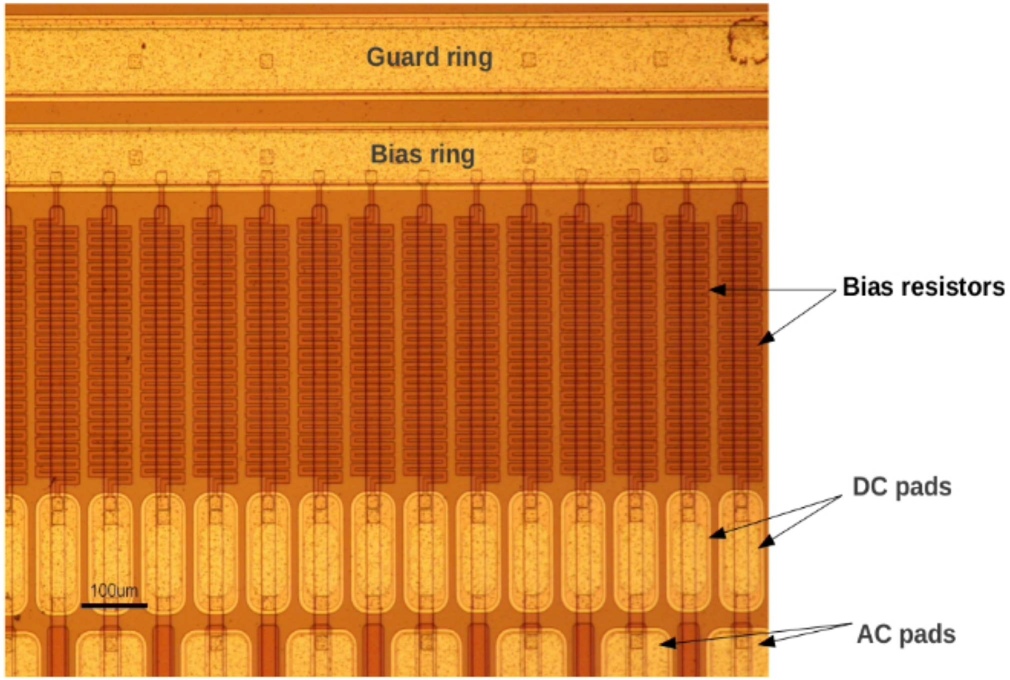


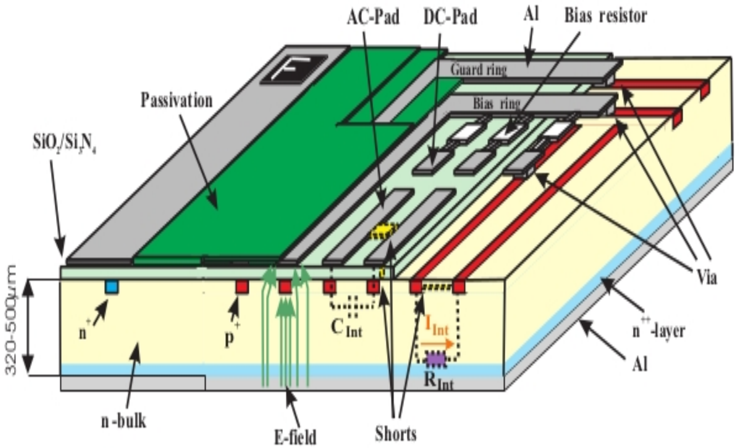


(a) (b)

ATLAS-IBL pixel modules

Sensors interconnections [2]





- Sensor to ROC interconnection. Each strip or pixel of a silicon sensor must be connected to its own readout channel. This can be done in two different ways:
  - DC coupling: direct connection from the strip or pixel to the electronics. The amplifier should sink part of the leakage current (common approach in pixels)
  - AC coupling: bypass the DC leakage current over a resistor and pick up only the AC part over a capacitor (common on strips where the leakage current can be significant)
    - In silicon strip detectors, resistors and coupling capacitors are usually integrated into the sensor. The bias resistor is commonly implemented as a polysilicon structure, which is less vulnerable to radiation damage.

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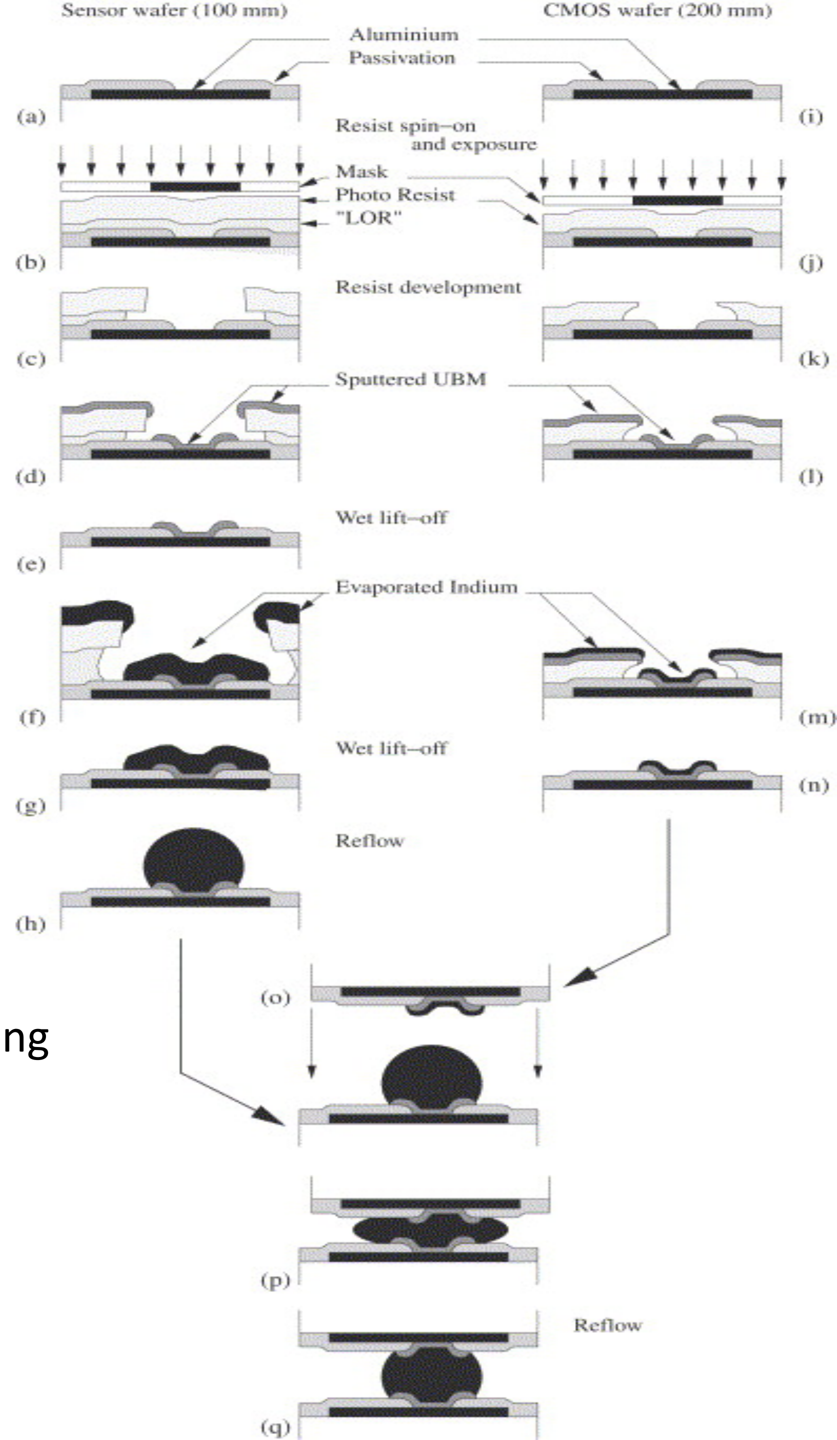
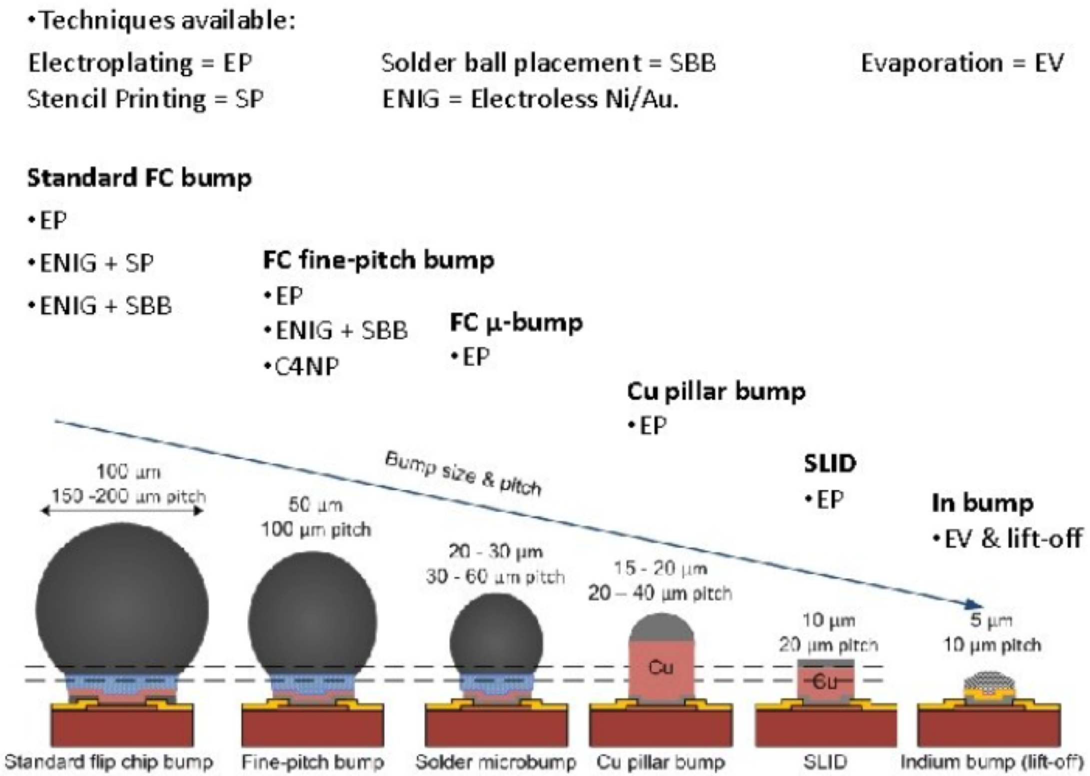
Bump bonding technique

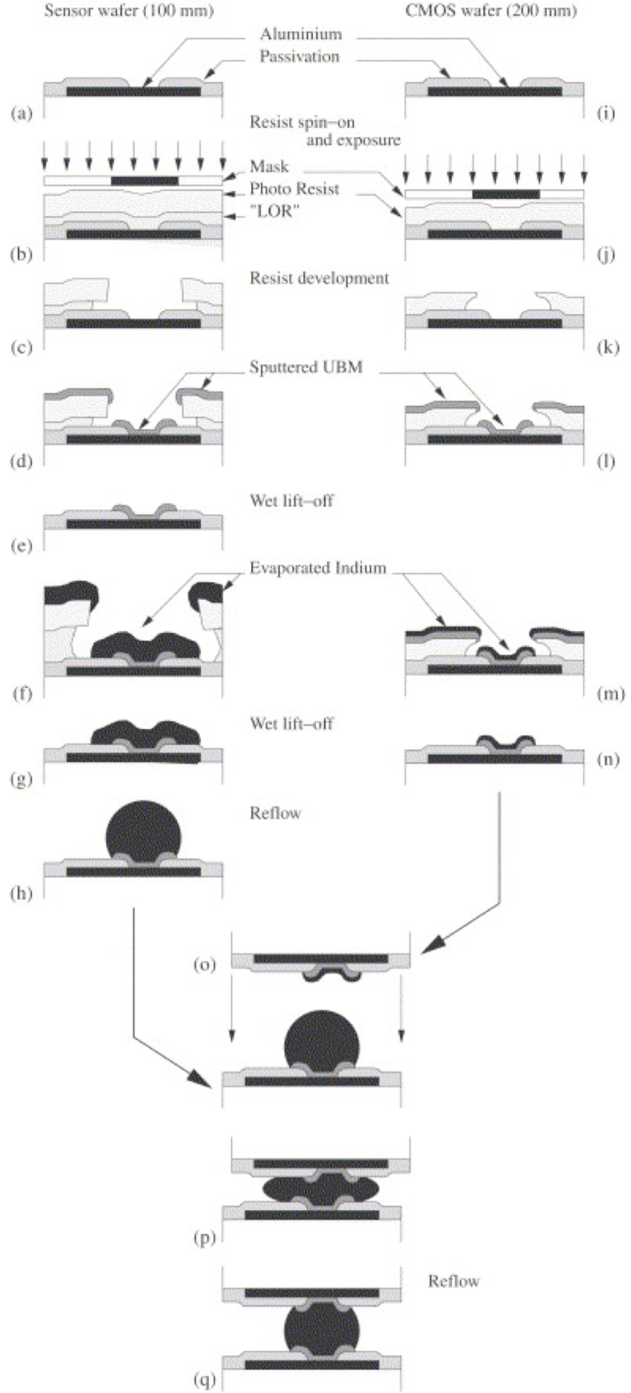
Right figure from [13]: Diagram of indium bump-bonding technique. From (a)-(g) is the under-bump metallization in case of the sensor and from (i) to (n) in case of the ASIC chip (all these steps are made on wafer). Step (h) is the first “reflow” after dicing. Steps (o) and (p) are the flip-chip process and the final step (q) is the second and final “reflow” after which the contact is finally stable and robust.

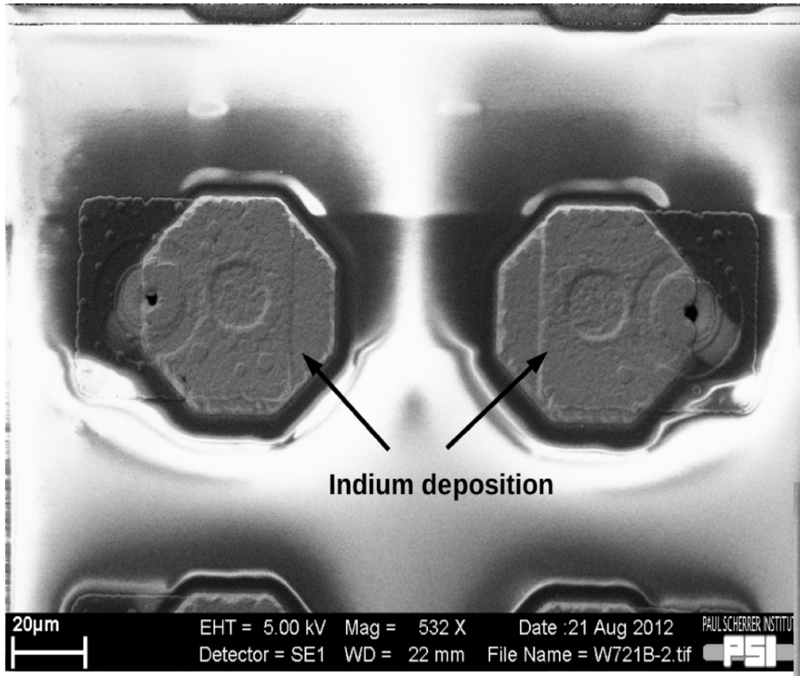


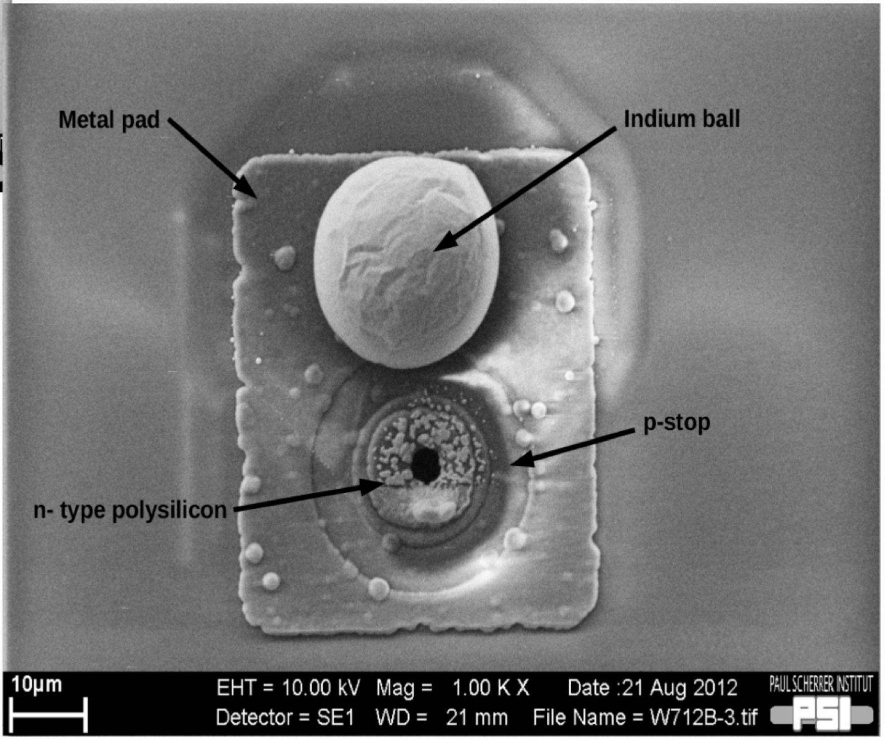


Left figure from [14]. Different bump-bonding Techniques.

Bump bonding technique [2]





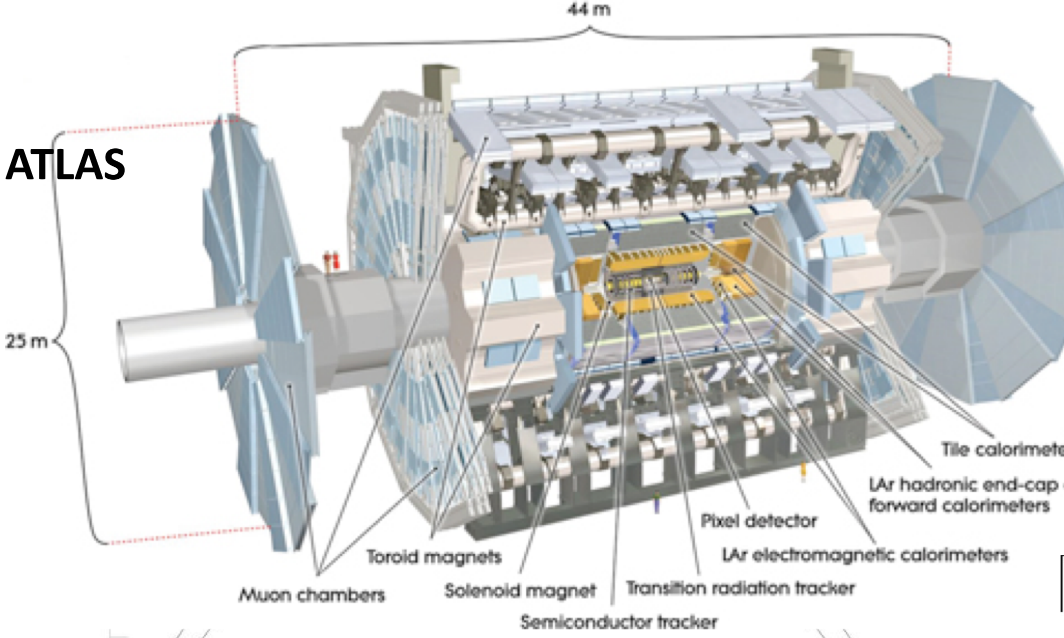


Scanning electron microscope pictures of indium bumps (Top) before and after (Right) reflow in 3D pixel sensors. The bumps pitch is of 100 µm and the reflowed bumps diameter is of 20 µm.

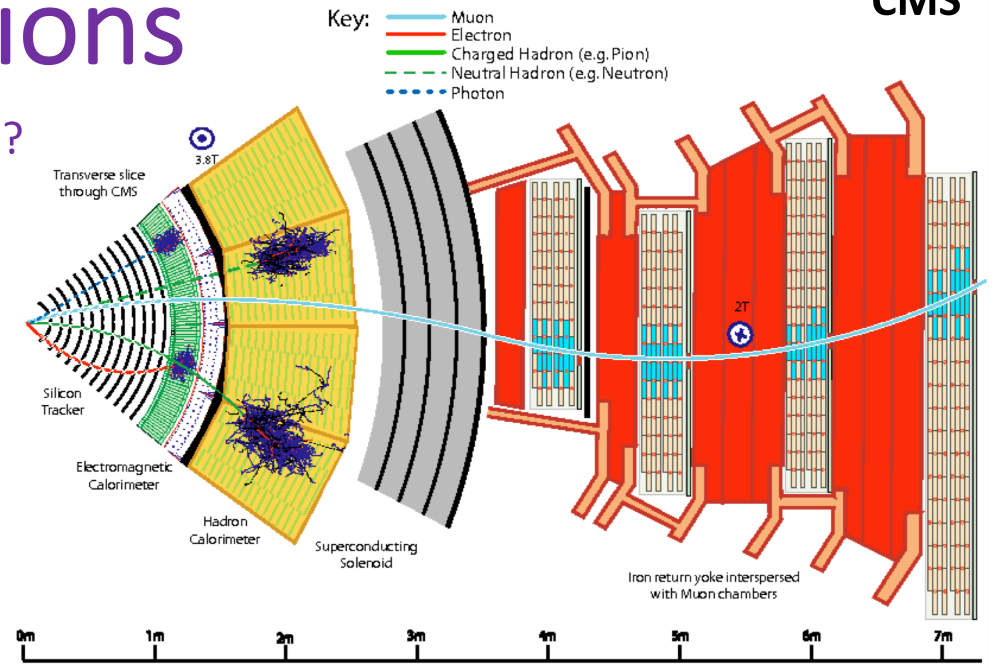
Collider experiments applications

Q4. Where do we use strips and where do we use pixels, and why? 3Ds?

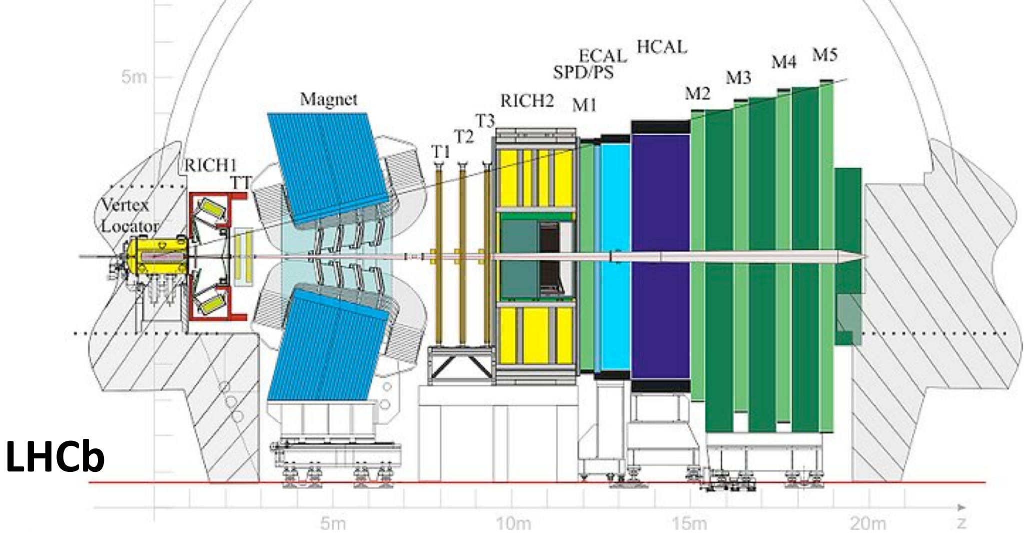
ATLAS



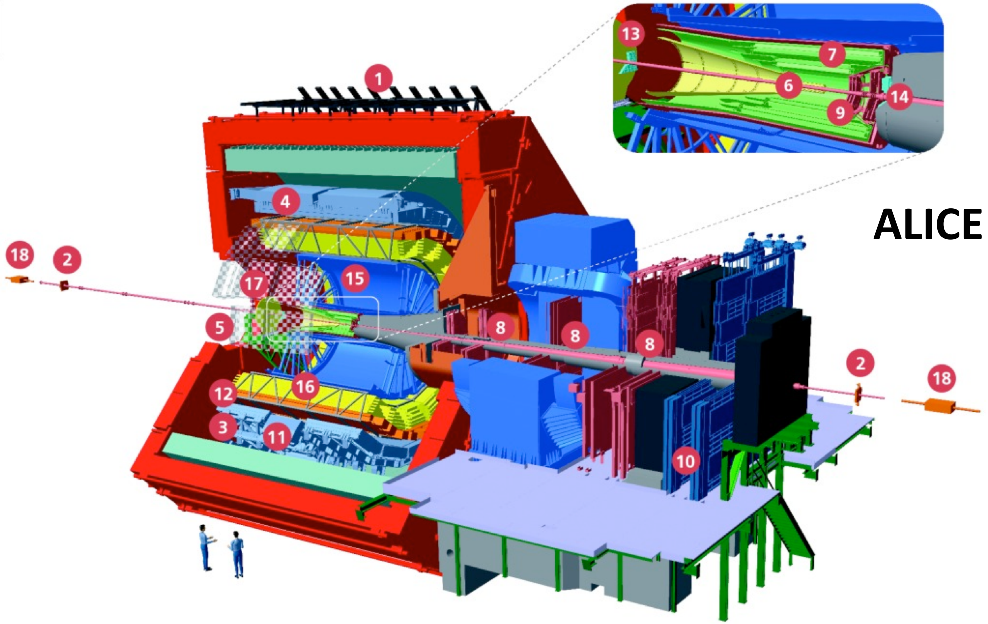
CMS



LHCb



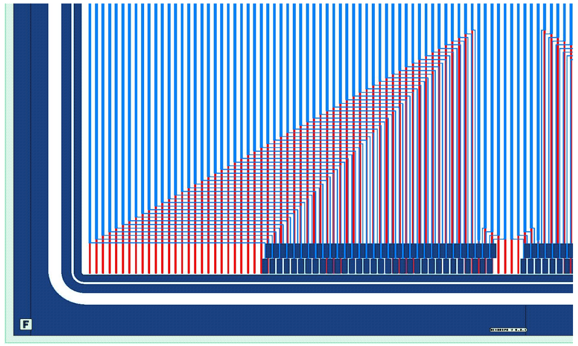
ALICE

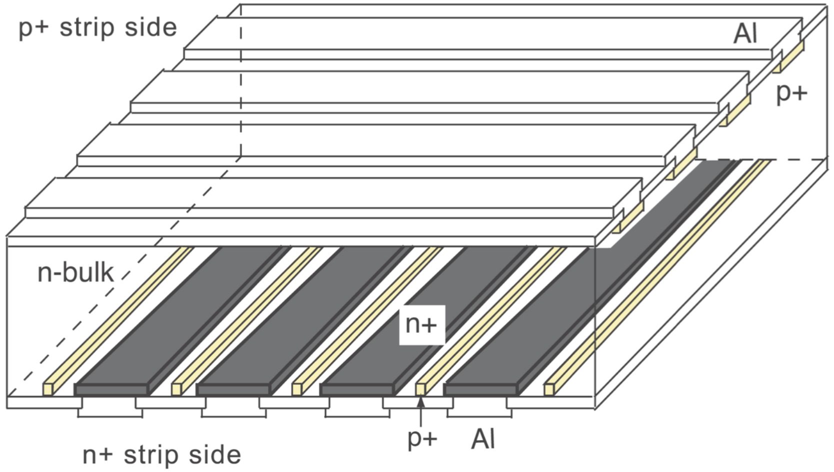


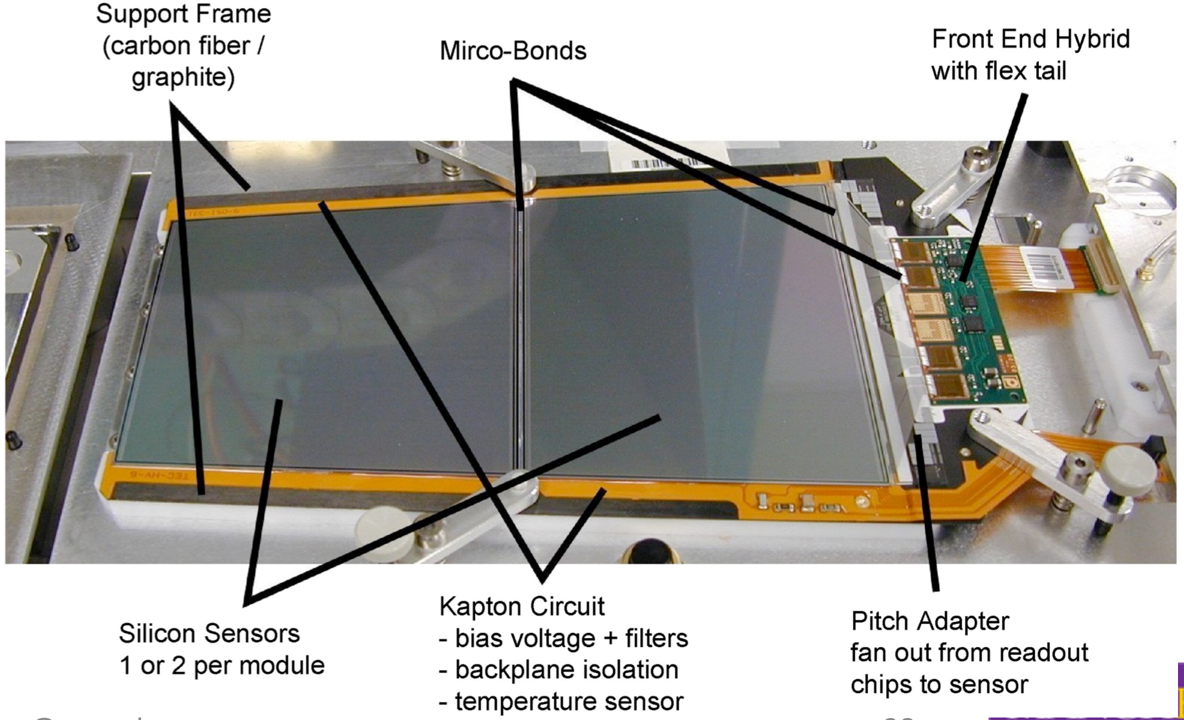
① **ACORDE** | ALICE Cosmic Rays Detector
② **AD** | ALICE Diffractive Detector
③ **DCal** | Di-jet Calorimeter
④ **EMCal** | Electromagnetic Calorimeter
⑤ **HMPID** | High Momentum Particle Identification Detector
⑥ **ITS-IB** | Inner Tracking System - Inner Barrel
⑦ **ITS-OB** | Inner Tracking System - Outer Barrel
⑧ **MCH** | Muon Tracking Chambers
⑨ **MFT** | Muon Forward Tracker
⑩ **MID** | Muon Identifier
⑪ **PHOS / CPV** | Photon Spectrometer
⑫ **TOF** | Time Of Flight
⑬ **T0+A** | Tzero + A
⑭ **T0+C** | Tzero + C
⑮ **TPC** | Time Projection Chamber
⑯ **TRD** | Transition Radiation Detector
⑰ **V0+** | Vzero + Detector
⑱ **ZDC** | Zero Degree Calorimeter

Micro –Strip detectors developments.

- Strip-detectors are used on the outermost layers of the trackers because they can cover bigger areas and less position resolution is required.
- There are also mitigation strategies to improve position resolution on strip detectors:
    - Geometry optimisation
    - Stereo angles
    - Integrated pitch adapter
    - Double sided



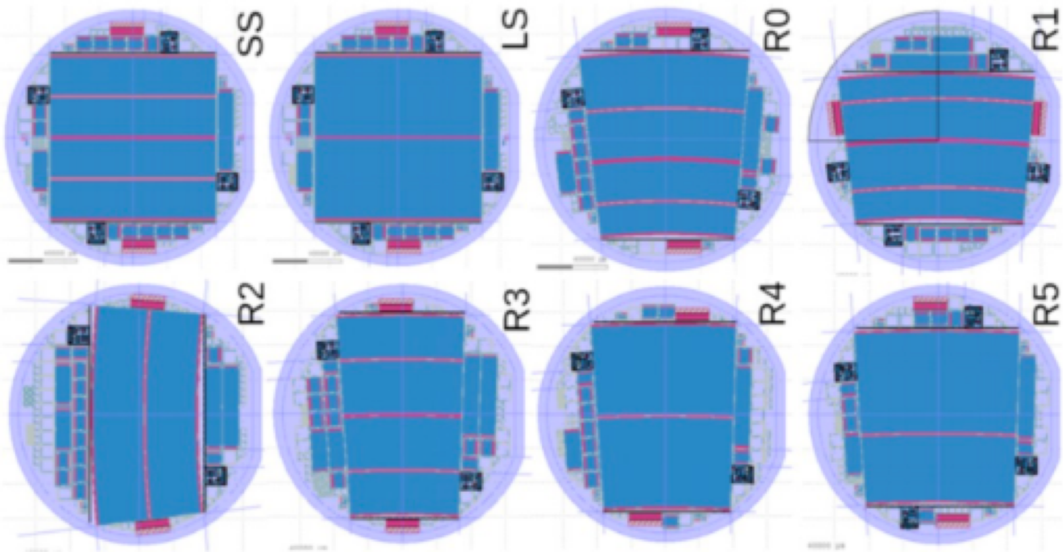


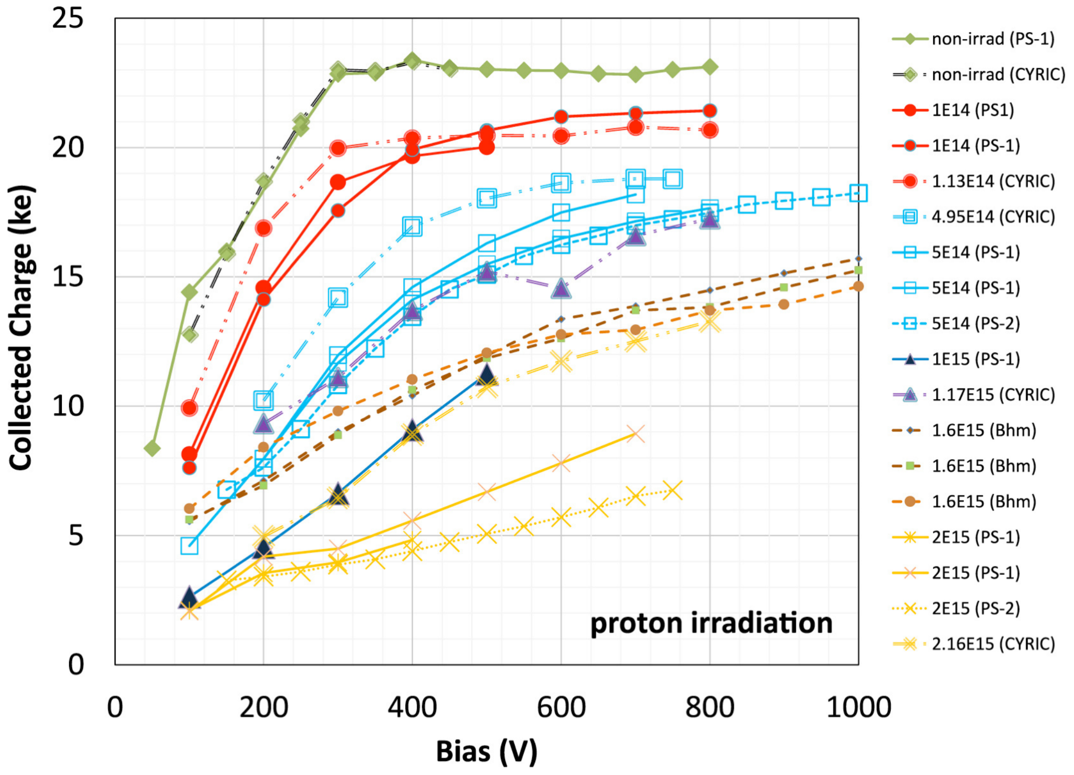


Micro –Strip detectors. One example of today in ITk [15].

- 8 sensors geometries:
  - 2 for the barrel, 6 for endcaps
  - 320 um thick n-in-p silicon
  - 70 -80 pitches
  - 1 sensor/silicon wafer
  - V_{bias} (100-500v)

SS, LS are barrel, R# are end-cap





Max. expected +SF = 1.6×10^{15} n_{eq}/cm^2

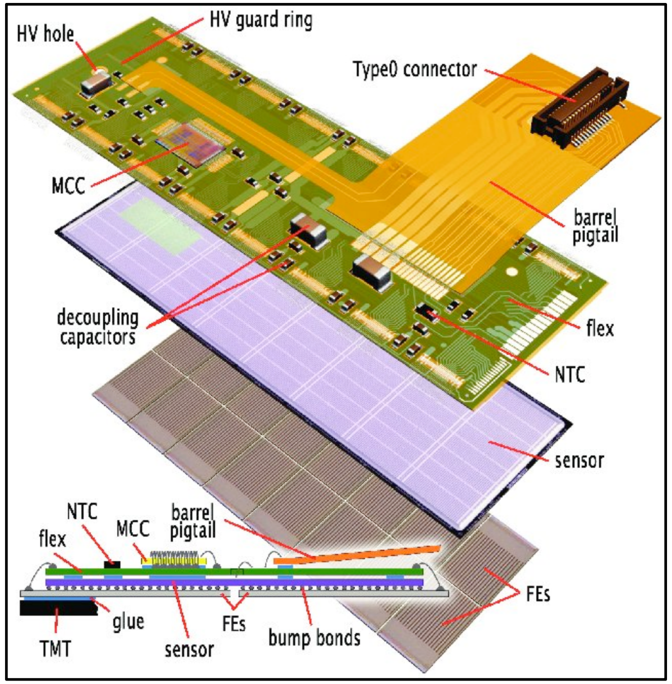
Q5. Why not thinner?

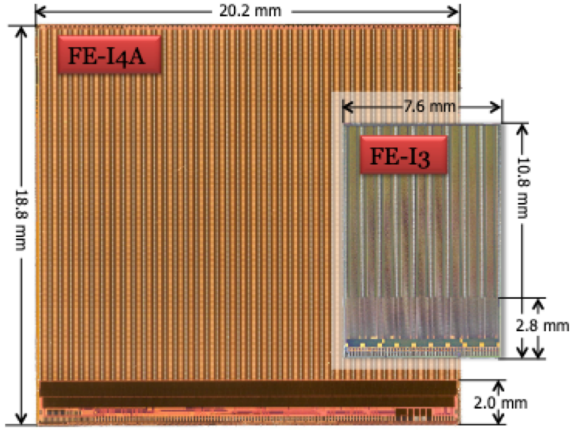
(When go down to 150 um in pixel)

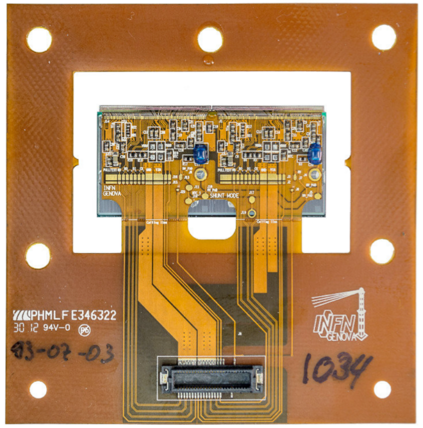
Pixel detectors developments.

- Pixel detectors are in the innermost layers:
  - Smaller areas to cover up and higher resolution requested
  - Pixel detectors are more expensive
- The developments have been on:
  - Thinning sensors
  - Smaller pixel size
  - Interconnection yield (bump bonding)
  - Getting closer to the beam pipe
  - Bigger area ROC (and thinner)
  - Radiation Hardness

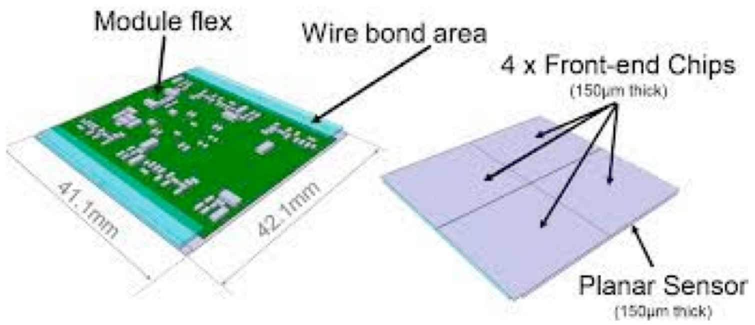
ATLAS ID – pixel module (50 x 400 um^2)







ATLAS IBL – pixel dual- module
(50 x 250 um^2)



ATLAS IBL – QUAD module (50 x 50 um^2)
Triplet (25 x 100 um^2)

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Radiation Hardness in the innermost layers of the pixel detector.

- At HL-LCH innermost layers we need technologies capable to cope with high irradiation doses (up to 2×10^{16} n_{eq}/cm^2). Thin devices of both, planar and 3D technologies.
  - The innermost layer of both CMS and ATLAS will be made on 3D pixel technology

Q6. Why 3D? Why only in the innermost layer? and what are the challenges?

  - Planar technologies elsewhere. To decrease the V_{FD} and trapping they have to be very thin
- Trackers in collider experiments are operated at very low temperatures! ~ -30C

Q7. Why? What do we avoid?

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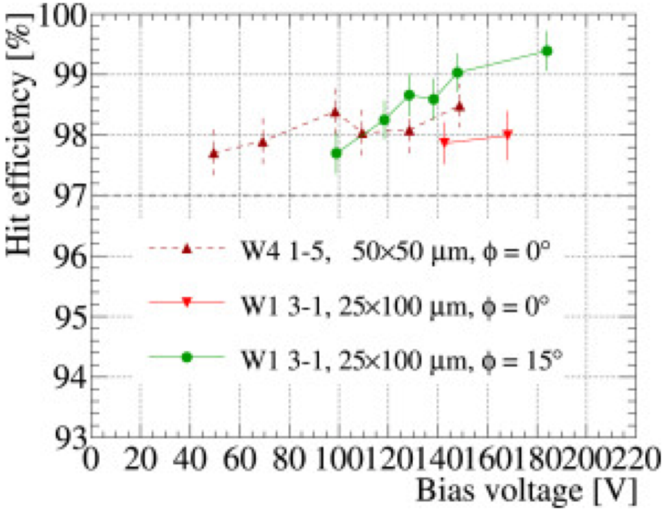
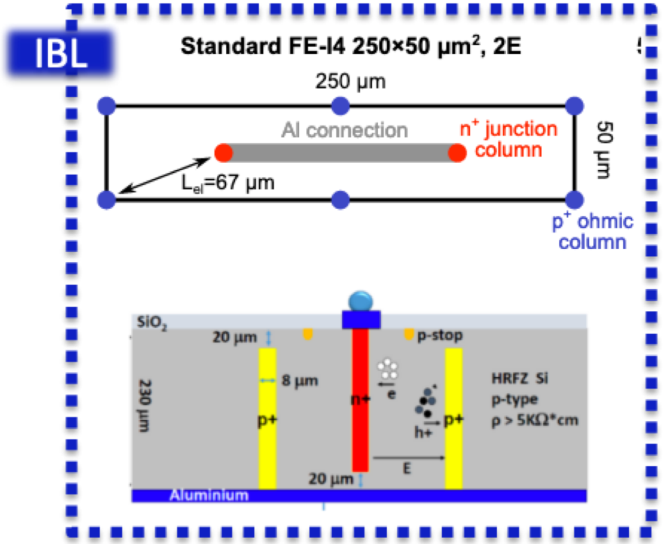
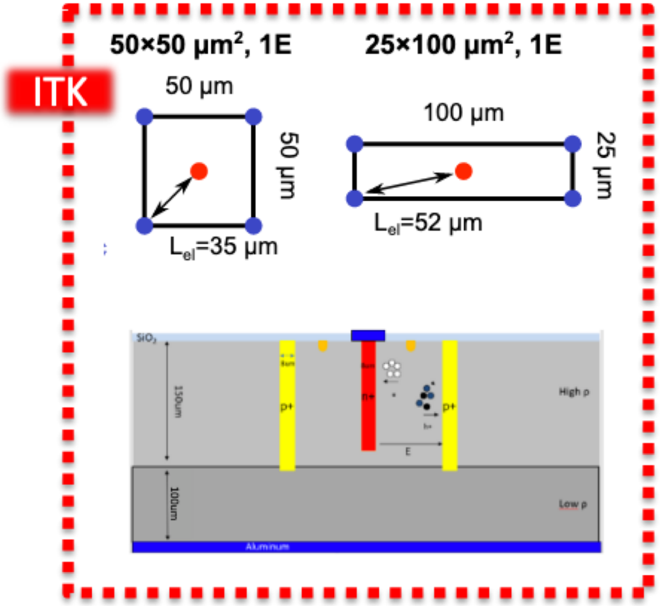
Pixel detectors. One example of today in ITk [15].

- 5 layers of silicon pixel system
  - Quad modules with Thin n-in-p planar silicon sensors (50 x 50 μm^2) in L1 to 4.
    - 100 μm thick in L1 → 400V
    - 150 μm thick in the rest →600V
  - Triplet modules with 3D silicon sensors in L0 (34 mm from the beam pipe).
    - 150 μm thick (effective)
    - 50 x 50 μm^2 pixel size→ 70V
    - 25 x100 μm^2 pixel size→ 100V
    - Single sided processing
    - Production yield







Future challenges for hybrid detectors

- Higher radiation resistance → better performance
  - Both ROCs and sensors
- Smaller pitch → higher resolution
  - Interconnection technique pitch, cost and yield with thin ROCs and sensors
  - Data handling (optic data transmission in high radiation environments)
- Timing information
  - Faster charge collection :
    - 3D trench sensors
    - LGADs

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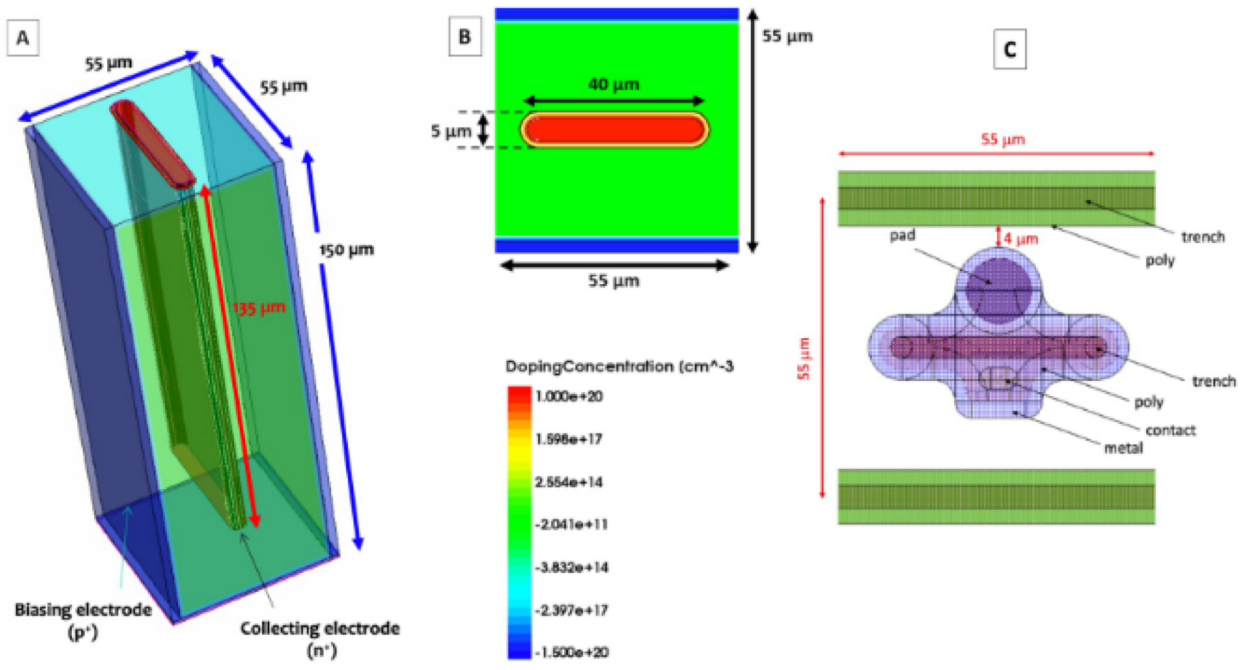
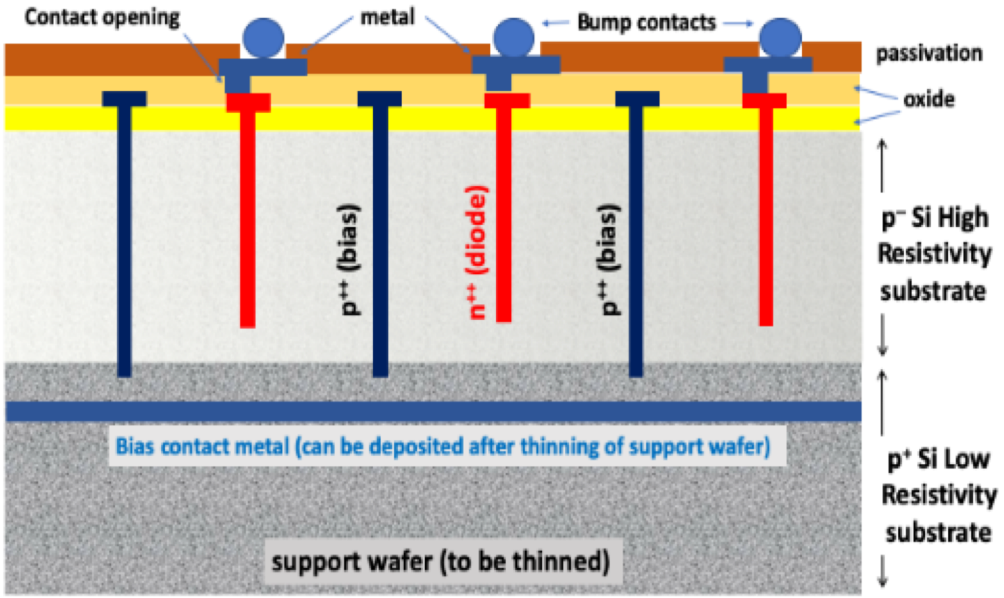
3D trench sensors [16]

- Timing detectors with high time resolution will become the next generation of detectors for future colliders with very high instantaneous luminosity



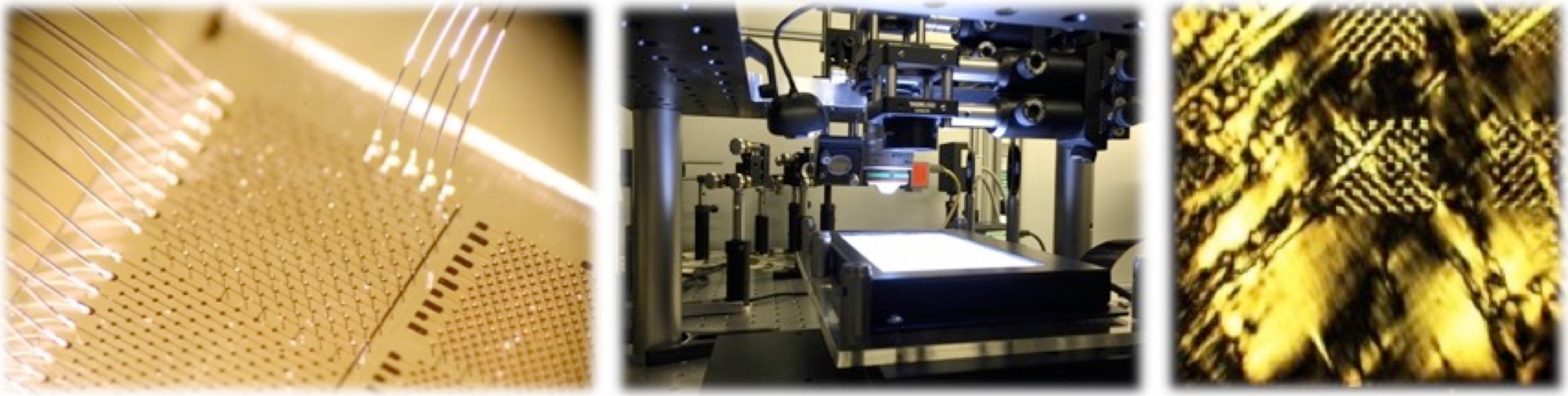


First results show time resolution between 20 and 40 ps

Other semiconductor detectors

** More on Alexander Oh lecture*

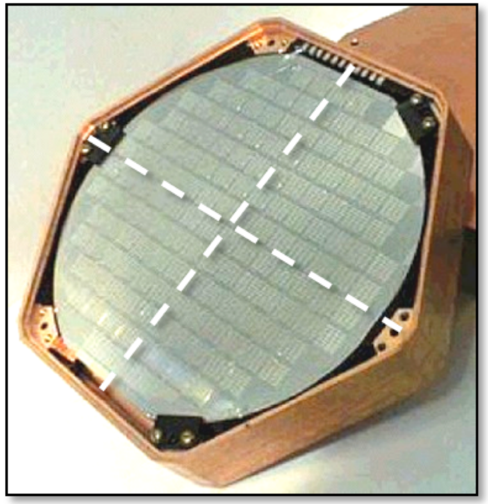
- Diamond detectors: it is a very good semiconductor:
  - Large band gap → low noise (also smaller signal)
  - High thermal conductivity → very low power dissipation
  - Large displacement energy → low radiation damage
  - Operates as an ionisation chamber (no pn-junction or doping is required)
  - Only the metal electrodes to collect the charge are required
- 3D diamond detectors use laser to create the columns (electrode) via graphitization of the diamond



Other semiconductor detectors

- Germanium-based [17]:
  - Same working principle than silicon
  - High atomic number, favourable to γ detection
  - Low band gap → cooling down (77K)
  - Lower energy needed to generate pairs
  - High Energy resolution
  - Used in X-rays and gamma detection
  - Low-mass dark matter detection at cryogenic temperatures (mK): CDMS. Phonon detection .

Back and front of a Ge-detector



CDMS Ge-detector

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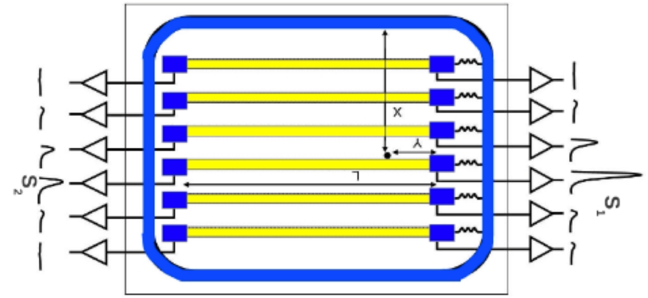
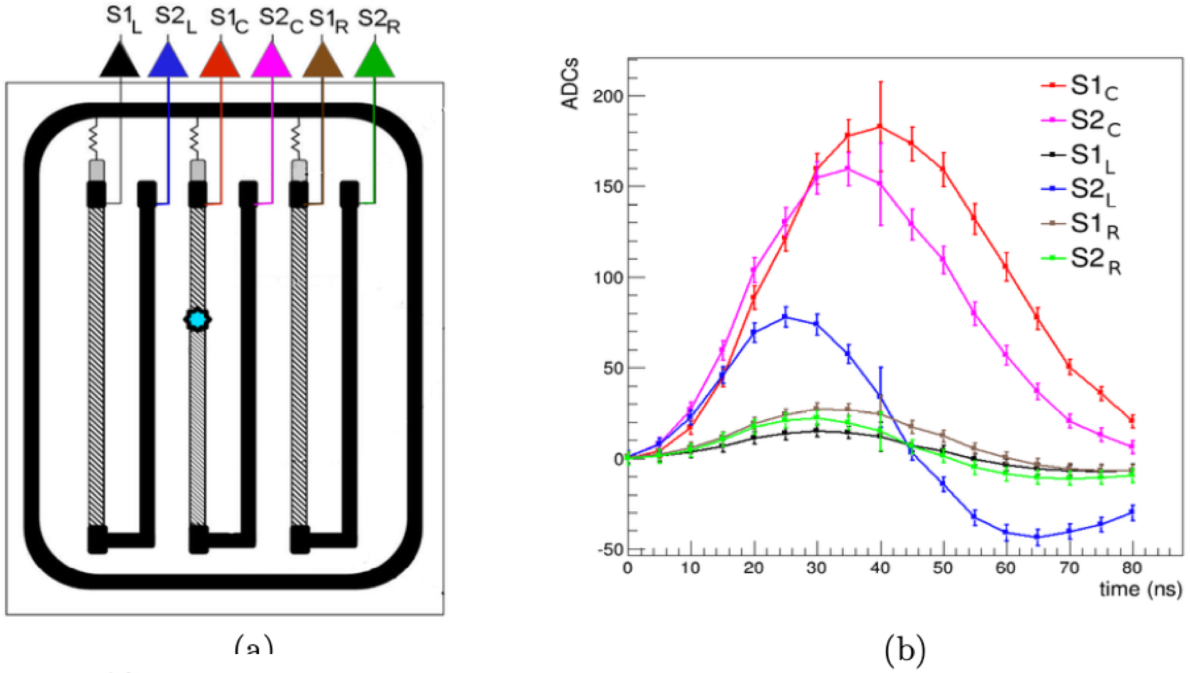
Some “exotic” ideas

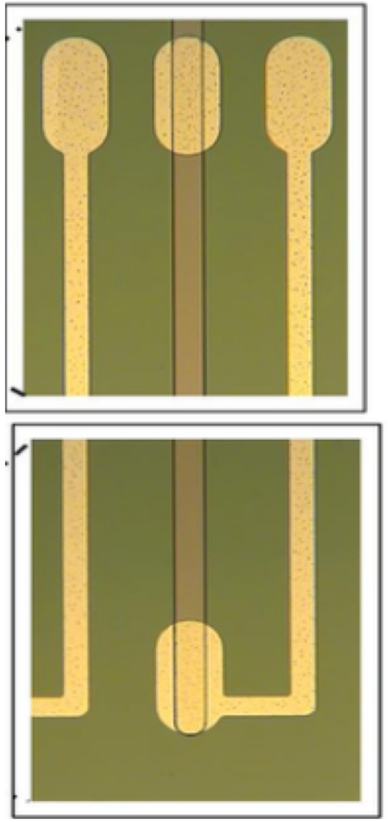
- 2D position sensitive microstrip detector [2] (p=160um, $p_{electronics}$ =80 um)
- **Polysilicon strips** to produce charge division along it.
- In the measurement the clear charge distribution among strips is shown, together to the event signal, there is some coupling contribution
- Polysilicon strips are very useful for alignment sensors (transparent to IR)

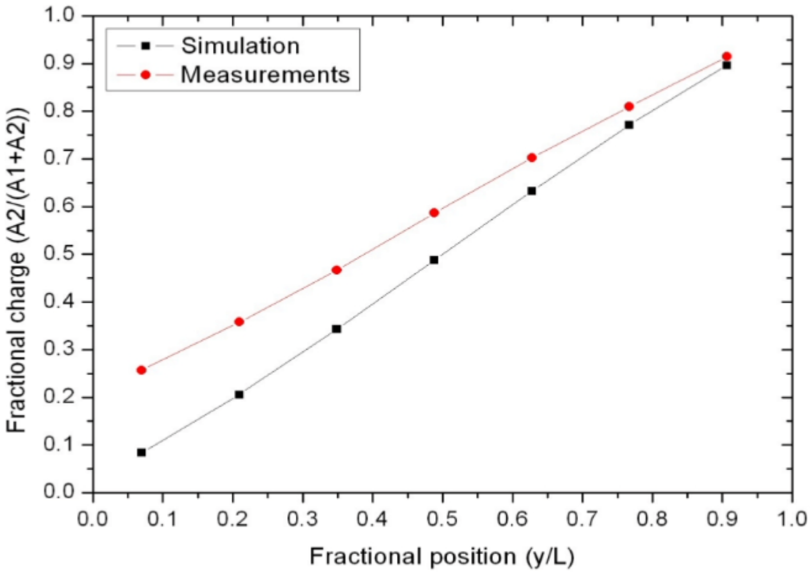




(a)

(b)



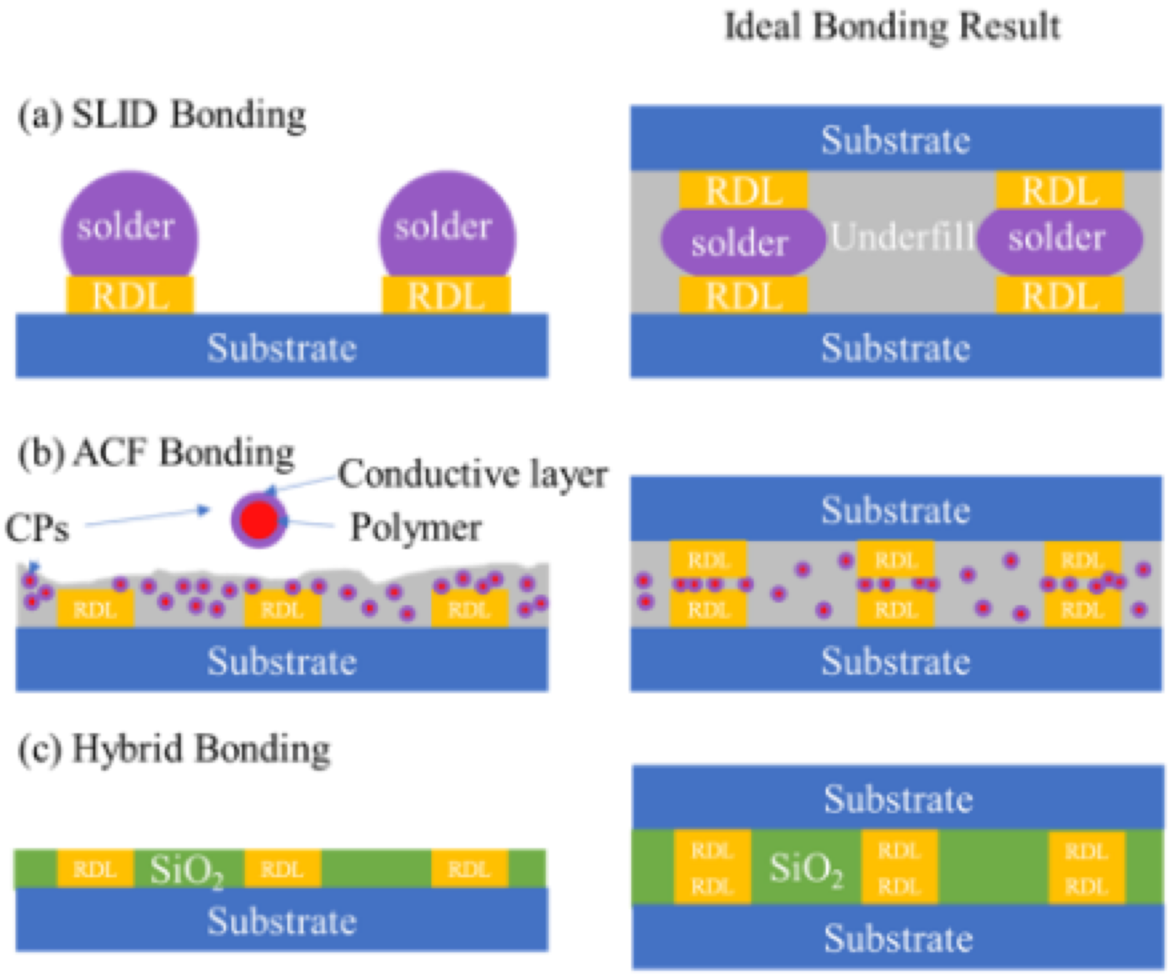


Q8. Look carefully to the results.

Can you understand the blue signal?

Some "exotic" ideas

- The development that could revolt the hybrid detectors technology will be to find a more efficient and less expensive technique to stack up sensors and read out electronics (you will have dedicated lectures on monolithic sensors)
- The three techniques here shown allow finer pitch (RDL-redistribution layer):
  - solid-liquid inter-diffusion
  - Anisotropic conductive film
  - Face-to-face bonding
- There is a significant effort on R&D for better yields



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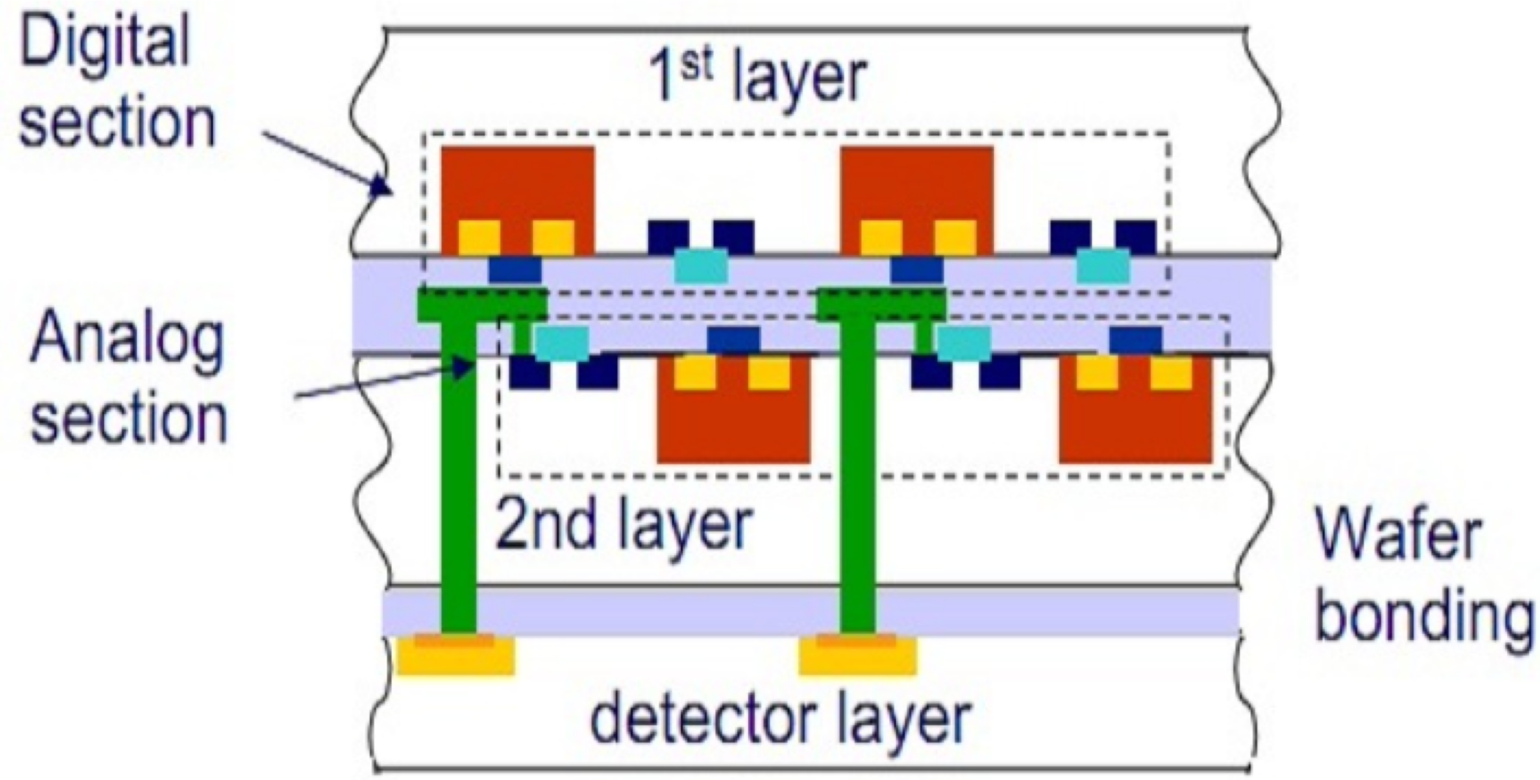
Some “exotic” ideas

- 3D-integration detectors [18]
    - Inter-Chip Vias (ICV)



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Questions

Discussion:

- I haven’t talk about services at all! But they are crucial!
- What do you think is the future/limitations of hybrid detectors for collider trackers? Planar and 3D?
- Advantages and dis-advantages?
- How would you build the best detector performance-wise using these technologies?
- Any missing information that you would add to this lecture?

Feedback Please!

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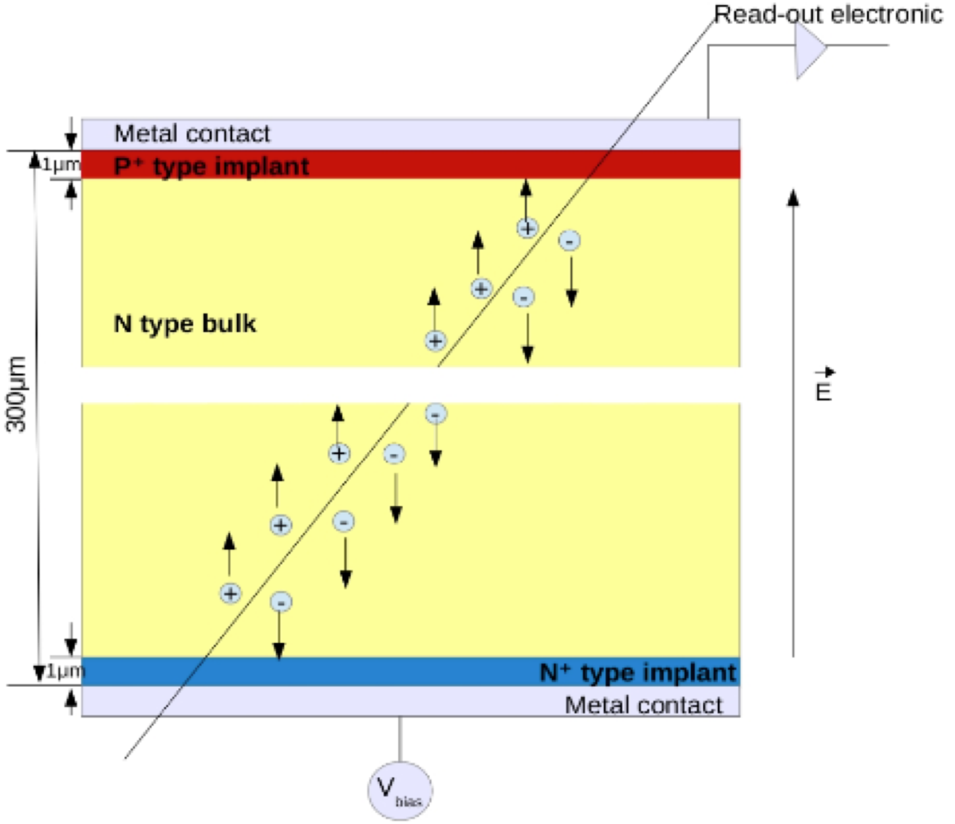
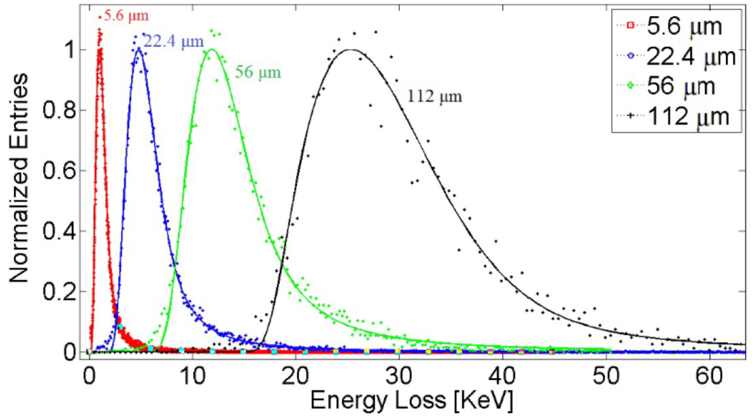
Silicon sensors basics [2]

- Signal generation:
  - Particle deposits energy that produces electron-hole pairs, negative and positive charge carriers. Helped by an electric field created with an external bias voltage, carriers move and induce a current (charge change) on the electrodes. **Ramo's theorem**
  - **Minimum Ionising Particle (MIP)** is a particle whose mean energy loss rate through matter is close to the minimum





Energy loss in different silicon thicknesses, from: https://iopscience.iop.org/article/10.1088/1748-0221/6/06/P06013/pdf