Circuits and layouts II

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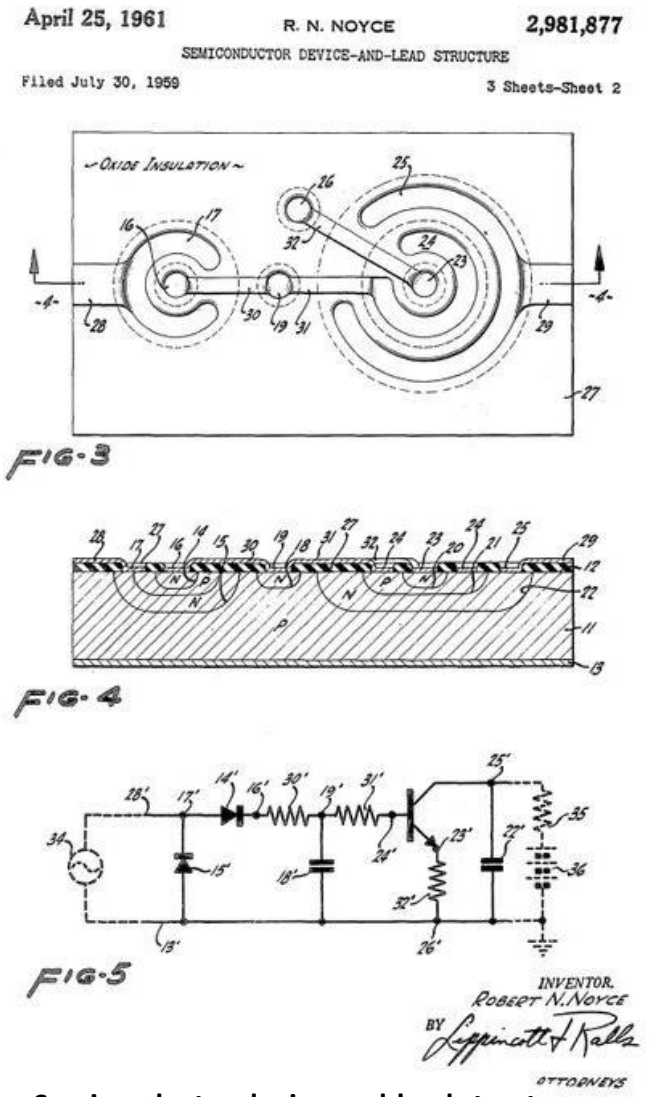
Overview

- **Introduction, definitions**
- **Hybrid and Monolithic Sensors**
- **Example of Monolithic CMOS Sensors layout and fabrication**
- **Isolation techniques**
- **HV biasing**

Introduction

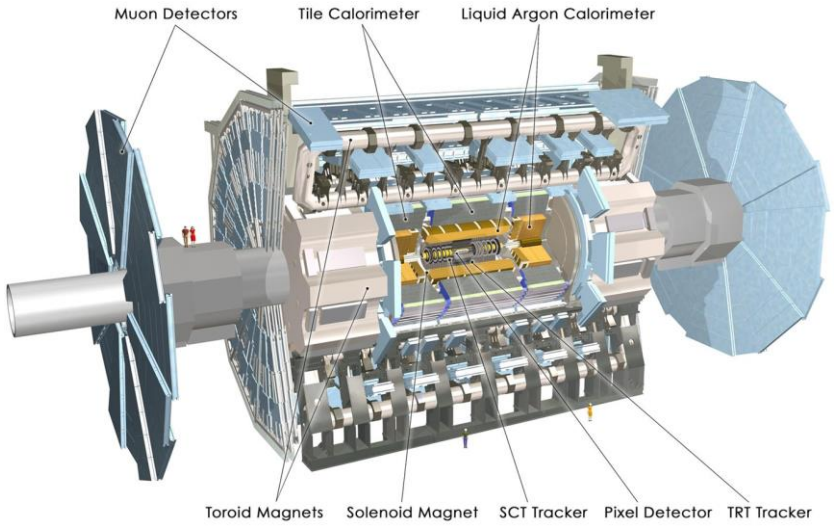
- IC (integrated circuit) single silicon chip that includes active and passive interconnected devices to implement complex operations (analogue, digital)
- Planar technology: the processing steps are implemented in a thin layer of the surface of the chip

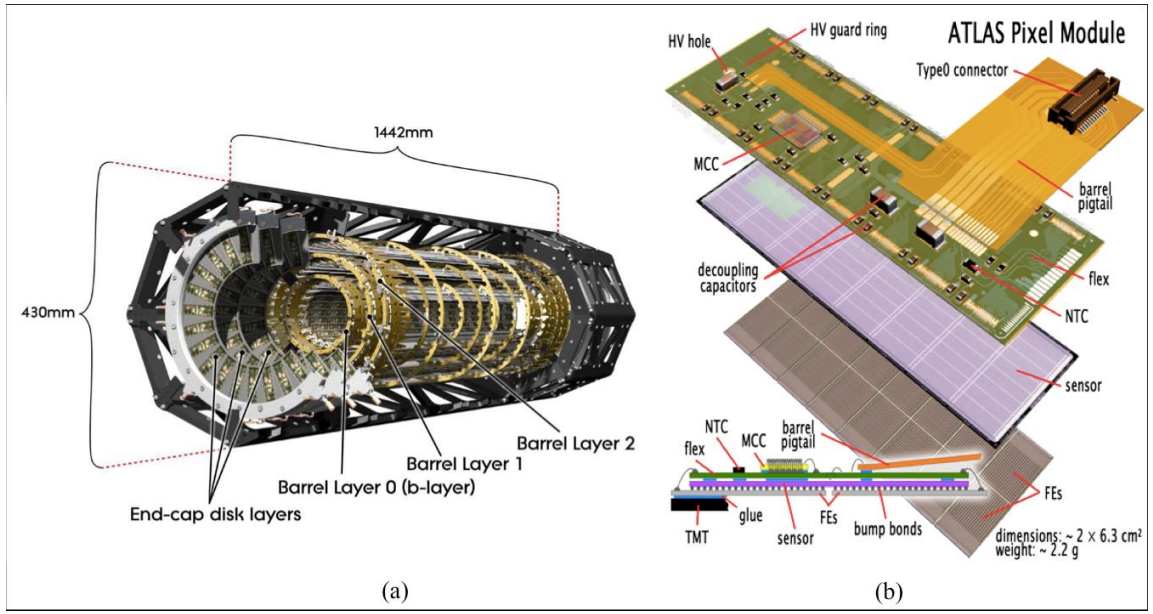


Semiconductor device-and-lead structure
US2981877A
First planar IC patent, 1961

Introduction

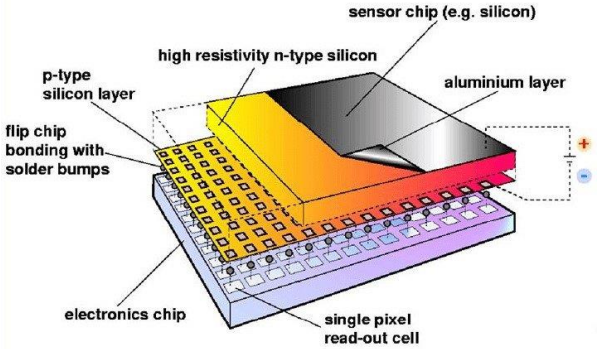
- Planar technology used also for detector fabrication
- Remarkable evolution in planar technologies impacted on detector performances as well
- Historically used '**hybrid**' approach

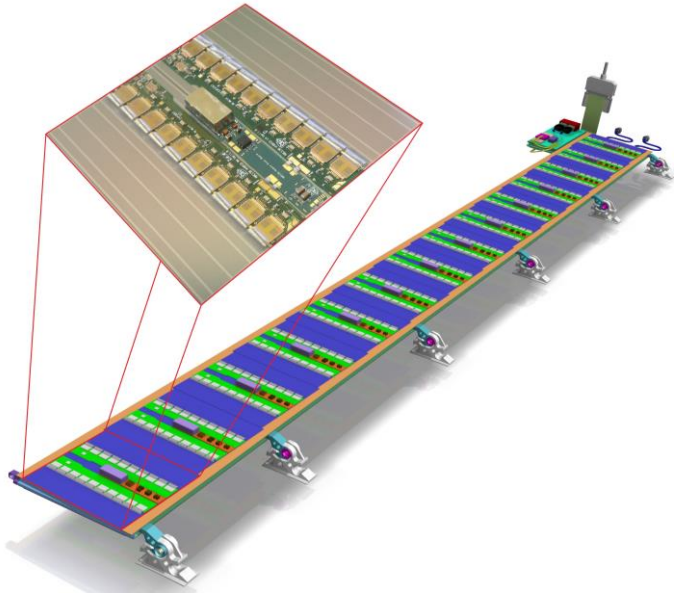




Hybrid solution

- **Hybrid**: different operations are implemented on different silicon chips (like sensing and read out on separate carriers)
    - HR substrate for the sensor optimize the charge collection efficiency and speed
    - It requires complex bonding, affecting reliability, costs
    - Extra material due to the various layers

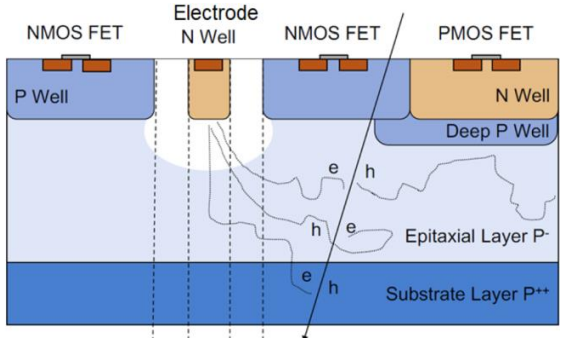




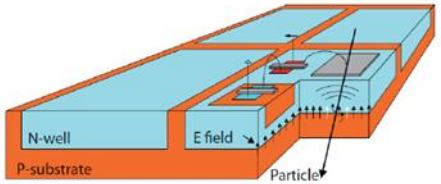
ATLAS Inner Tracker Upgrade (ITk) silicon strip module on barrel stave

Monolithic Solution

- **Monolithic**: sensing and read out are implemented on the same silicon chip
  - Mostly use commercial CMOS process
    - Redundancies of foundries
    - Potentially low cost, large area cover possible
    - High yield
  - Reliability, no need for wire/bump bonding



Deep P Well



Deep N Well

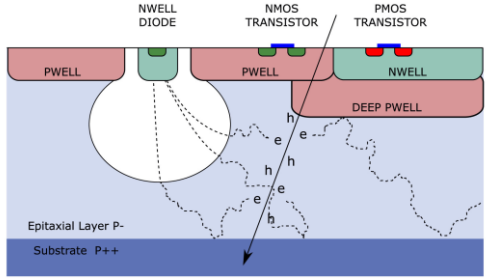
LHC Tracker Upgrades	Area
ALICE ITS	12 m²
ATLAS Pixel	8.2 m²
ATLAS Strips	193 m²
CMS Pixel	4.6 m²
CMS Strips	218 m²
LHCb VELO	0.15 m²
LHCb UT	5 m²

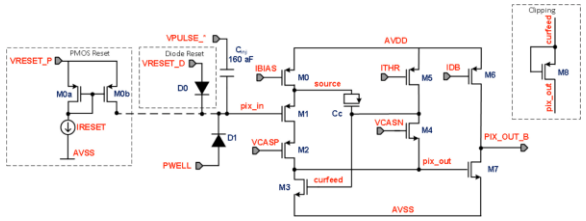
Monolithic approach is an interesting option for most HEP experiments

Monolithic solution

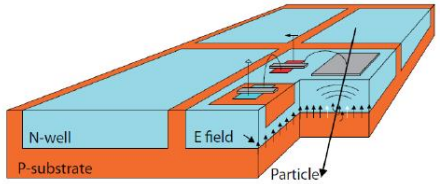
- **Monolithic**: sensing and read out are implemented on the same silicon chip
    - In-pixel processing possible: amplification and digitization integrated in the same chip
    - Small pixels (‘10’s x 10’s um)
    - Low noise, due to small pixel, low leakage, low capacitance
    - Good S/N
    - Sensitive region 10’us um, backthinning possible to reduce mass

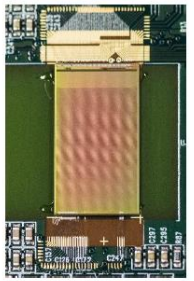
The vertex detector of the STAR experiment, the first to use CMOS MAPS





MAPS used for ALICE ITS upgrade, with in-pixel FE circuitry

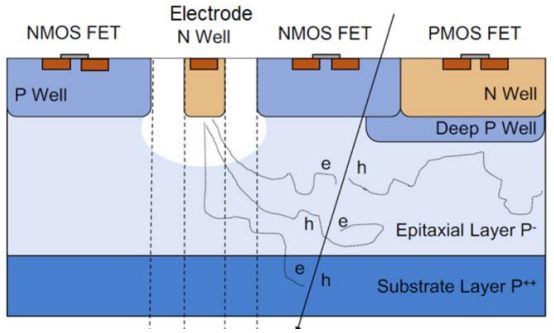




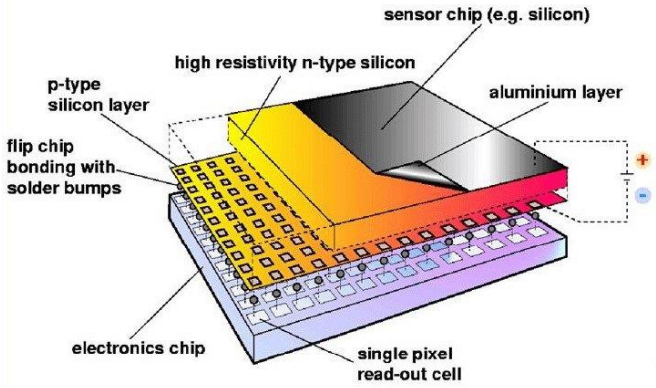
HV MAPS used for Mu3e

Pros and Cons of Hybrid and Monolithic

- **Hybrid and Monolithic** approaches:
  - Guard rings, barrier stops to avoid surface currents required in both solutions
  - Usually high voltage (100's V)are needed for biasing of sensors in hybrid approach: HV biasing technique present additional challenges
  - Lower voltages (10's V) are needed for monolithic: small signals call for optimized S/N from RO electronics



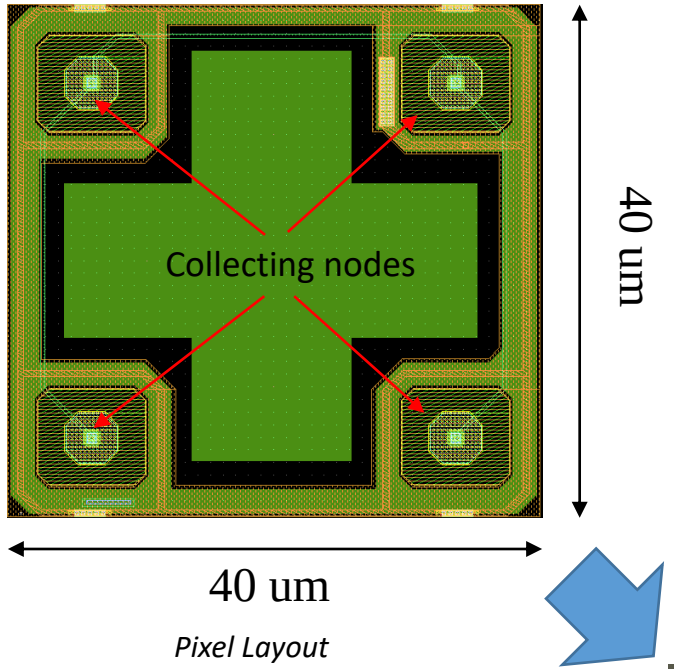
Monolithic Layout, mostly focusing on Sensor part (monolithic RO will be covered by others)



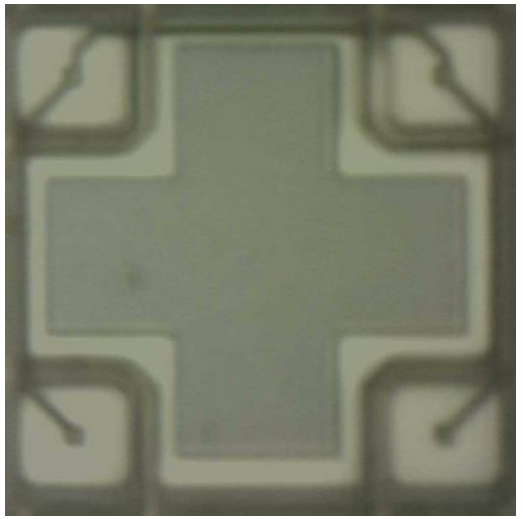
Hybrid Layout, mostly focusing on sensor HV biasing

Example: Monolithic CMOS sensor Layout and fabrication

- Example of fabrication process of a monolithic devices (OVERMOS) using a (simplified) CMOS process
- Sensor implemented in p-type Silicon epi 18 um thick
- Layout of the cell includes 4 collecting diodes isolated by a p-well
- Only ¼ layout is processed, at the end it will be mirrored and reflected to obtain the full cell



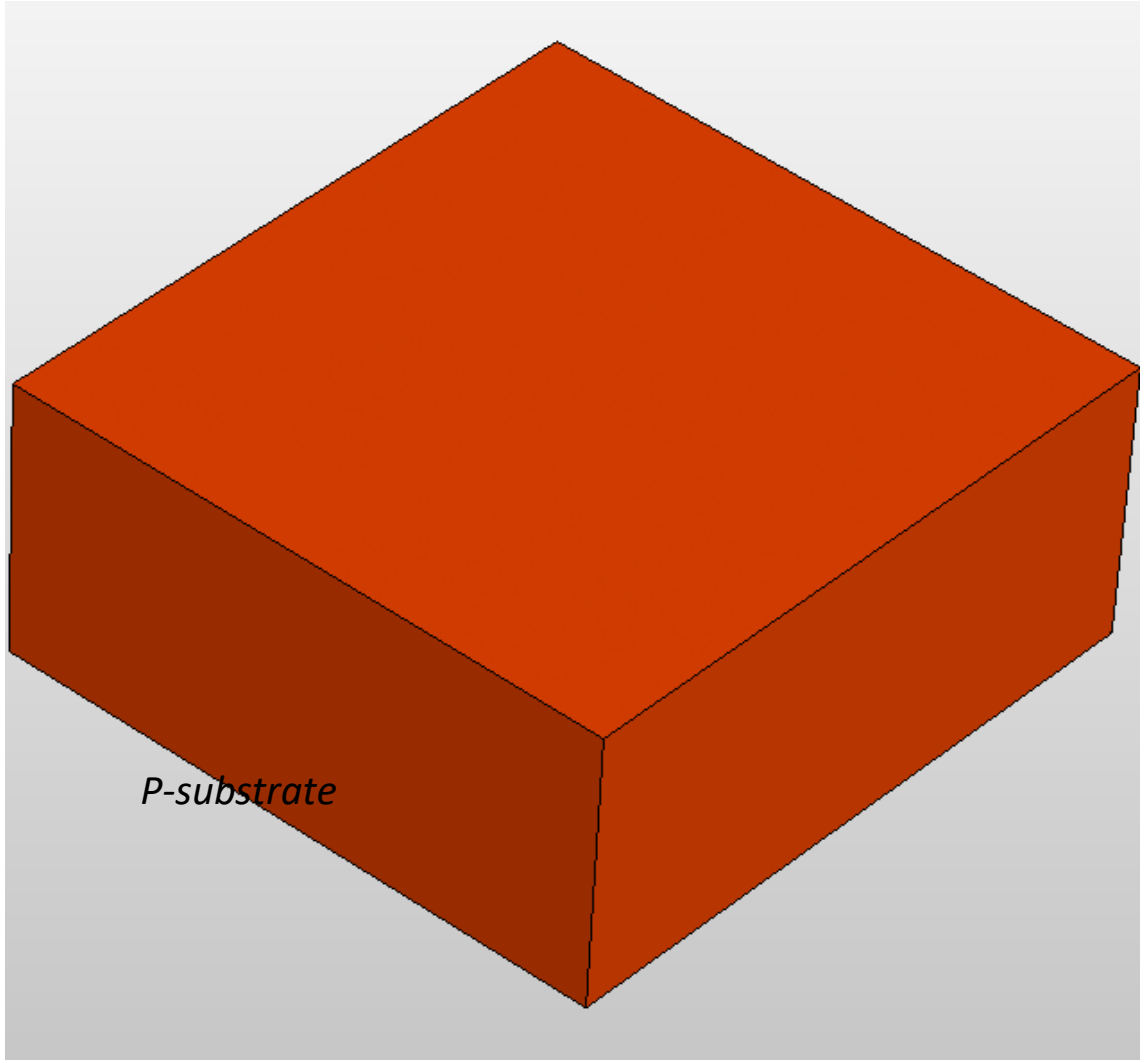
Pixel Layout



Picture of real cell

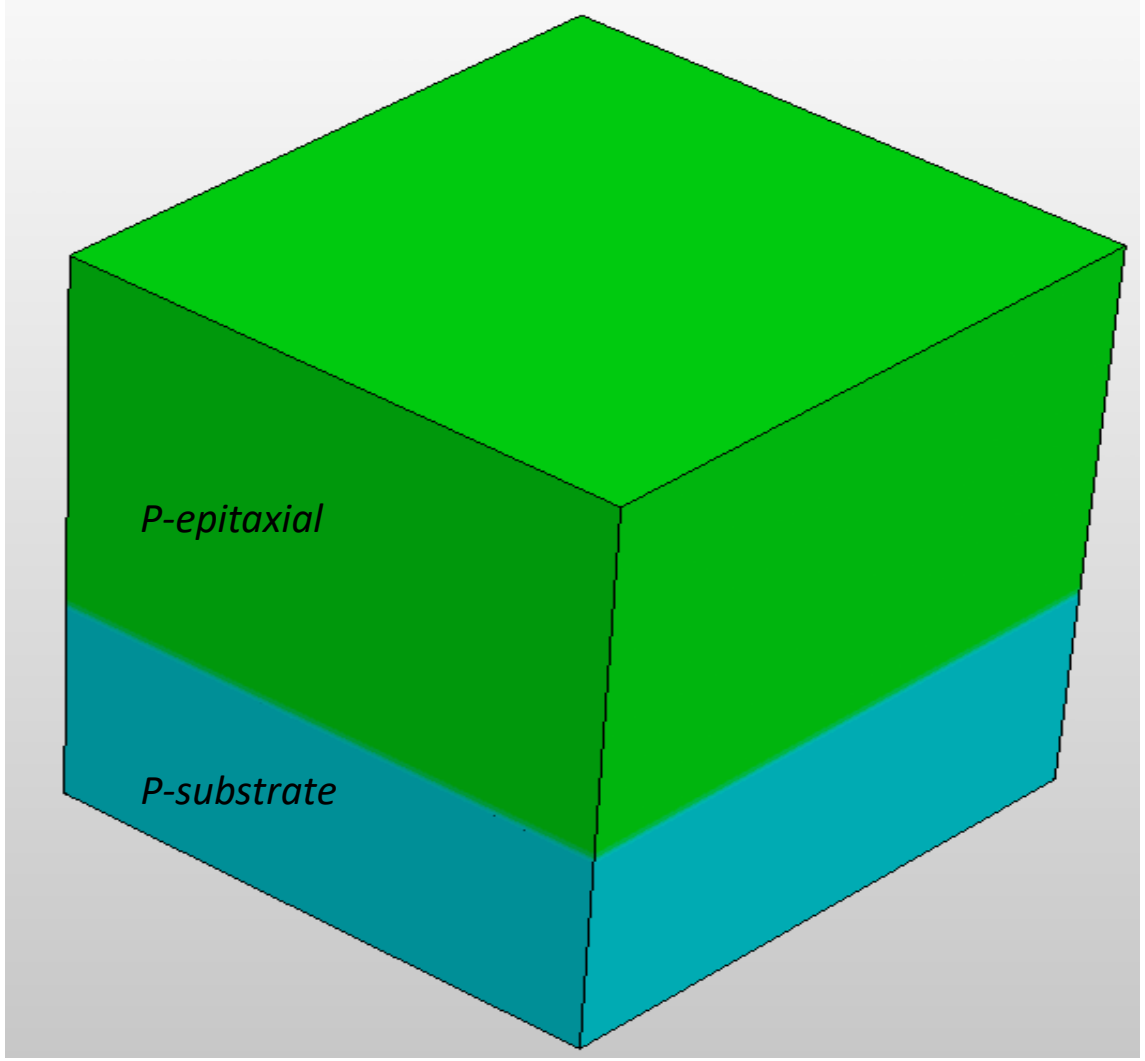
Example: Monolithic CMOS sensor Layout and fabrication

- Silicon substrate P-type CZ $N_A \sim 5 \bullet 10^{18}$ cm^{-3}
- Typical doping > 10^{18} cm^{-3}



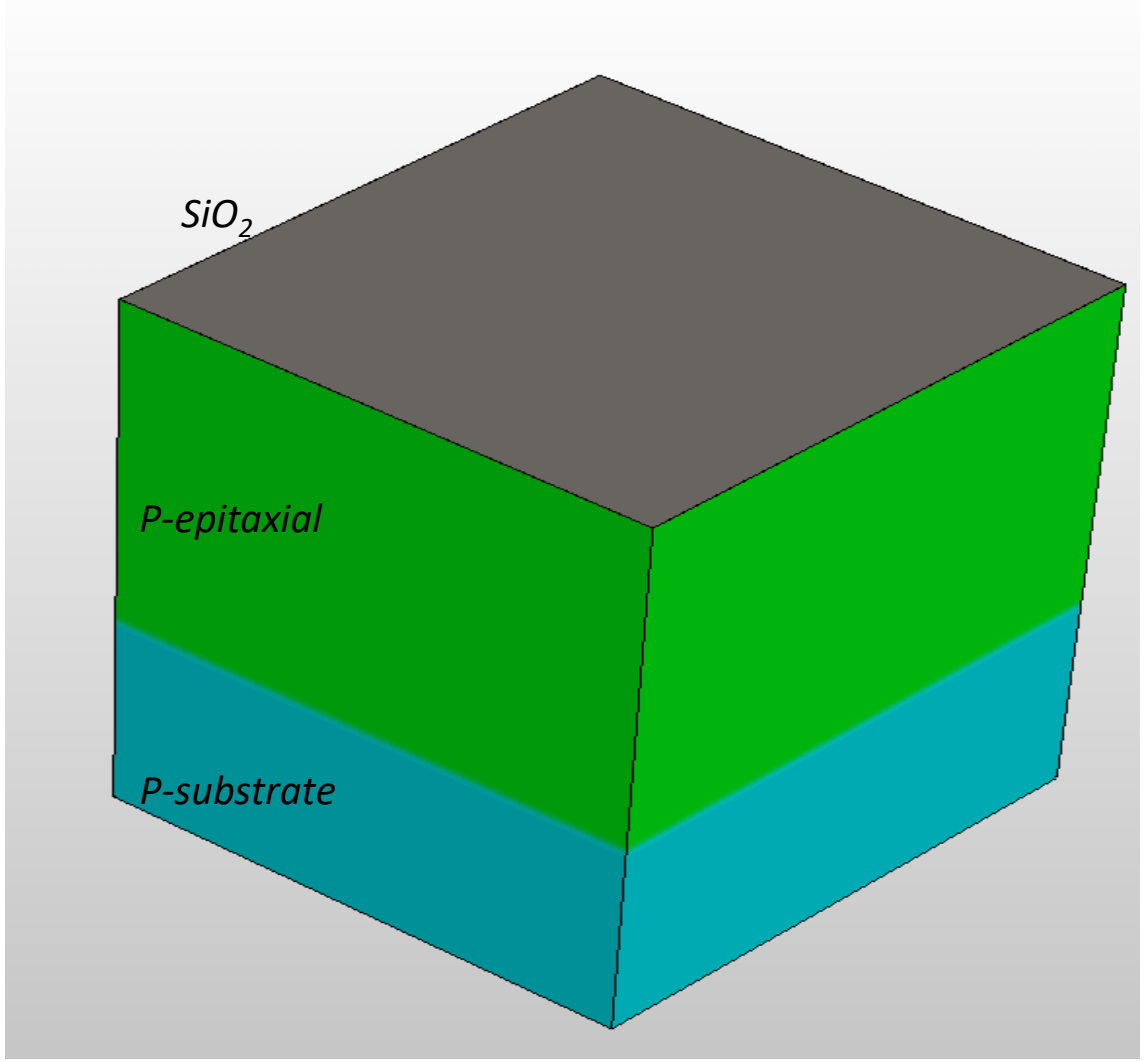
Example: Monolithic CMOS sensor Layout and fabrication

- Epitaxial silicon growth 18 um thick <100> doping ~ 10^{13} cm^{-3}
- Temperature 1000 C, 600 sec anneal



Example: Monolithic CMOS sensor Layout and fabrication

- Thermal oxide growth 8 nm
- $Si+O_2$ @ 1000 C P = 1 atm

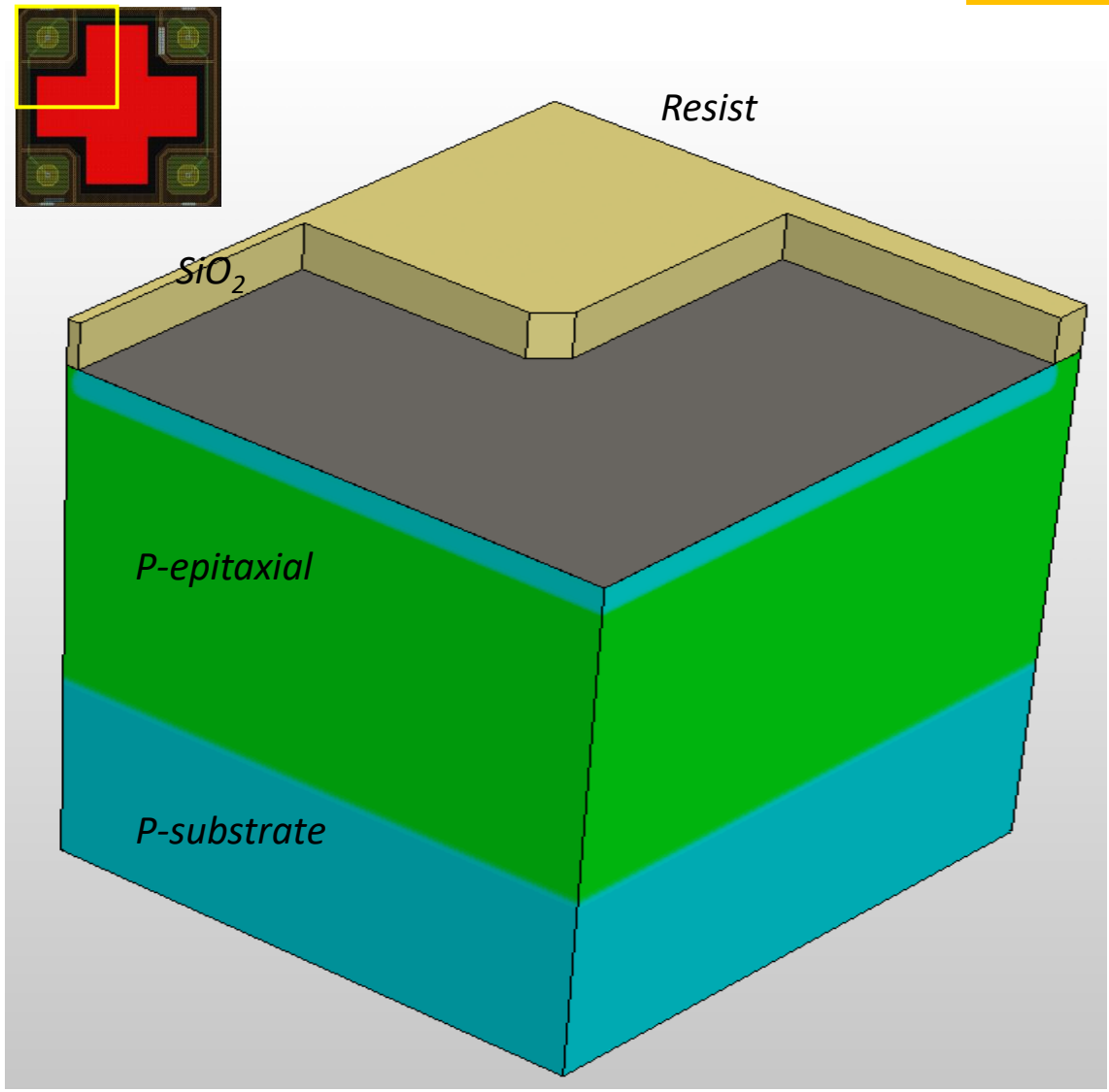


Example: Monolithic CMOS sensor Layout and fabrication

- Resist deposition >1 µm
- Patterning via mask
- Resist development
- Strip resist

- B^{11} implantation (PW well)

- Strip residual resist

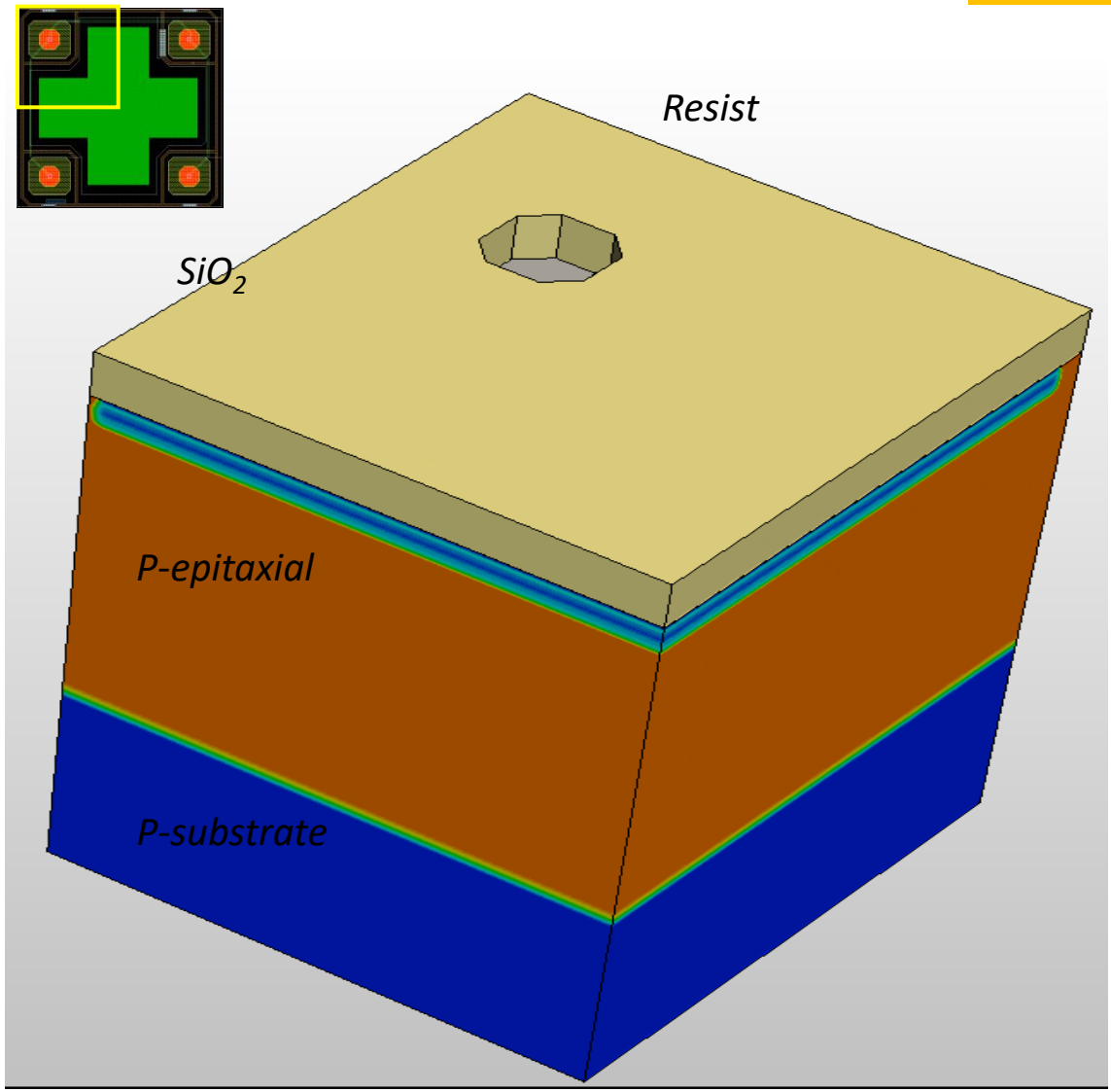


Example: Monolithic CMOS sensor Layout and fabrication

- Resist deposition >1 µm
- Patterning via mask
- Resist development
- Strip resist

- P^{31} implantation (NW well)

- Strip residual resist

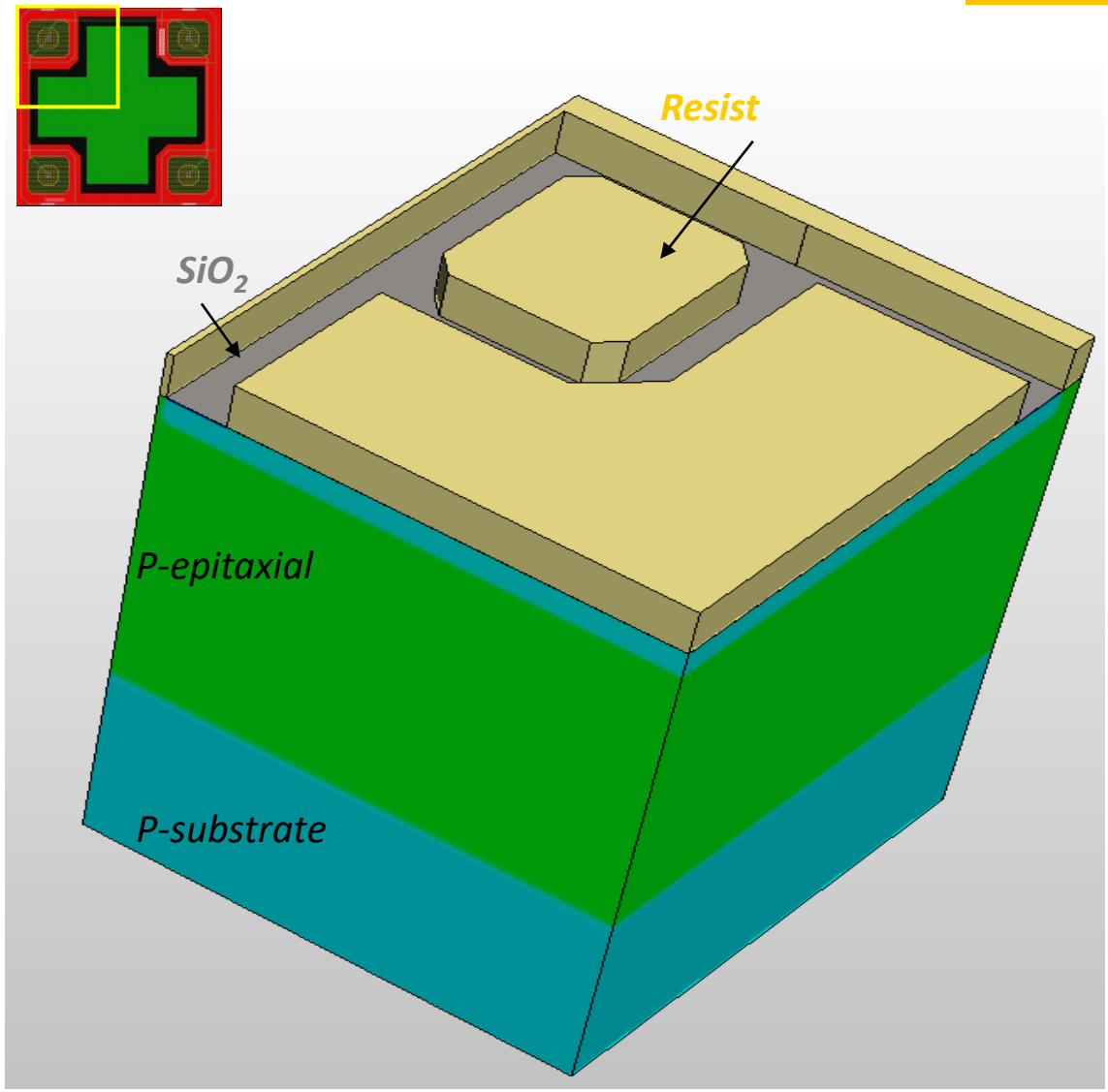


Example: Monolithic CMOS sensor Layout and fabrication

- Resist deposition >1 µm
- Patterning via mask
- Resist development
- Strip resist

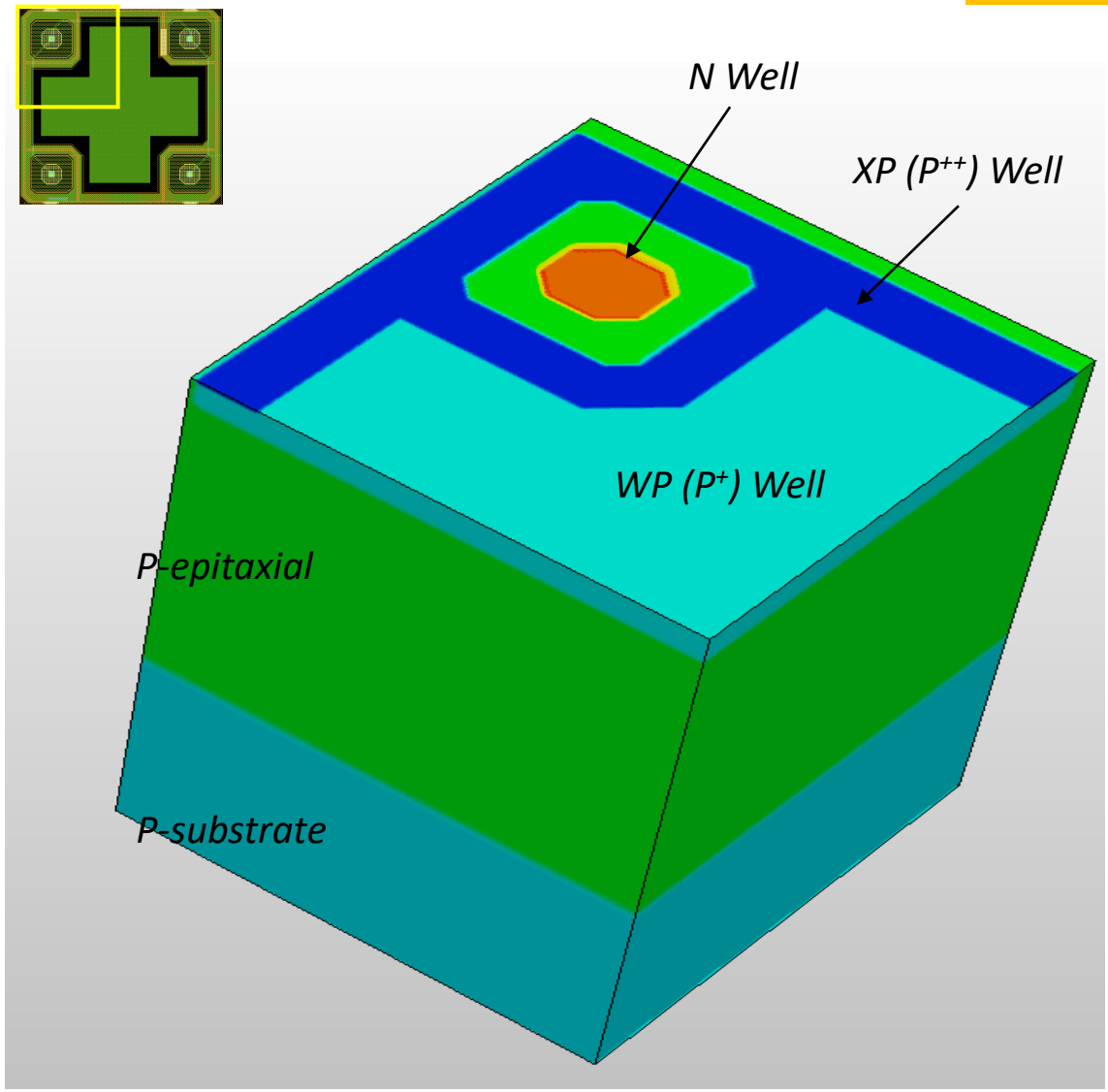
- B^{11} implantation (XP well)

- Strip residual resist



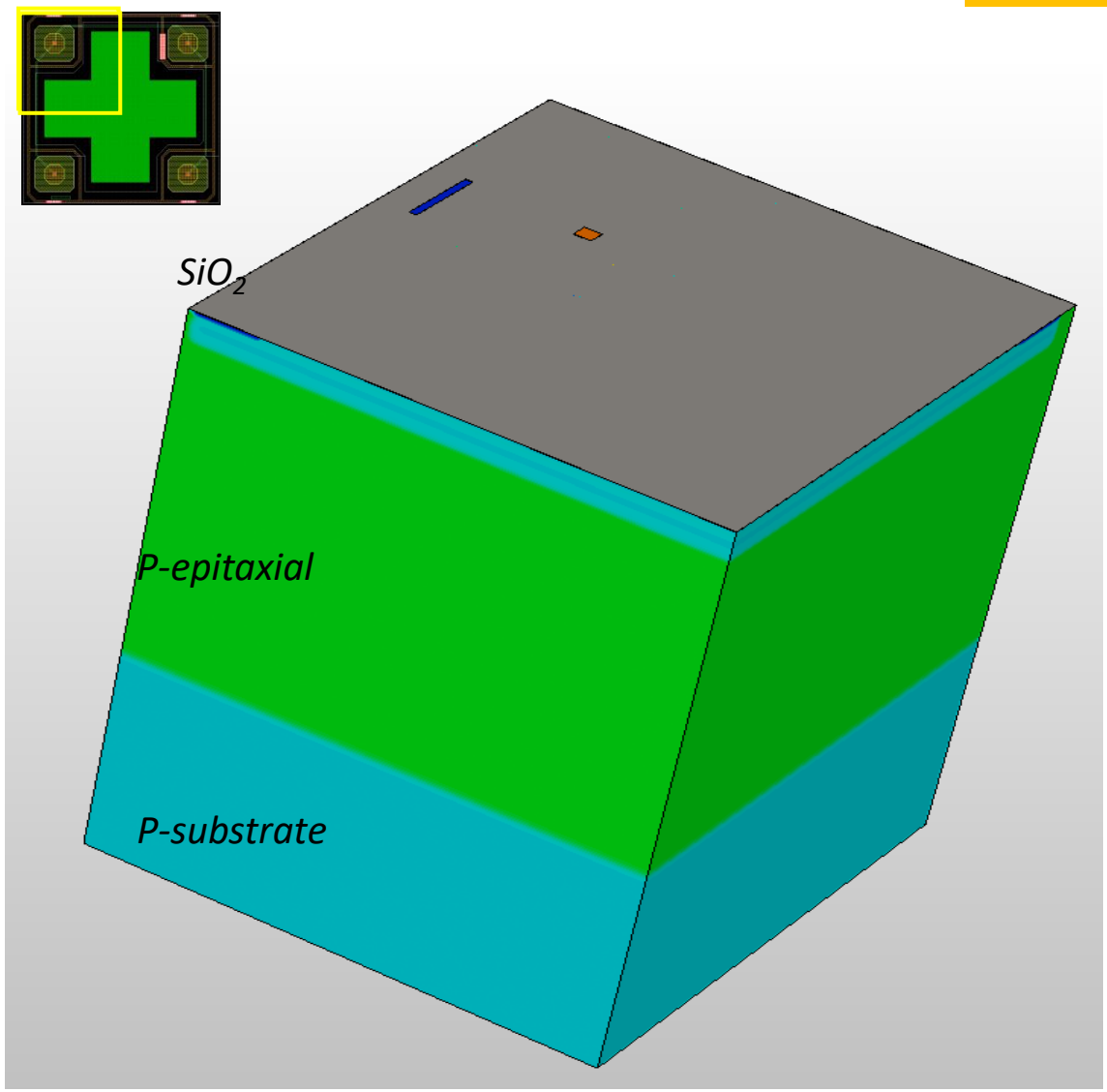
Example: Monolithic CMOS sensor Layout and fabrication

- RTA temperature up to 1022 °C, 20 secs. max
- Strip residual resist



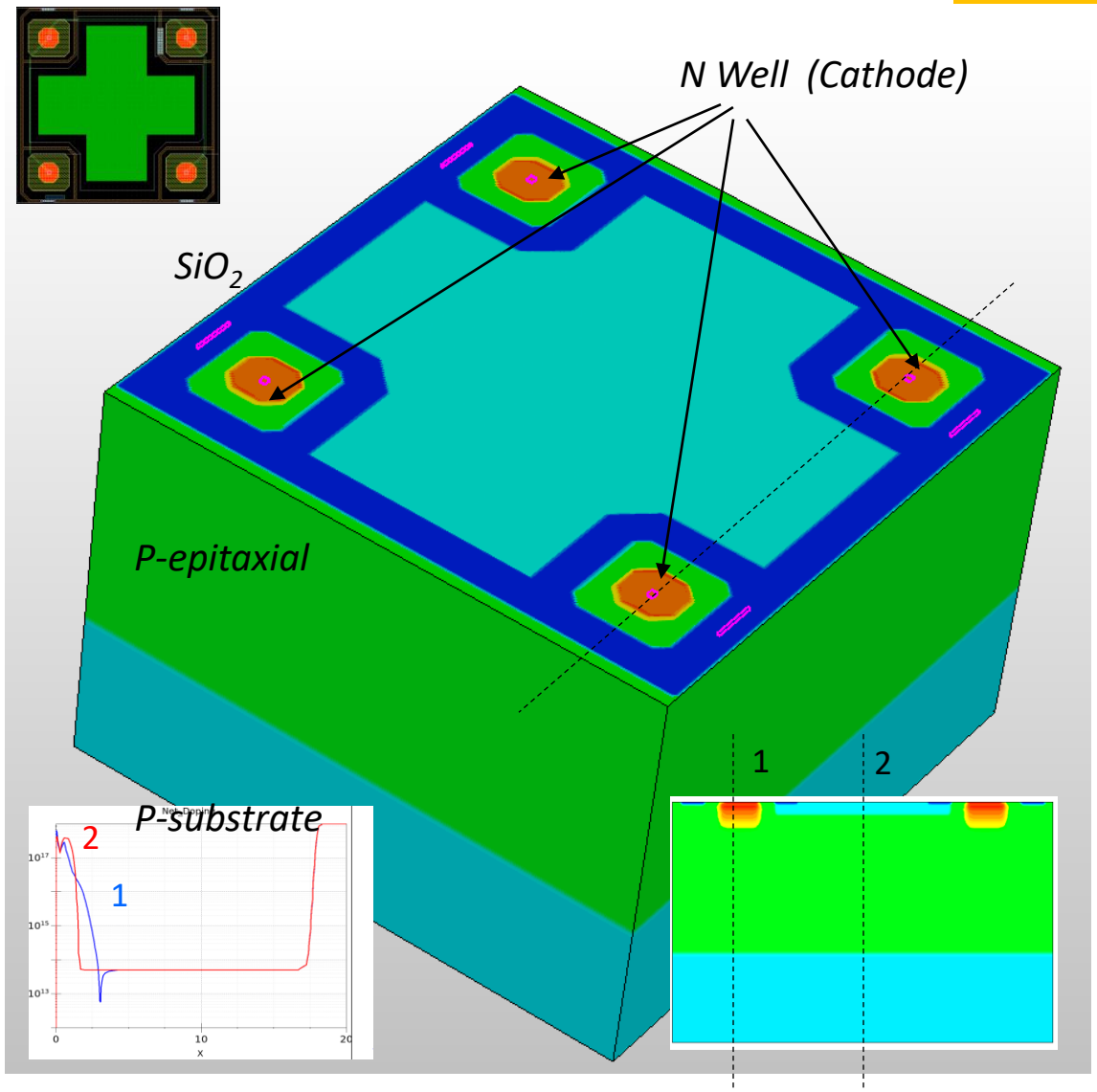
Example: Monolithic CMOS sensor Layout and fabrication

- SiO_2 anisotropic (dry) etching for VIAs and contacts placement



Example: Monolithic CMOS sensor Layout and fabrication

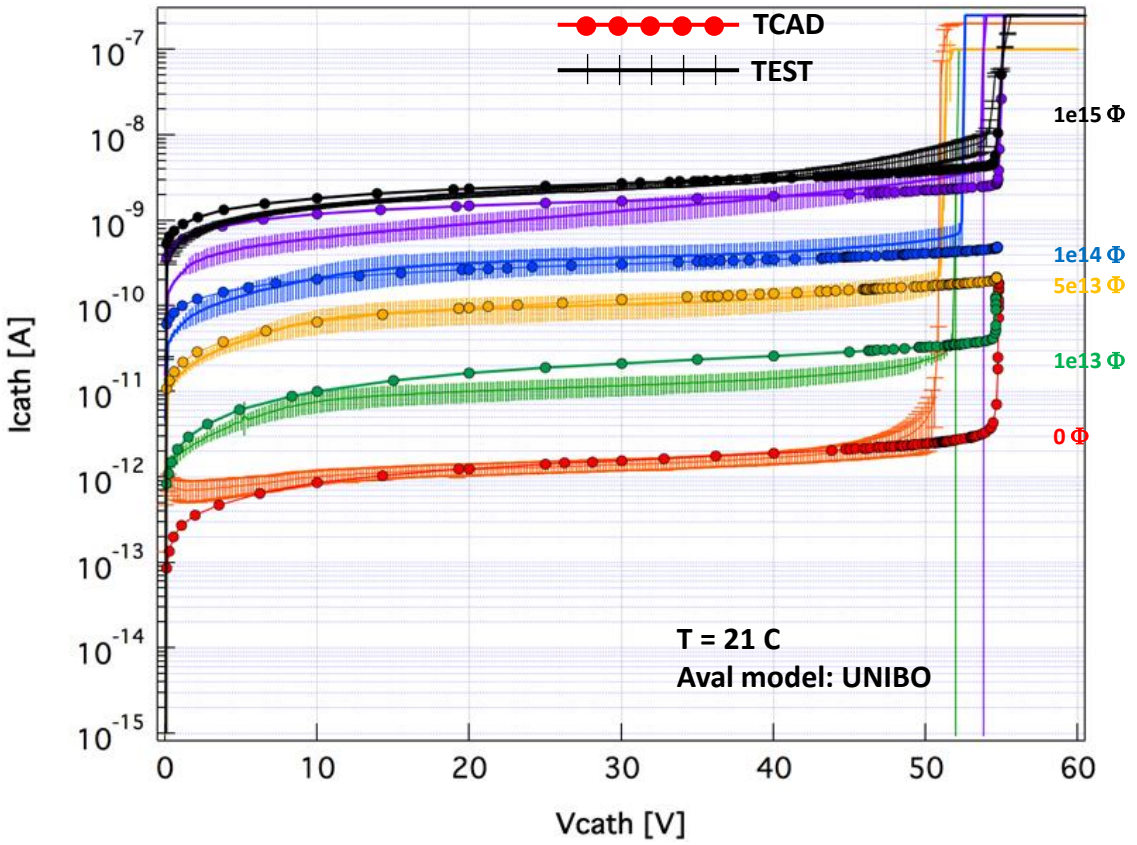
- The simulated model is reflected and mirrored to get a full realistic device
- Around 10,000 secs to ‘build’ a simulated model cell of 40 x 40 μm^2 on a 4-core 3.6GHz machine 16 GB
- Resolution to < nm (fraction of Debye length) in some regions (Si-SiO_2 interface, PN junctions)



Example: Monolithic CMOS sensor Layout and fabrication

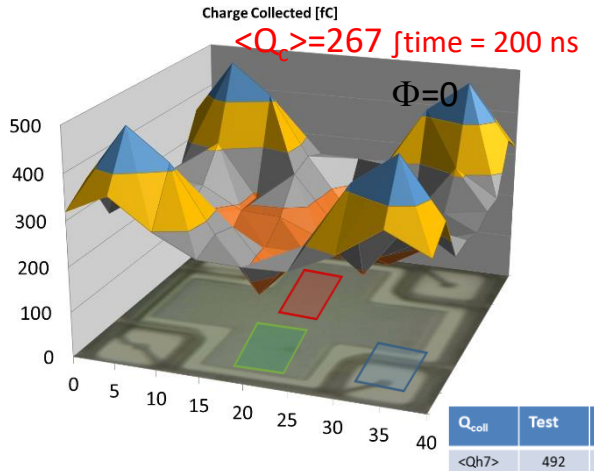
- Simulated devices compare reasonably well with real devices in DC

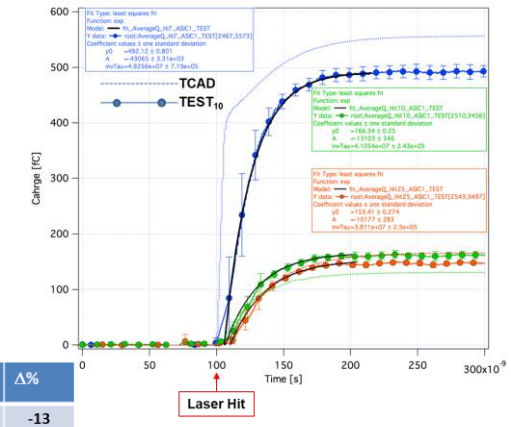
- Also including radiation damage effects (neutron bulk damage up to 10^{15} 1 MeV n-eqv fluence – Penta traps Hamburg model)



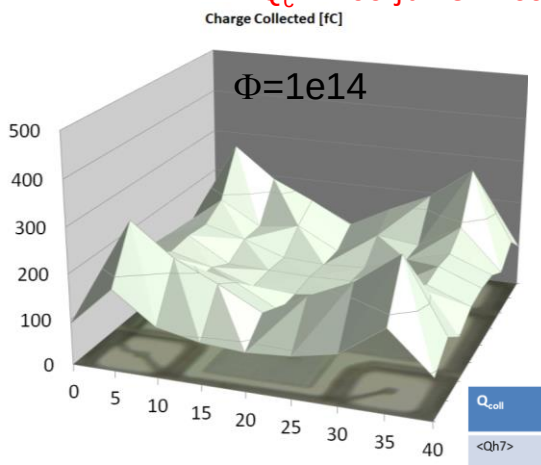
Example: Monolithic CMOS sensor Layout and fabrication

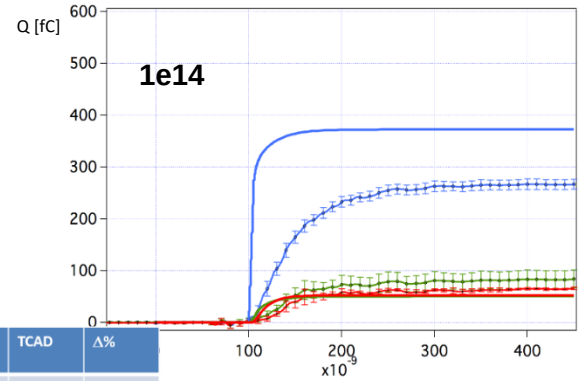
- Approximately 15% overestimate in Charge Collection when non-irradiated, up to 70% for neutron irradiated devices (depending on fluence)





Q_{coll}	Test	TCAD	Δ%
<Qh7>	492	556	-13
<Qh10>	166	131	21
<Qh25>	153	166	-8.4

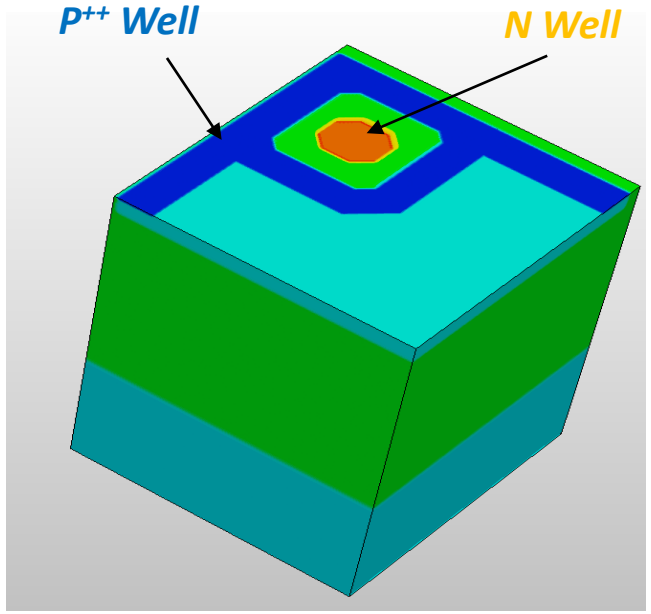


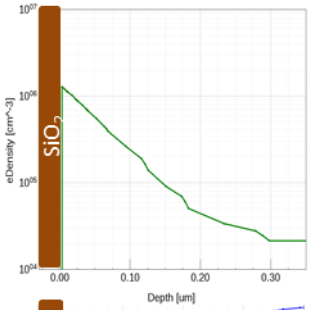


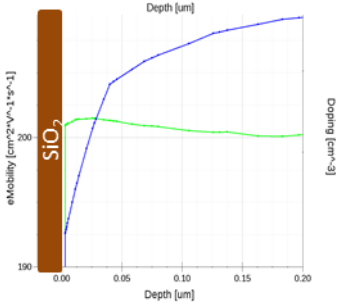
Q_{coll}	Test	TCAD	Δ%
<Qh7>	265	373	-40
<Qh10>	82	51	37
<Qh25>	65	53	18

Example: Monolithic CMOS sensor Layout and fabrication

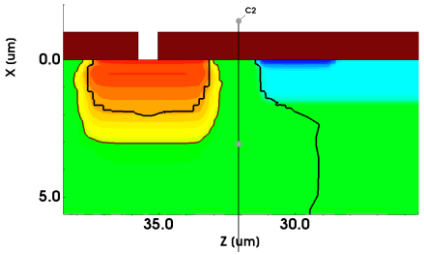
- The presence of XP region helps isolate the collecting wells
- At interface of SiO_2/Si interface states usually positively charged
- An inversion channel is created, especially important in low doped substrate







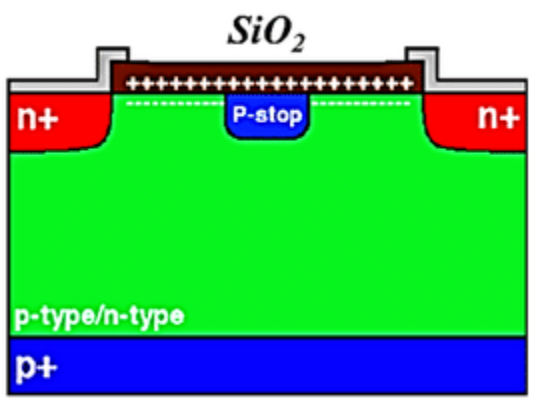
Interface Defect	Level	Concentration	σ
Acceptor	E_C-0.4 eV	40% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Acceptor	E_C-0.6 eV	60% of acceptor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV
Donor	E_V+0.7 eV	100% of donor N_{IT} (N_{IT}=0.85·N_{OX})	0.07 eV



* ***Effects of Interface Donor Trap States on Isolation Properties of Detectors Operating at High-Luminosity LHC***, *DOI:* 10.1109/TNS.2017.2709815

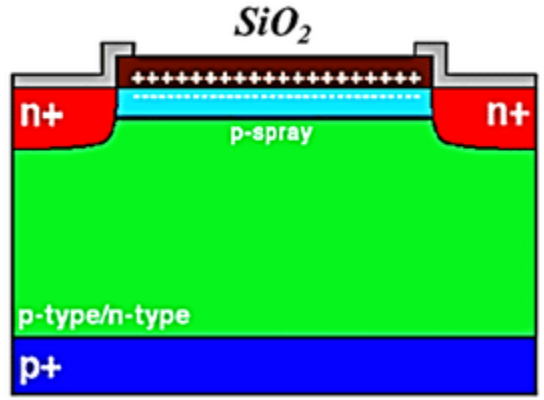
Isolation techniques

- Non-irradiated sensors, fixed positive charge around 2e11 cm^{-2} (technology dependent)
- Values up to > 1e12 cm^{-2} following irradiation
- Good isolation among n collecting wells is needed
- P-stop and p-spray isolation techniques



*The **floating p+ stop** method consists of placing a p+ implant in between two adjacent n+ strips*

It requires an additional mask



*The **p-spray** method consists of having uniform p+ layer beneath the Si/SiO2 interface.*

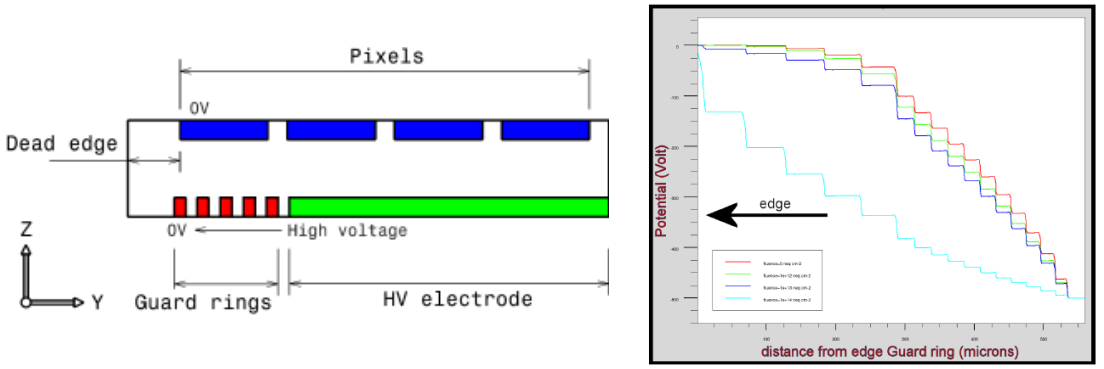
It requires careful dose of doping (too low does increase BV but does not isolate, too high isolate but decreases BV)

Isolation techniques

- The biasing of sensors with High voltage is required to guarantee good charge collection efficiency and short collection time

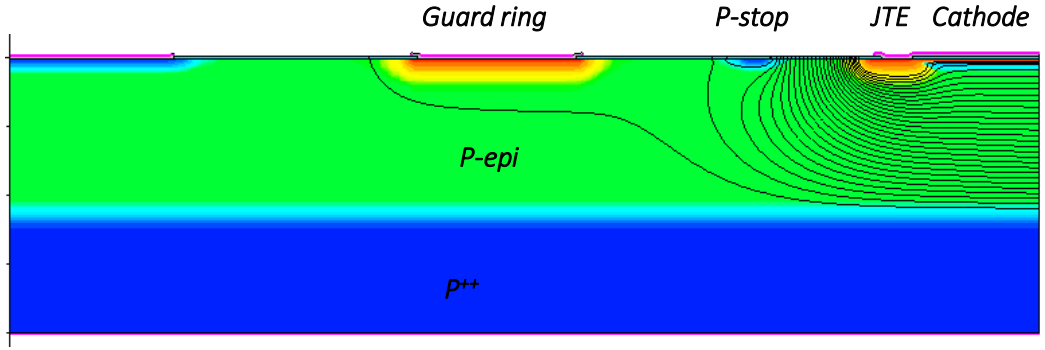
- The biasing voltage is usually increased following sensors irradiation, due to loss of charge collection efficiency

- Techniques are needed to suppress the likelihood of breakdown



Multi guard rings *improve the high voltage operation, by decreasing the electric field at the sensor edge*

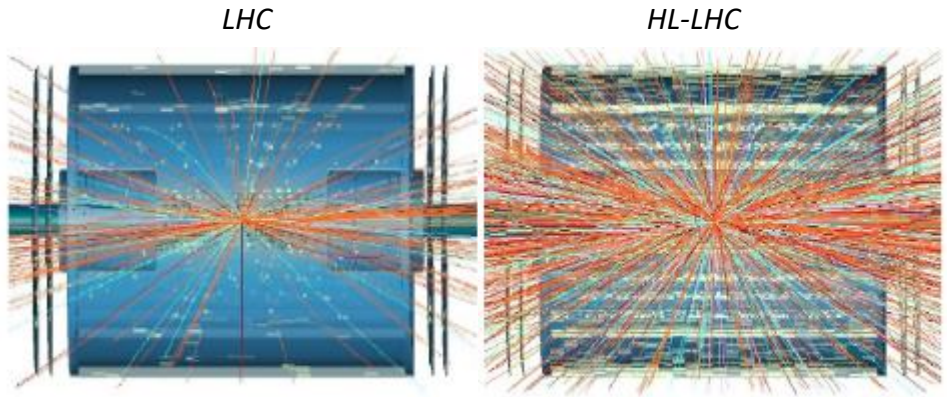
Simulation of guard ring influence on the performance of ATLAS pixel detectors for inner layer replacement DOI: 10.1088/1748-0221/4/03/P03025



The use of ***junction termination extension*** *(JTE) reduces gradually the potential from the edge of the sensor, decreasing the field*

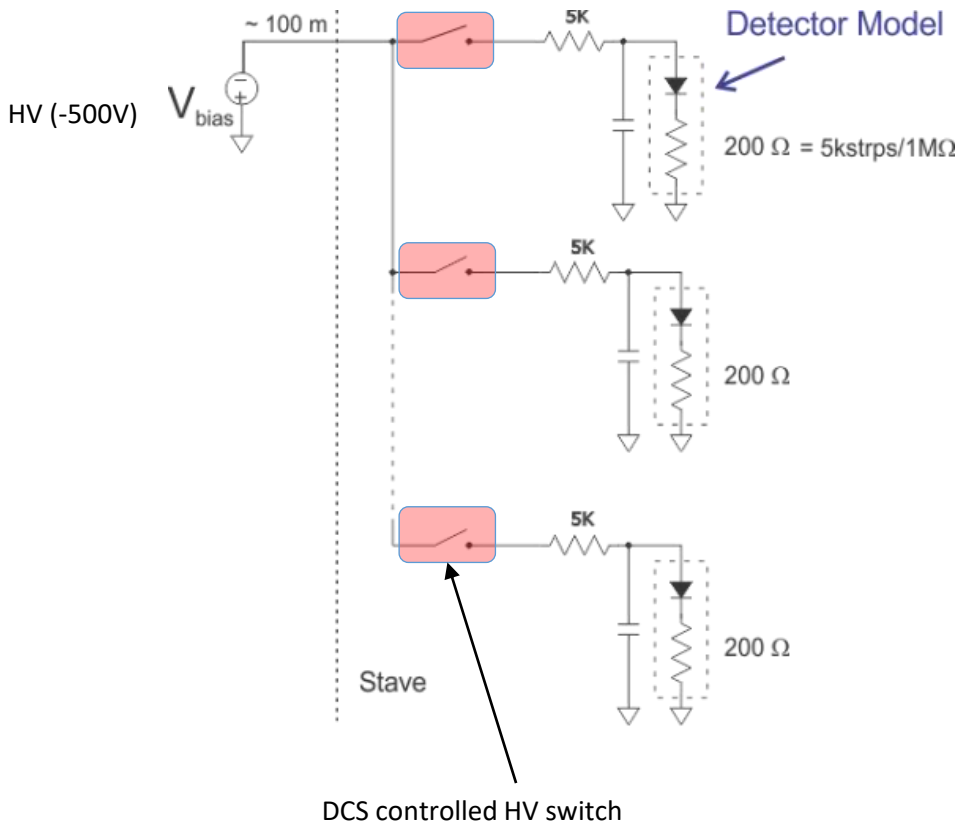
HV biasing hybrid approach

- Current ATLAS SCT uses independent powering for the 4088 detector modules. Each sensor has its own independent HV bias line.
- ‘ideal’ solution:
  - High Redundancy
  - Individual enabling or disabling of sensors and current monitoring
- The increased number of sensors in the Upgraded Tracker (>10 k modules in barrel upgrade vs. ~2 k in present barrel) implies a trade off among material budget, complexity of power distribution and number of HV bias lines



HV biasing

- Use single (or more) HV bus to bias in parallel all sensors and use one HV switch for each sensor to disable malfunctioning sensors: High Voltage Multiplexing ‘HVMUX’
- The HV switch is DCS controlled, with control signals provided by custom ASIC



HV biasing

High Voltage switches strip detector requirements:

- **Rated to 500V** plus a safety margin
- **Must be radiation hard**, nominal maximum expected ~1x10^{15} n_{eq}/cm^2 , ~ 30Mrad (Si) for strip end cap. Multiply by 1.5 to include safety margin
- **On-state impedance** R_{on} << 1kΩ // I_{on} ~ 10mA (for irradiated strip sensors)
- **Off-state impedance** R_{off} >> 1GΩ // I_{lkg} << I_{sens}
- **Must be unaffected** by magnetic field
- **Must maintain satisfactory performance** at -30° C
- **Must be small (mass/area constraint) and cheap** (around 1E4 needed)

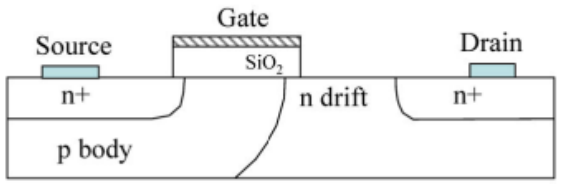
Partial list of investigated HV devices

Crystalonic 2N6449	Si JFET	300V	FAILED
Interfet 2N6449	Si JFET	300V	FAILED
IXYS CPC5603	Si MOSFET	410V	FAILED
ROHM R6006ANX	Si MOSFET	600V	FAILED
Infineon IPA50R950CE	Si MOSFET	500V	FAILED
Semisouth SJEP170	SiC JFET	1700V	PASS – N.A.
USCi UJN1205	SiC JFET	1200V	FAILED
CREE CPMF-1200	SiC MOSFET	1200V	FAILED
ROHM S2403	SiC MOSFET	1700V	FAILED
GeneSiC GA04JT17	SiC BJT	1700V	FAILED
TranSiC FSICBH057A120	SiC BJT	1200V	FAILED
Transphorm TPH2006C	GaN JFET	600V	FAILED
EPC2012	GaN JFET	200V	PASS
GS66502B	**GaNFET**	**650V**	**PASS**
PGA26E19BV	**GaNFET**	**600V**	**PASS**

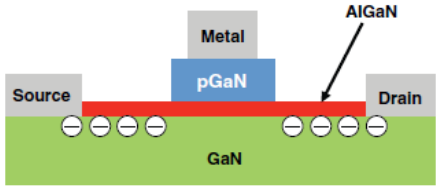
HV biasing

- Typical Si HV MOSFET use regions of low doping to increase high voltage capabilities: this affects their radiation hardness

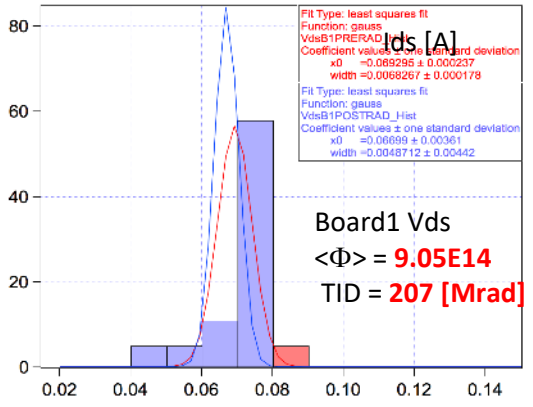
- Non-ionizing and ionizing irradiation test results of GaN FET devices indicate very high radiation hardness



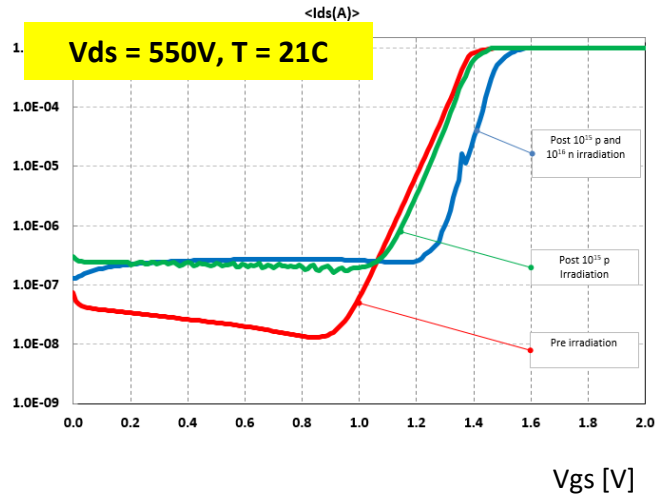
*A Lateral Double-Diffused MOS (LDMOS). A **long drift region of lower doping** reduces the electric field*



Example Xsection of a HEMT E. GaN FET. Strain-induced polarization at interface forms a 2DEG



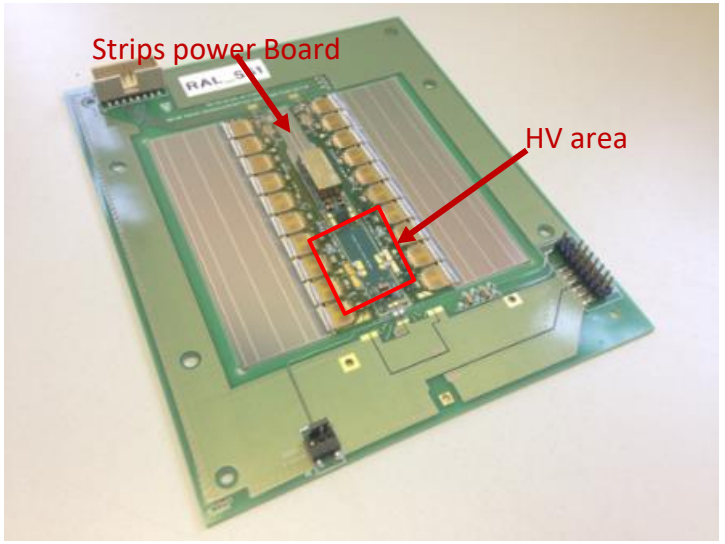
GaN Vds shift with irradiation



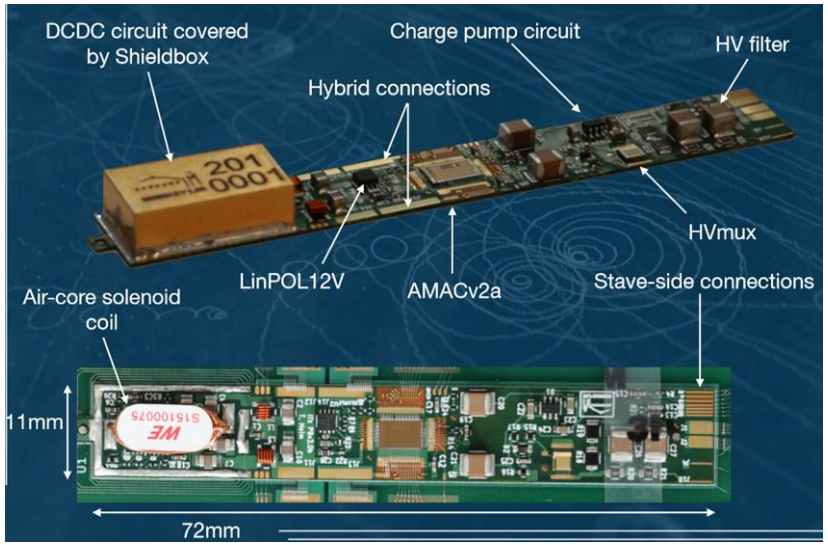
*Additional test performed on 18 devices Total **p** fluence **1.0E15, ~**TID **200Mrad(GaN)** Total n fluence **1.0E16***

HV biasing

- The HVMUX sits on the lower side of a flexi power board (PB).
- The PB final version incorporates power control and HVMUX elements in the AMAC (Autonomous Monitor And Control) ASIC.



A barrel short strip module with two hybrids and one powerboard with HVMUX

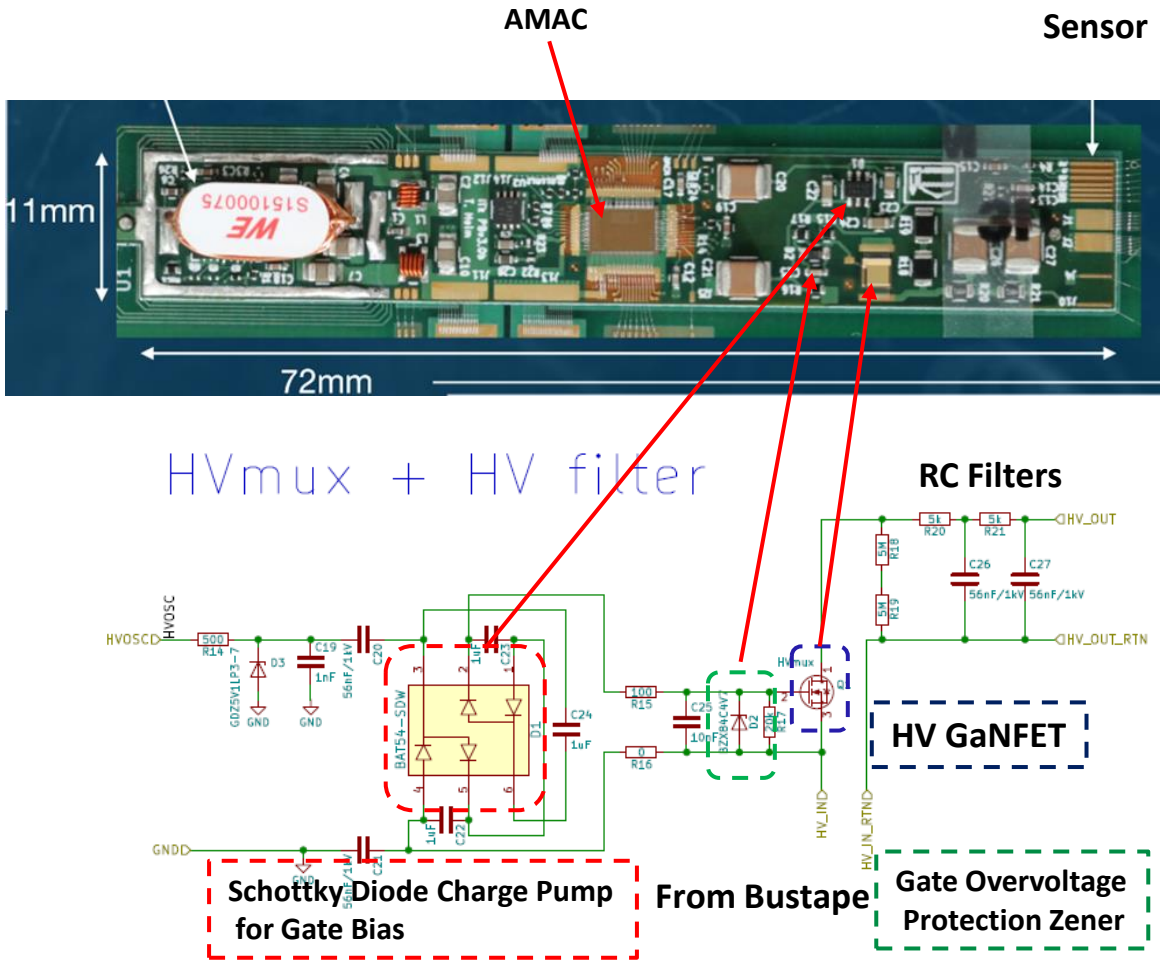


Power board v3.0b

HV biasing

- A charge pump voltage multiplier driven by AC drives the gate of a GaN FET, rated for HV
- Investigated stacked solutions demonstrated switching voltages > 1kV
- Up to 600V with the implemented ItK solution
- Baseline solution for HV bias of ItK strips

LBNL V3 PowerBoard with HV Mux



Villani, E.G., and ATLAS Collaboration. *HVMUX, a High Voltage Multiplexing for the ATLAS Tracker Upgrade*. United States: N. p., 2016.

Thank you

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Circuits and Layouts I Summary

- Hybrid and Monolithic technology pros and cons
  - From layout to device example of CMOS sensor fabrication
  - Isolation techniques
  - HV biasing