Cadence Confidential

28nm mixed-signal workshop

Alessandro Caratelli [CERN ASIC Support]
CERN - June. 2023

Monday

- Technology Overview and designer's guidelines

  Franco BANDI (CERN)

- Overview of the 28nm common design platform

  Marco ANDORNO (CERN)

- Total Ionizing Dose response of the 28nm technology

  Giulio BORGHELLO (CERN)

- Analog simulation with Explorer and Assembler in 28nm

  Helga Dornelas

  LAB SESSION

- Mixed-signal simulation analog-on-top

  Helga Dornelas

  LAB SESSION

Tuesday

- Mixed-signal simulation digital-on-top (in Xcelium)

  Helga Dornelas

  LAB SESSION

- Analog Backend VXL Best Practices

  Philippe Carriere

  LAB SESSION

- IP block characterization Abstract generation

  Philippe Carriere

  LAB SESSION

- DRC, LVS and Extraction using PVS

  Philippe Carriere

  LAB SESSION

Wednesday

- IP block characterization Timing models

  Marco Andorno

  LAB SESSION

- Digital-on-top flow introduction

  Erwan Dekhil

- Single event effects hardening in digital design

  Alessandro Caratelli

  LAB SESSION

- Timing constraints and synthesis

  Erwan Dekhil

  LAB SESSION

- Logic Equivalence Checking

  Erwan Dekhil

  LAB SESSION

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Wednesday

- IP block characterization
  Timing models

  Marco Andorno

  LAB SESSION

- Digital-on-top flow introduction

  Erwan Dekhil

- Single event effects hardening in digital design

  Alessandro Caratelli

  LAB SESSION

- Timing constraints and synthesis

  Erwan Dekhil

  LAB SESSION

- Logic Equivalence Checking

  Erwan Dekhil

  LAB SESSION

Thursday

- Block-level implementation

  Erwan Dekhil

  - Run implementation with Innovus
  - Power planning
  - Placement
  - Timing analysis
  - Synthesizing the clock tree
  - Post CTS timing analysis and optimization
  - Routing

  LAB SESSION

- Sygnoff implementation

  Erwan Dekhil

  - Post route and Signoff timing analysis
  - Signoff power analysis

  LAB SESSION

Friday

- Top-level hierarchical implementation

  Erwan Dekhil

  - floor-planning and power planning
  - Top level implementation

  LAB SESSION

- Top-level signoff analysis

  Erwan Dekhil

  - Top level signoff IR-drop analysis
  - Top level signoff STA
  - Top level export data for DRC/LVS
  - Gate-level Simulation
  - Merging top-level and block script

  LAB SESSION

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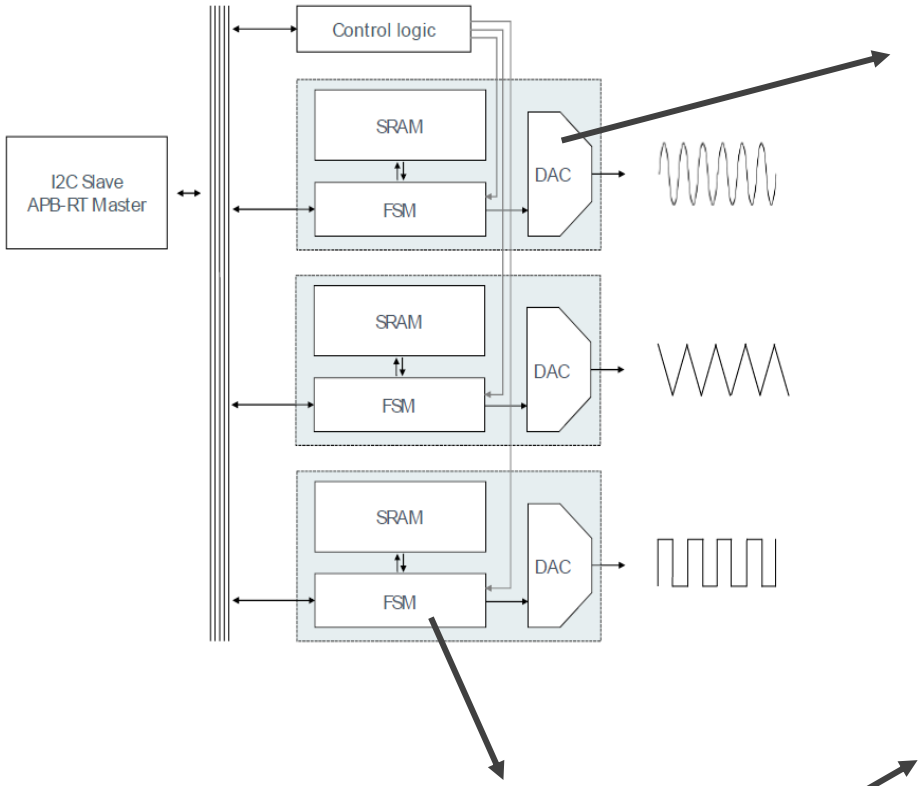
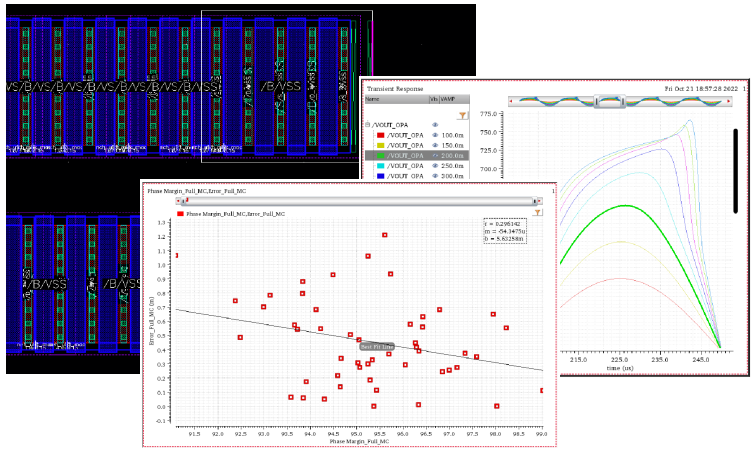
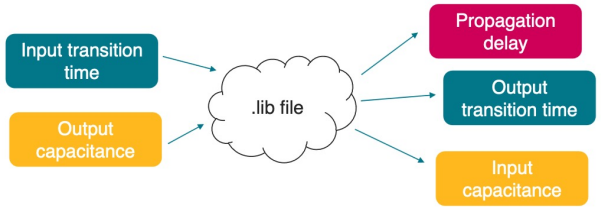
Lab sessions



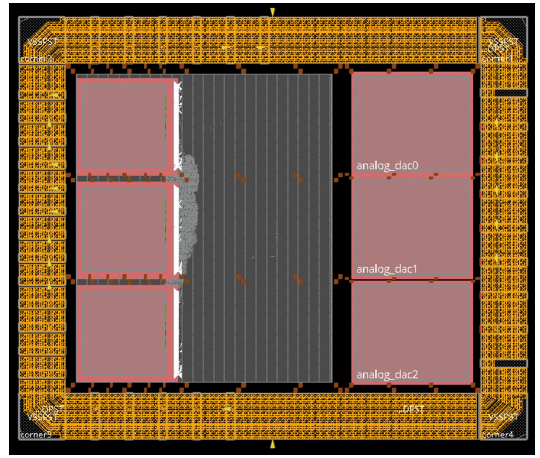
Analog and Mixed-signal design



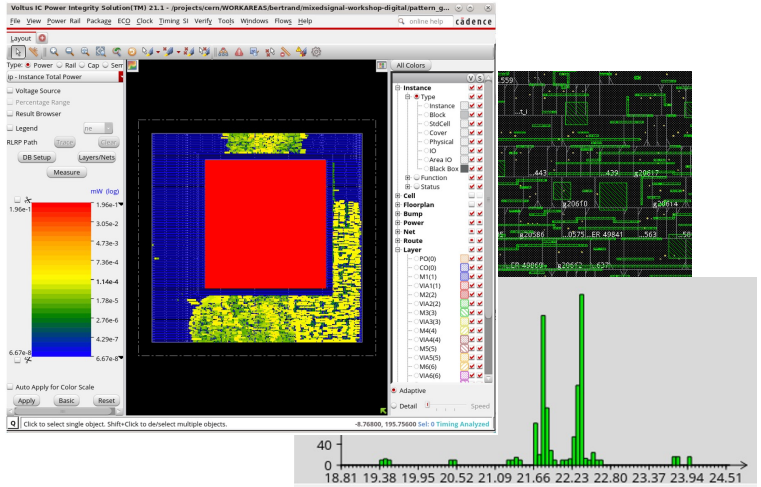
Analog IP-block characterization



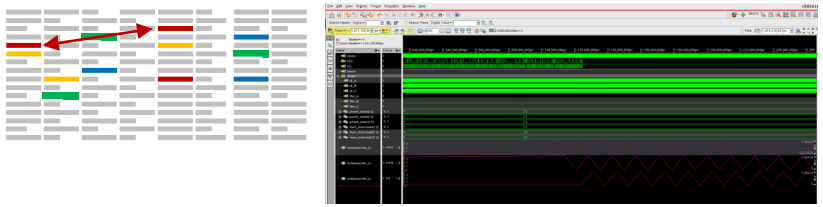
Top-level chip integration



Digital block implementation and analysis



Digital simulation and SEE hardening



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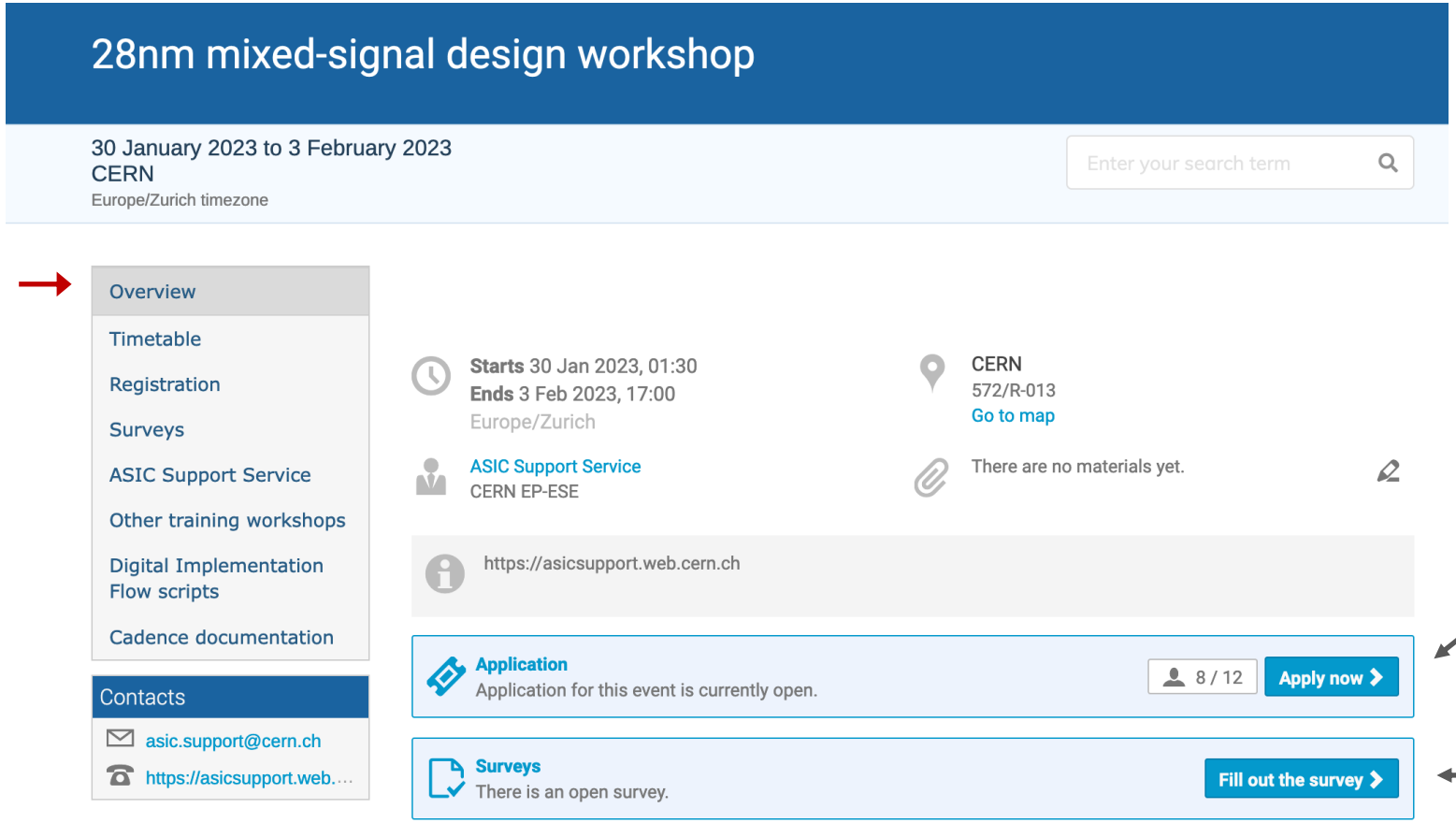
Some practical information about the workshop



REGISTRATION

To get access to the course material please register with this link

SURVEY

You are kindly invited to complete the survey at the end of the course to help us improving next session

Link to the workshop material: https://indico.cern.ch/e/28nm-workshop-1

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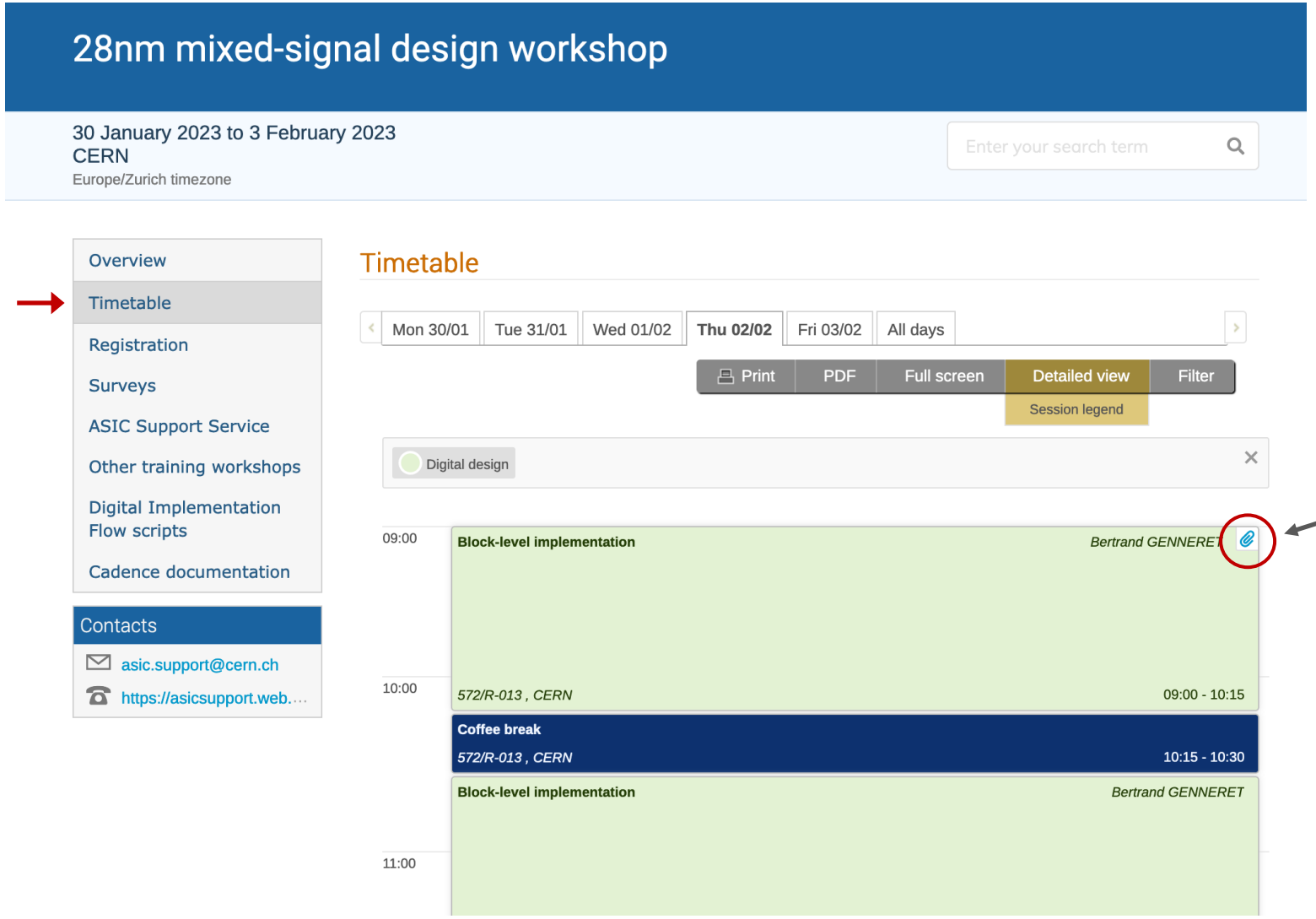

WORKSHOP MATERIAL DOWNLOAD

To download the slides and the lab instruction to follow during the course

Material download is protected by NDA

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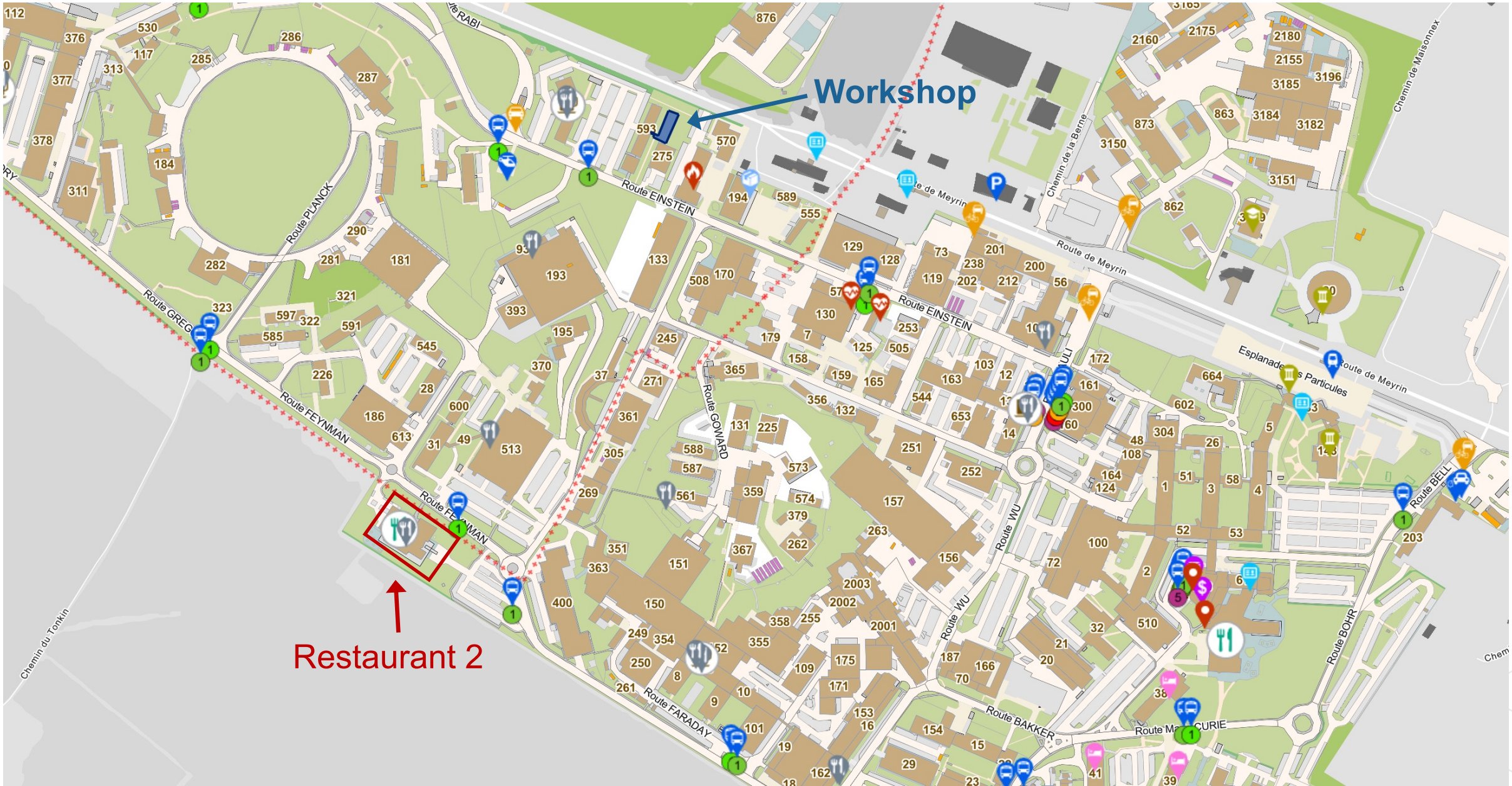
Some practical information about the workshop



Certificates

- Certificates of attendance will be distributed at the end of the course
- If you need a certificate for ECTS credits please contact asic.support@cern.ch
  - 35h training course + mini-exam ➔ usually recognized as 2 ECTS credits

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Training courses catalog

Digital-on-top hierarchical Implementation in workshop

DoT Workshop

(3 days)

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2 TIMES PER YEAR FOR THE LAST 3 YEARS

Workshop on Mixed-Signal design in 28nm process

Designing in 28nm

(5 days)

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Learn the main concepts of the analog and Mixed-Signal design in 28nm
- Learn main concepts about TIDs and SEUs tolerance design
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

NEW - FIRST SESSION IN JANNUARY 2023

System Verilog Advanced Verification Environment using UVM workshop

Verification / UVM

(3 days)

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

1 TIME PER YEAR

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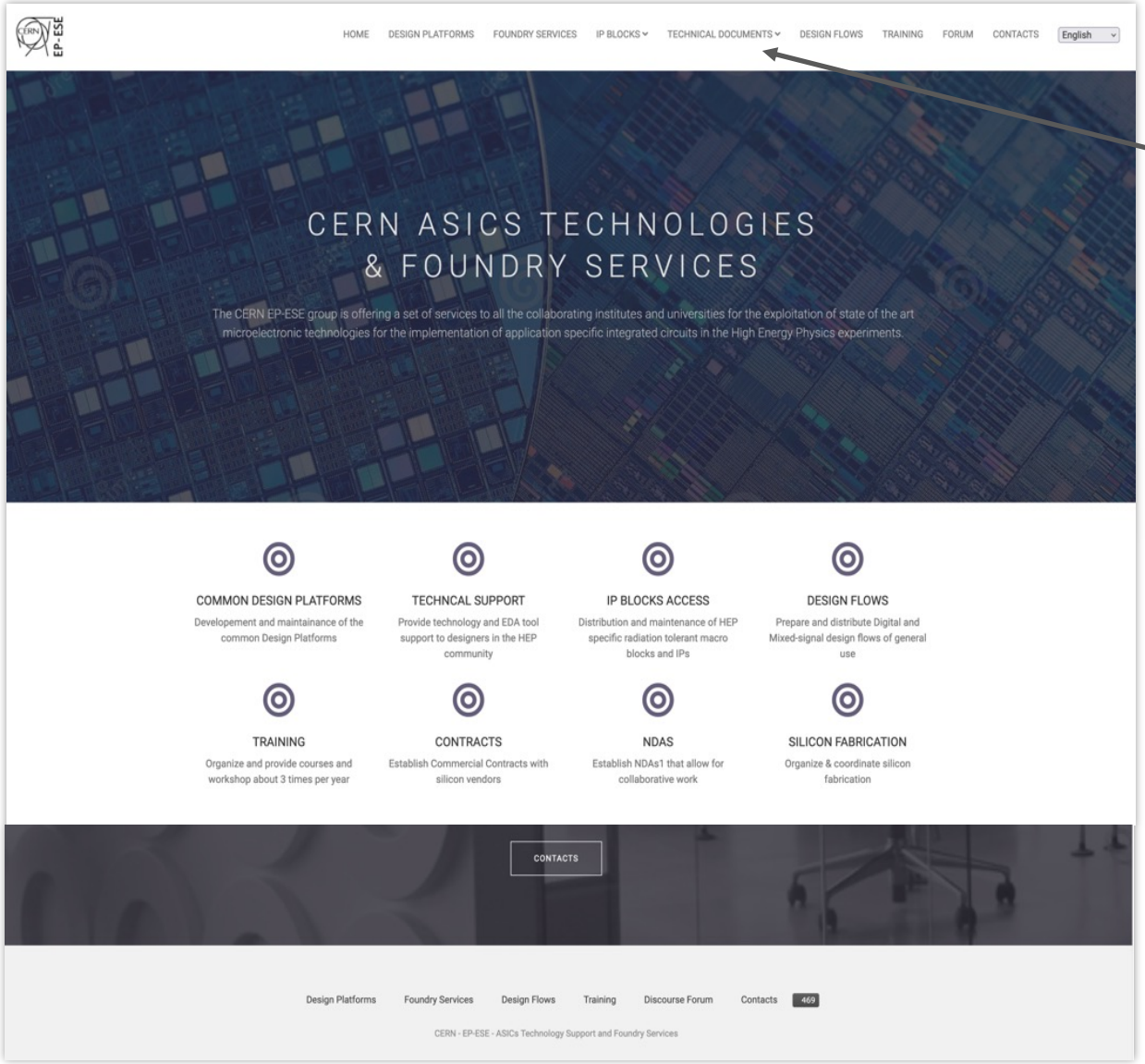
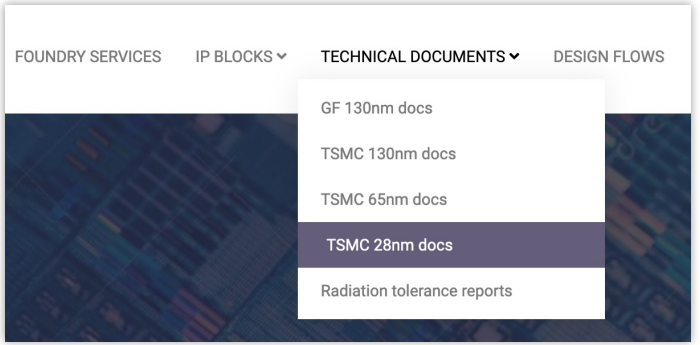
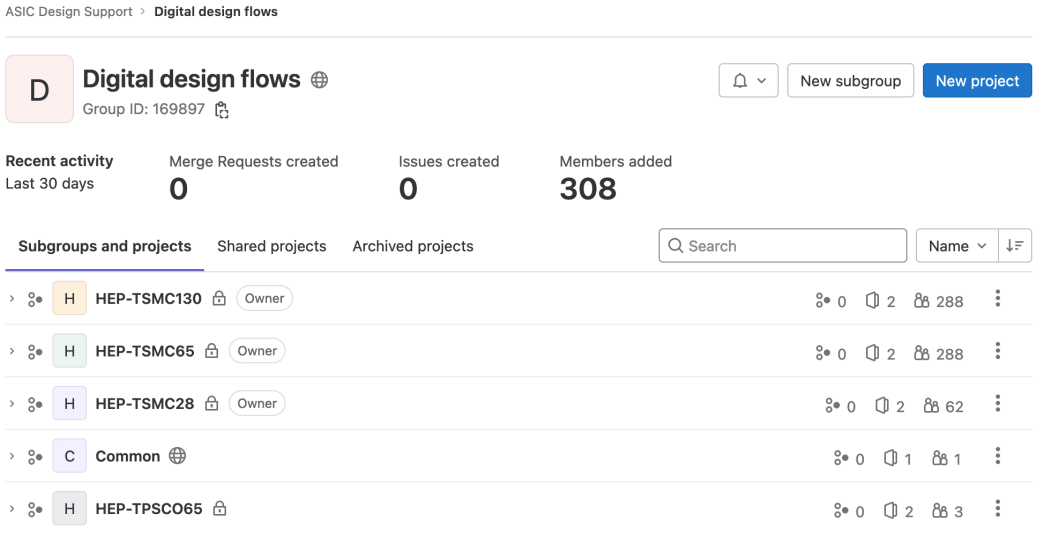
28nm Resources https://asicsupport.web.cern.ch





Digital scrips and design flows:

https://gitlab.cern.ch/asic-design-support/digital-design-flows



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28nm Resources https://asicsupport.web.cern.ch

DESIGN MANUALS AND GUIDELINES

March 2, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

In this section you can access the design manuals and PDK documentation

CONTINUE READING

LIMITED-ACCESS DOCUMENTS AND DESIGN GUIDELINES

March 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

In this section you can access the Limited Access documents and design guidelines

CONTINUE READING

CALIBRE DRC RULES

February 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service
Manuals, Foundry, Application Notes

All Calibre DRC files are in the directory: $PDK_PATH/$PDK_RELEASE/pdk/1P9M_5X1Y1Z1U_UT_AlRDL/cdsPDK /Calibre/drc For ease of updating, rule definitions and switches are kept in separate files, so that when a new rule update comes, there is no need to change the switches as well.

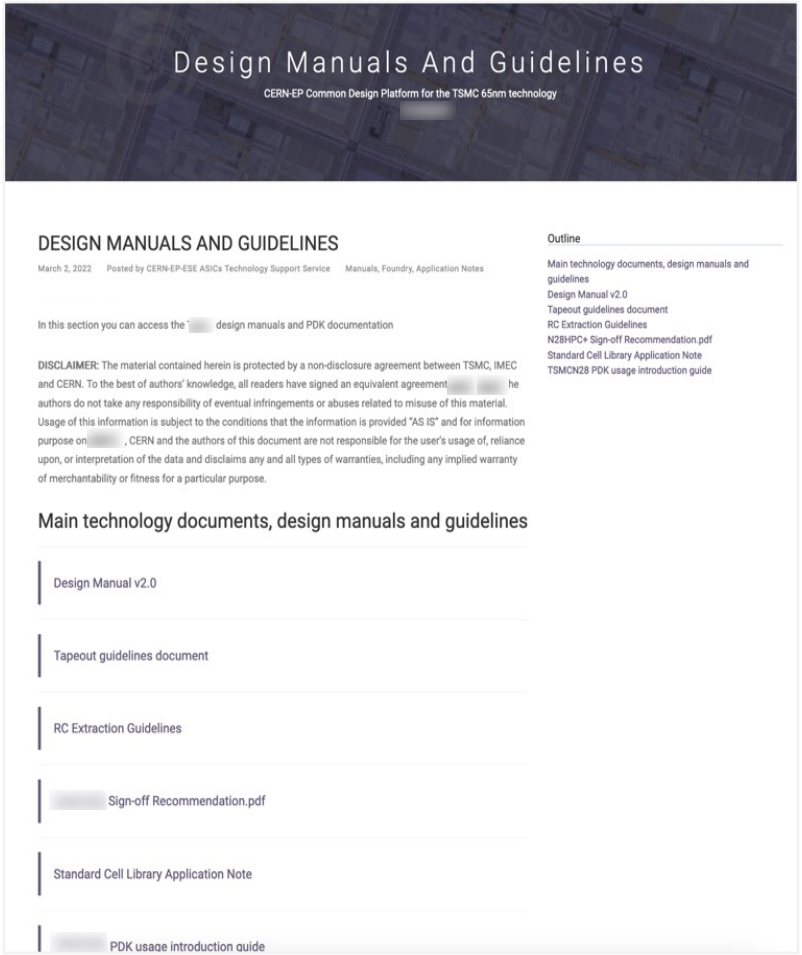
CONTINUE READING

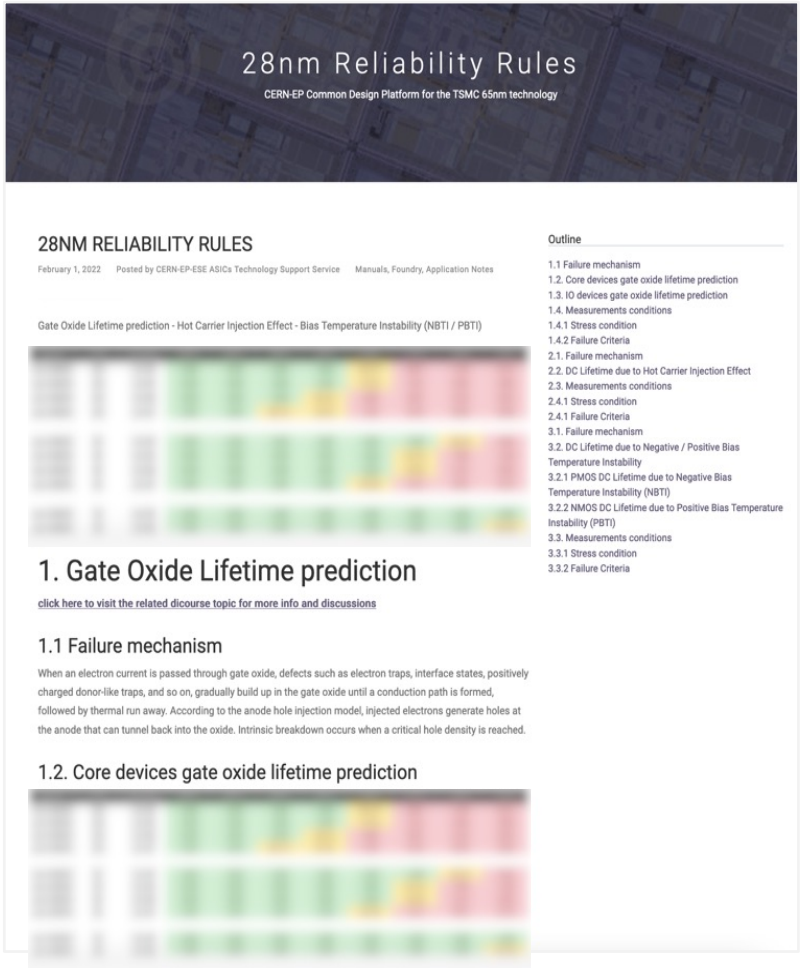
CERN MSOA DESIGN KIT ACCESS AND INSTALLATION

January 1, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service MSOA Design Kit

The HEP Common Design Platform is built by CERN EP-ESE in collaboration with Cadence around the 65nm foundry PDK to facilitate the collaborative work among the institutes, supporting the interoperability within the HEP community, avoiding incompatibilities across design teams.

CONTINUE READING





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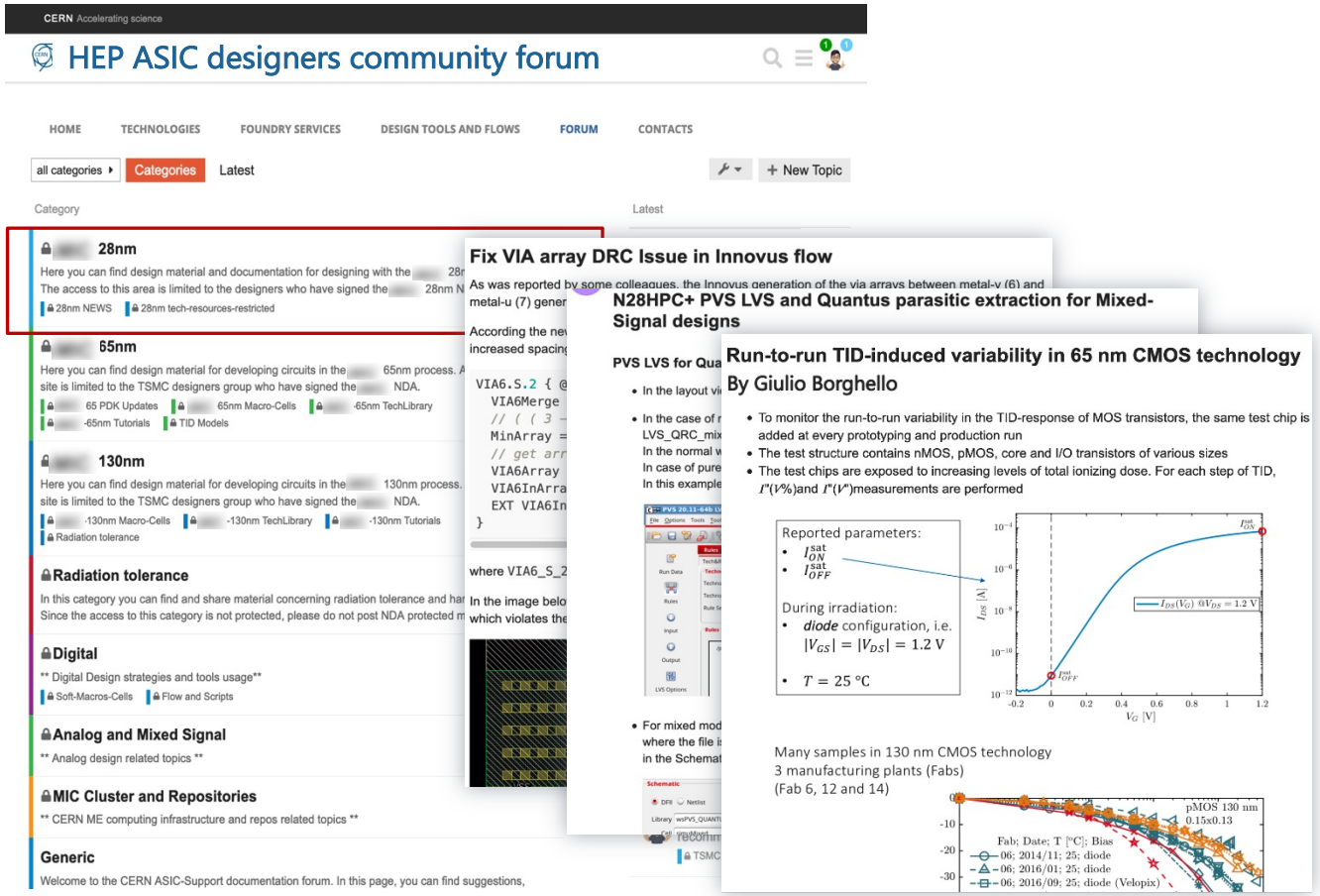
Resources

The HEP designers forum

a place where to share information and search solutions

https://asicsupport-community.web.cern.ch

- Design and EDA tools Tutorials
- Additional documentation
- Design practices suggestions
- Exchange of information
- Everybody can benefits from the findings, solutions and scripts of the others without having to deal with the same issues
- 28nm dedicated section



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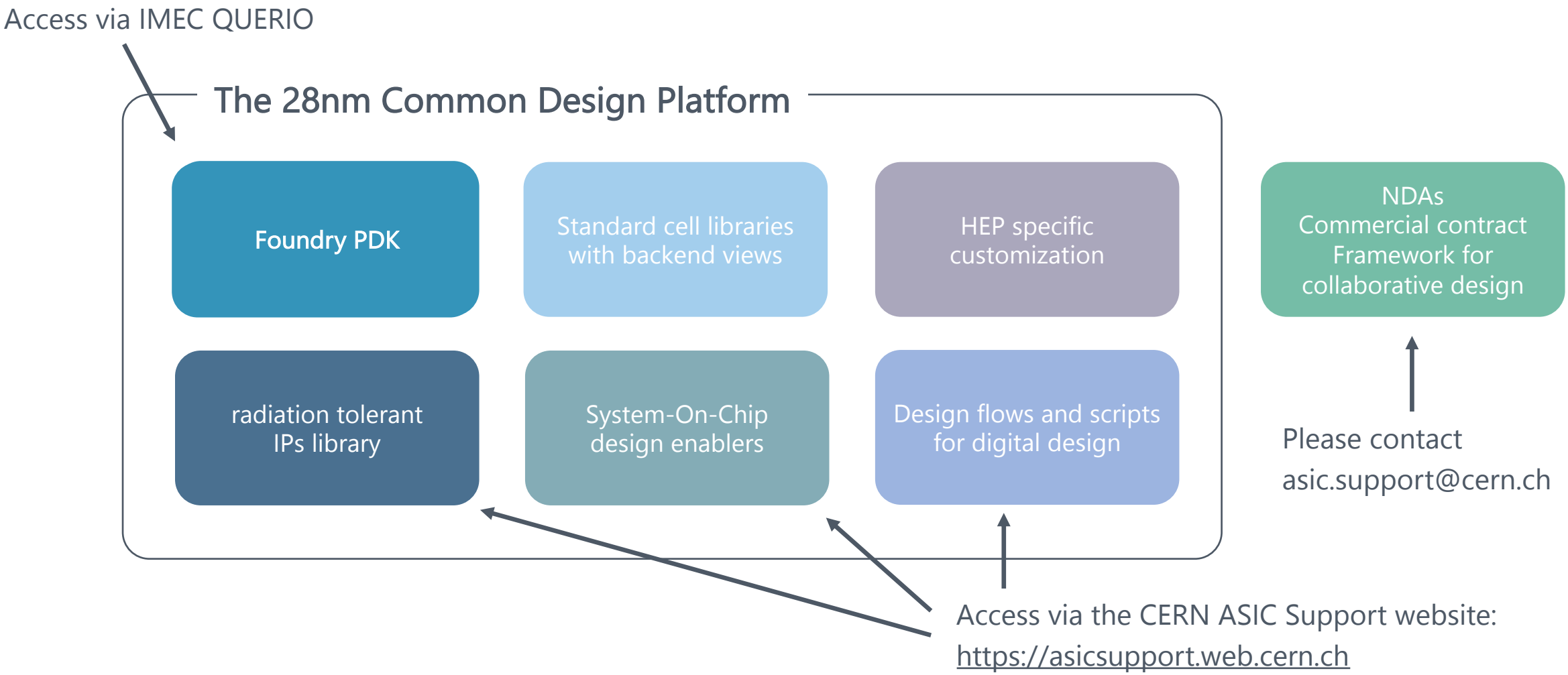
28nm HEP Common Design Platforms

An integrated solution that provides the essential instruments, blocks and experience to facilitate the ASICs collaborative design work in 28nm.



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The CERN ASIC Support Service


Promote the collaborative works and knowledge sharing


Provide support to HEP community for technology and EDA tool usage


Enhance, update and maintain the PDKs for commonly used technologies in HEP environment


Develop and distribute the Common Design Platforms for mixed-signal ASICs design


Distribution and maintenance of common macro blocks


Preparation and maintenance of design flows of general use


Organize training workshops for HEP specific

CORE TEAM: Marco Andorno, Wojciech Bialas, Alessandro Caratelli, Kostas Kloukinas

CONTACTS: asic.support@cern.ch

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The CERN Foundry Service

Establish Commercial Contracts with silicon vendors

Establish NDAs that allow for collaborative work

Organize & coordinate silicon fabrication

For silicon fabrication services (MPWs, engineering & production runs)
please contact foundry.services@cern.ch

CORE TEAM: Kostas Kloukinas, Maxence Ledoux, Cinzia Pinzoni

CONTACTS: foundry.services@cern.ch

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Technical support

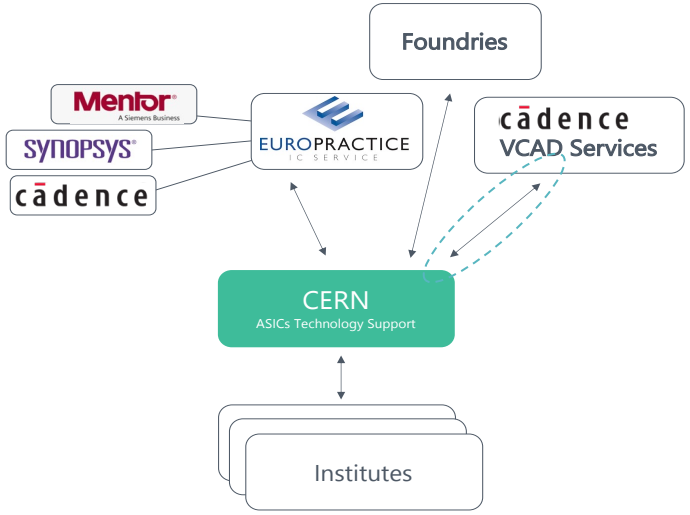
You can contact asic.support@cern.ch
for requests related to:

- Support for the **EDA tools** usage, **Design Flows** and the **Design Kits**
- Support **for design specific** issues
- **Distribution of shared IP blocks**
  (and assistance for design integration).
- Administrative requests (process of **signing NDAs**, **technology information** access, **PDK requests**).

If you are in need of specific design assistance and implementation or verification tasks, please contact instead the chips.service@cern.ch

If needed for solving your issue, we can as well:

- put you **in contact with CERN designers** with experience in the field
- Involve **CADENCE VCAD Service** with which we have a support contract in place



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