DAQ system for superconducting Magnets

“Lessons learned after 14 years in SM18”

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BE-CEM-MTA CERN

In this presentation

Who are we?

History of SC magnet tests at CERN

The RADE framework

Gathering specification of the DAQ system to design

Signals and hardware considerations

Data Storage and analysis

Software engineering

CEM – Controls Electronics & Mechatronics

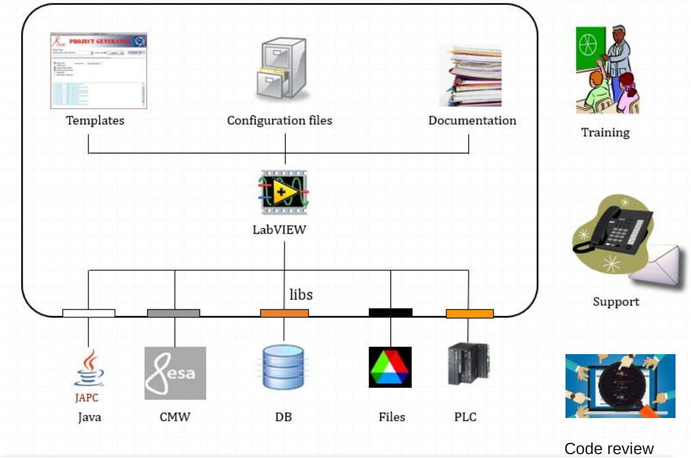
Group Leader: Alessandro Masi

CEM
Controls Electronics & Mechatronics
GL: A. Masi
DGL: J. Serrano

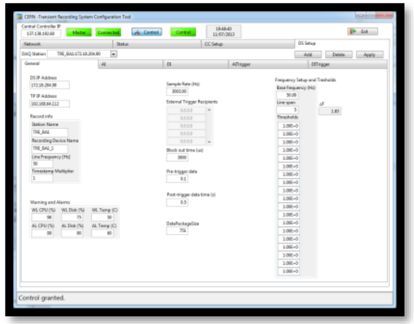
- **EPR** – Electronics Prod. & Radiation Tolerance – SL: S. Danzeca
- **EDL** – Electronics Design & Low level software – SL: J. Serrano
- **IN** – Infrastructure – SL: I. Kozsar
- **MRO** – Mechatronics, Robotics & Operation – SL: M. Di Castro
- **MTA** – Measurement, Test & Analysis – SL: O. Andreassen

SM18 superconducting magnet test stands

Responsible for the CERN-wide support for all tests & measurement systems based on LabVIEW and a selected set of commercial off-the-shelf products.

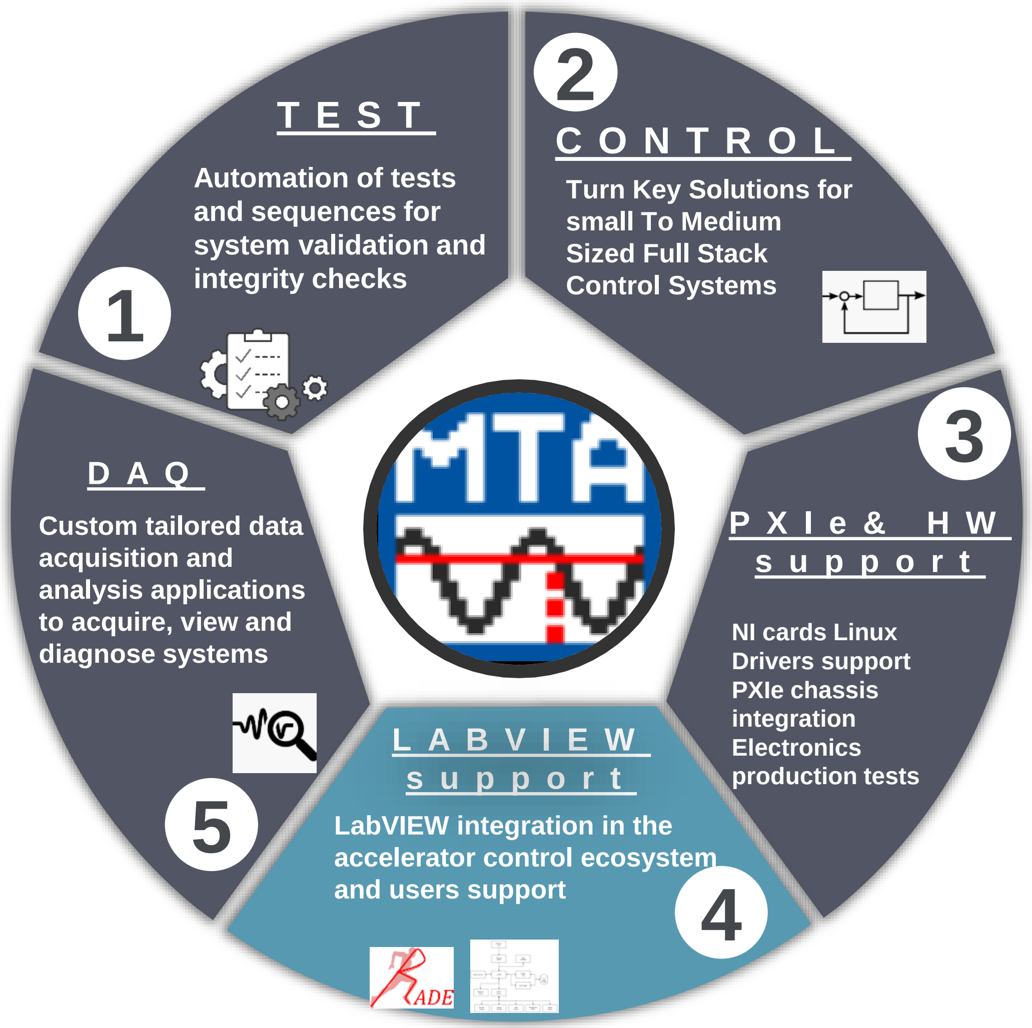


CERN LabVIEW support



Oscilloperturbography (EN-EL)

The MTA Section



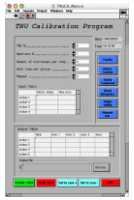
The MTA section develops and provides CERN-wide support for all test & measurement systems based on a selected set of commercial off-the-shelf products (e.g. NI, Inca)

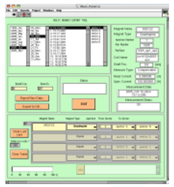
We also provide custom code reviews, teaching of best practices and aid in development and implementation for more than 600 users at CERN

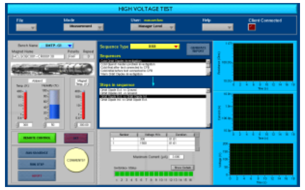
How it started?

- Measurement Test & Analysis (MTA) team started at CERN in early 90
  - Collaboration with SC magnet design & testing team
  - DVP of a control application to power LHC magnet prototypes
- SM18 test hall: construction of test benches for the LHC dipole prototypes (1992-1996)
- Several Apps to control a wide range of testing equipment
  - … and preparation for the magnet series measurements
- SM18 converted into a magnets test factory (2004-2007)
  - Existing measurements & DAQ systems remotely controlled
  - SW layers to orchestrate the magnet tests

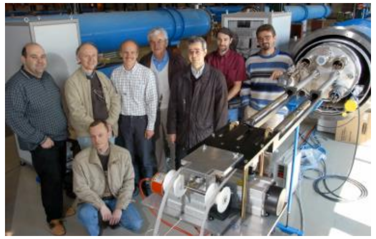
Fig. 7. On 14 April 1994 the first 10 m LHC dipole prototype from INFN was successfully powered at CERN for the first time. This magnet is now operating in the CAST experiment at CERN.

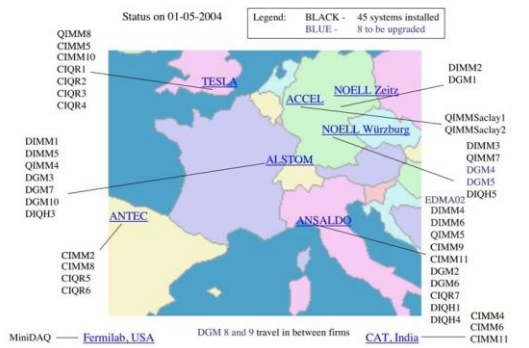






How it started?





- 45 Measurement systems developed & deployed in USA, Europe & India
    - Collaboration with several teams at CERN
    - Systems installed, used and maintained in the magnet assembly firms
    - > 1200 Dipoles, 400 Quadrupoles and 6000 Correctors tested in industry at warm temperature
    - Then tests executed at cold in SM18 on the final magnet assemblies

- From 2008 to now …
    - SM18 adapted to the HL-LHC R&D and testing campaign
    - Tools upgraded and adapted to the current needs and technologies
    - FAIR project: dedicated measurement systems for the magnet series tests
    - IT-String project: new tools to execute some of the tests and to analyze results

The challenge

- 10.000+ Magnets
- 1750 Circuits
- 13000+ Tests

The challenge

Rapid Application Development Environment

Specifying requirements

"Getting to know your user"

Project
- Short / long term usage
- Support / long term maintenance
- Reliability / Safety
- Budget
- Deadlines

Hardware Architecture
- Local / distributed signal sources
- Homogenous / mixed signal types
- New system / integration into existing
- Channel count / density
- Single system / duplication expected
- Modular platform

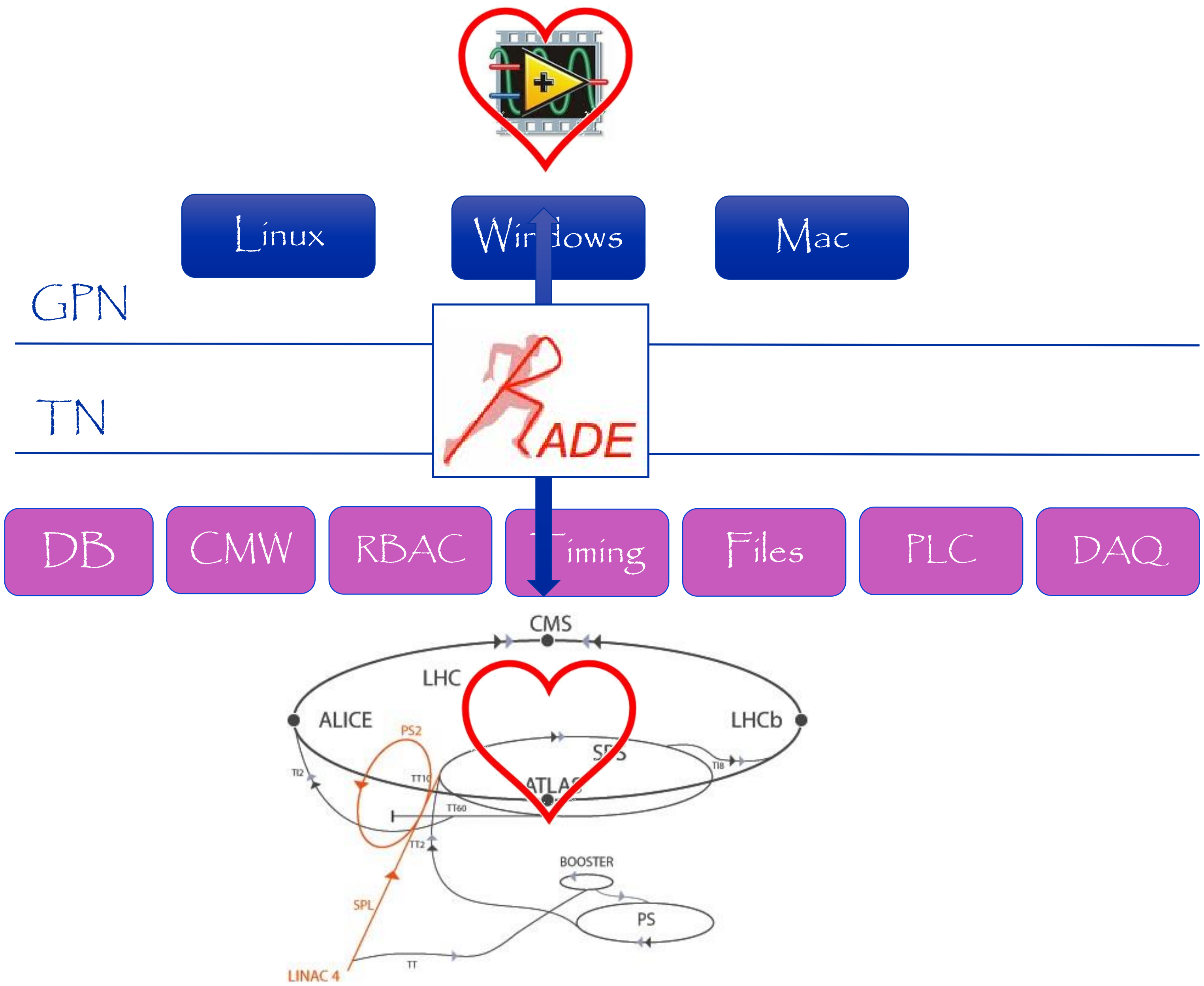
Software
- Availability of HW drivers
- Expandability
- OS & language
- Data processing
- Storage volume
- Data analysis
- GUI

Signals
- Type of signals (analog, digital, mixed)
- Ground reference mode (DIFF, RSE, NRSE)
- Max / Min ranges
- Amplification
- Noise filtering

Time & Frequency
- Sampling speed
- Bandwidth
- Acquisition duration
- Triggers
- Triggers frequency

Precision
- ADC resolution
- ENOB
- Offset

… most important … discuss with the future users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Timing
Files
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CMS
LHC
ALICE
LHCb
PS2
SPS
ATLAS
TT60
BOOSTER
PS
SPL
LINAC 4
TT

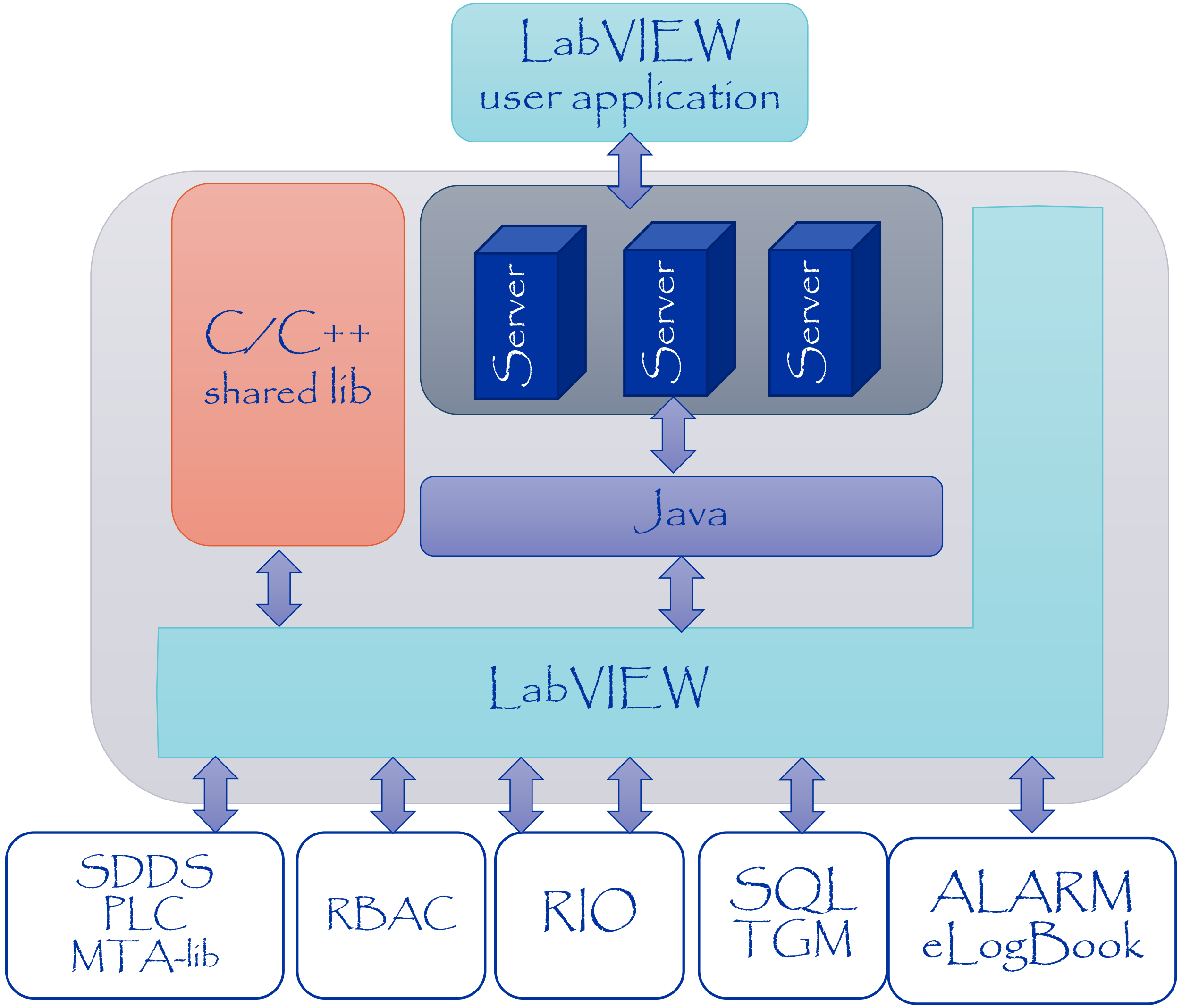
Fulfilling requirements

- Fast programming
- Rapid learning curve
- Drag and drop GUI development
- Wide range of analysis libraries
- Light/independent environment
- Integration with CERN infrastructures

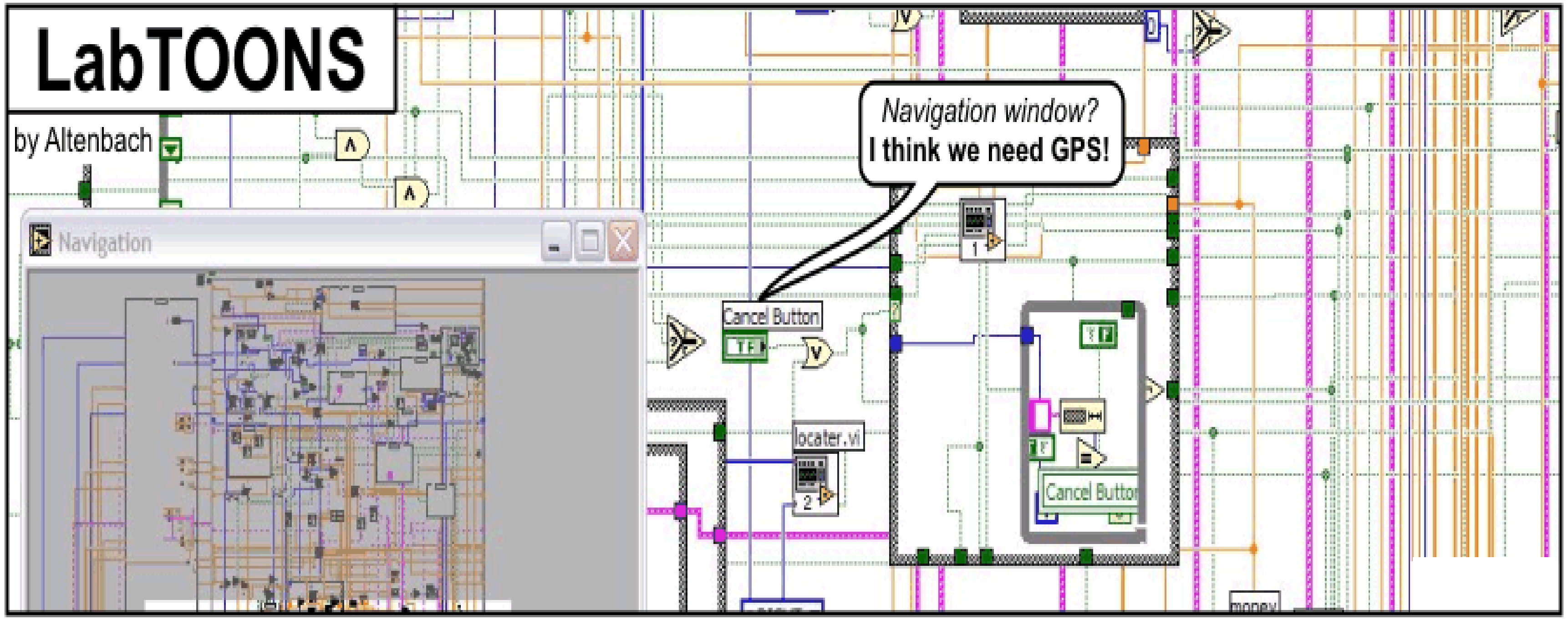
LabVIEW

RADE

Fulfilling requirements



Fulfilling requirements – copying with large applications



Fulfilling requirements

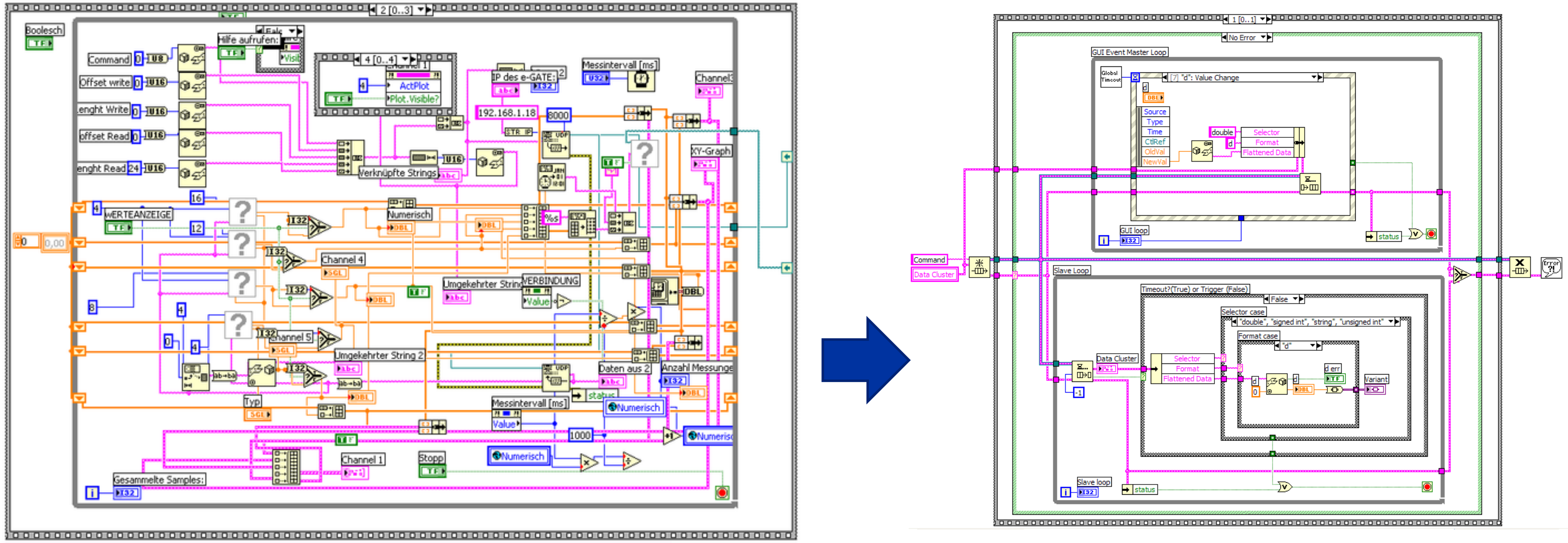
- Fast programming
- Rapid learning curve
- Drag and drop GUI development
- Wide range of analysis libraries
- Light/independent environment
- Integration with CERN infrastructures
- Source control and distribution
- Instance generation
- Templates and documentation
- Automated tests and builds

LabVIEW

RADE

RADE Concept – design

- Design patterns and templates
- LabVIEW Guides: https://readthedocs.web.cern.ch/x/igJV
- Code reviews: make maintainable and performant



RADE Concept - hardware

Hardware

- PXI
- CompactRIO
- DAQ

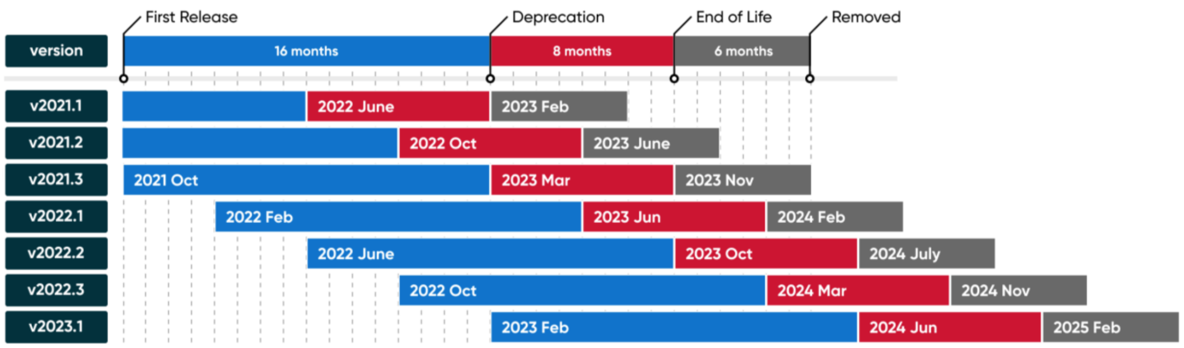
&

Software

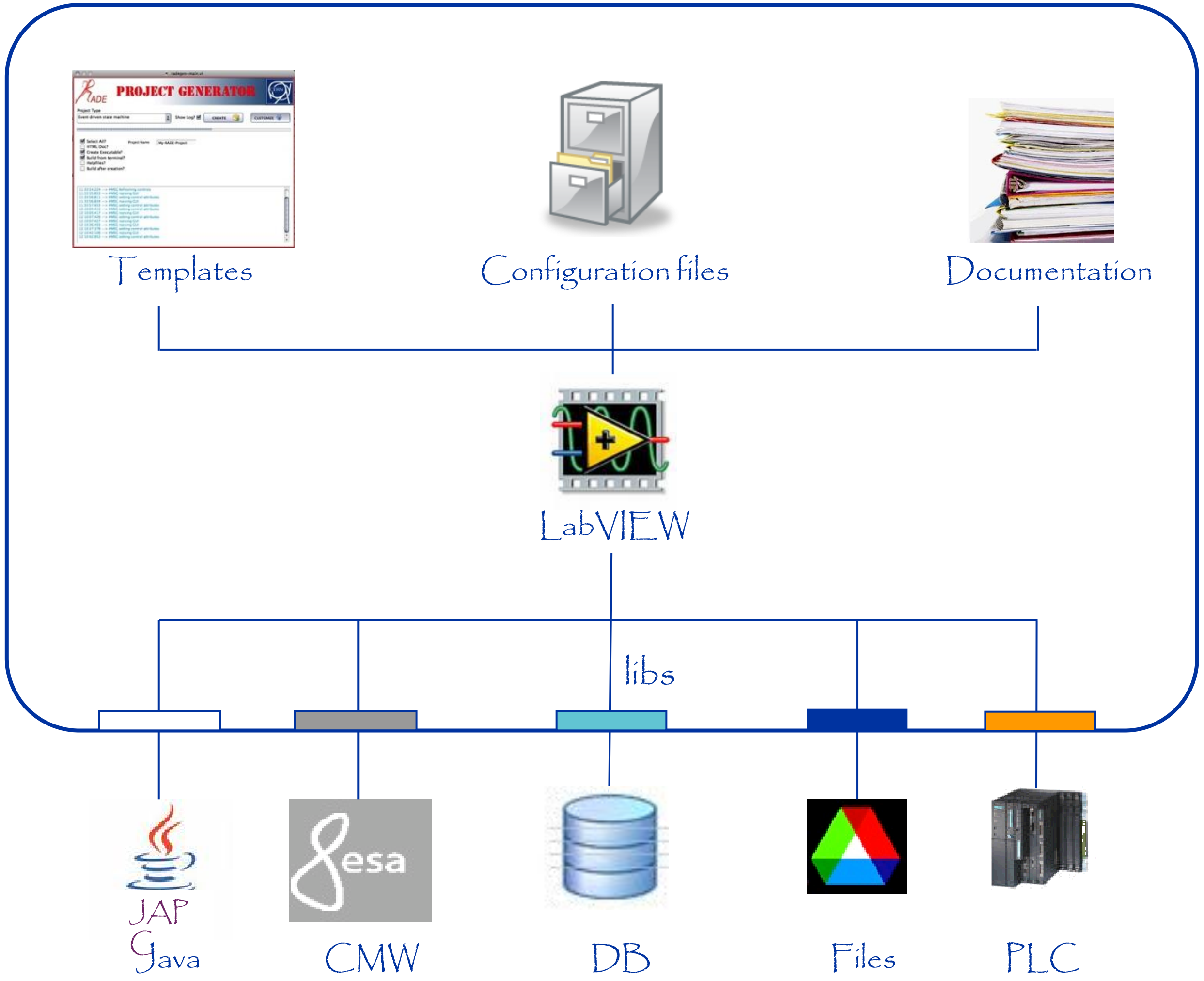
- LabVIEW
- TestStand
- DIAdem
- and other NI products

RADE Concept – long-term support

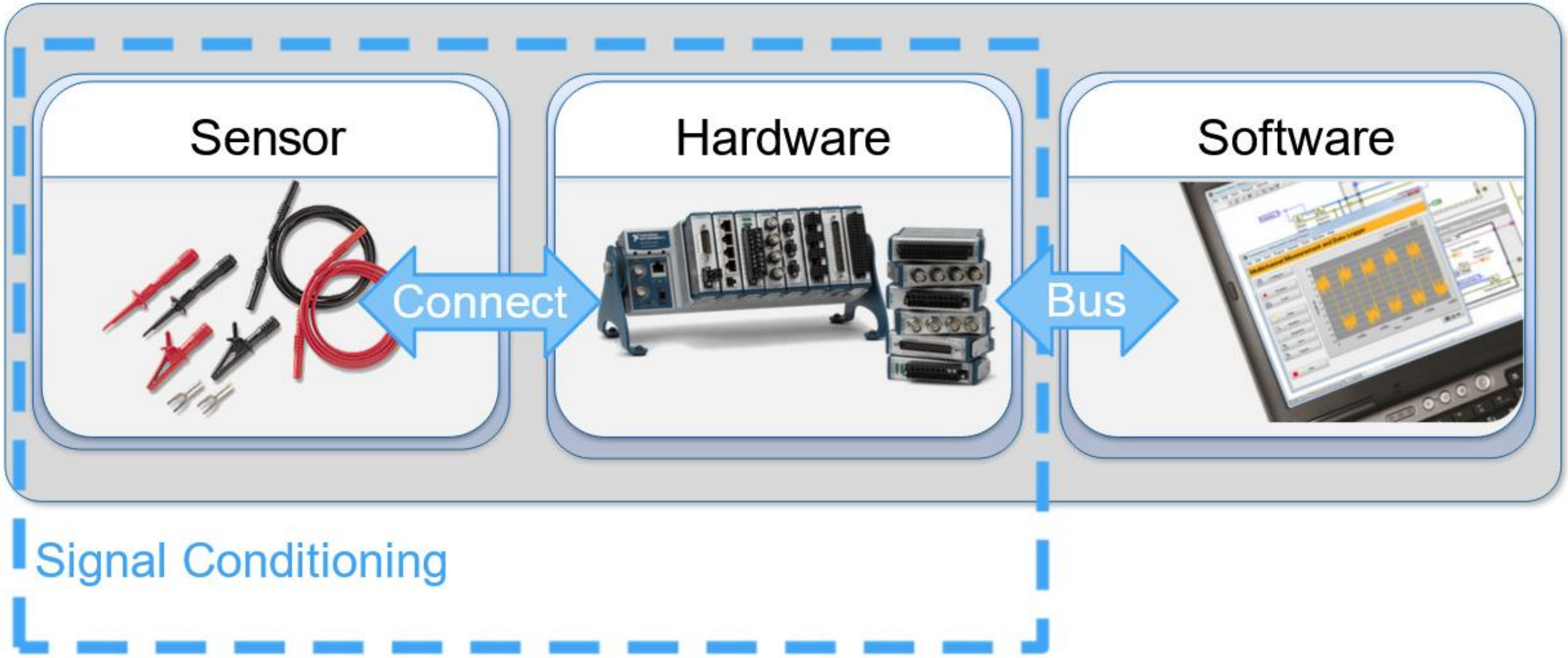
- Use modular HW architecture (upgrade components … not the full system)
- Keep spare parts for the critical pieces (power supplies, specific module, …)
- Design your system with modularity, expandability and maintainability in mind
- Use standard communication protocol (new ≠ best)
- Build your systems with exchangeable bricks
- Clearly separate functions (CPU, DAQ, storage, analysis, logging, monitoring, …)
- Document your systems
- Calibrate your measurement systems
- Keep track of industry & IT trends (HW, communication, analysis tools, cloud services, …)
- Upgrade your bricks before obsolescence



RADE Concept - framework



Components of the DAQ systems



NI.com : Measurement Fundamentals - Measuring Voltage or Current (Analog Input)

Physical requirements

Rule of Thumb #0: use rules of thumb wisely

Impedance and Matching

Impedance (Z) is opposition to a flow of energy; *impedance is often a function of (non-linear) frequency*

Matching ensures maximum power transfer i.e. $\mathbf{Z_{Load} = Z_{Characteristic} = Z_{Source}}$

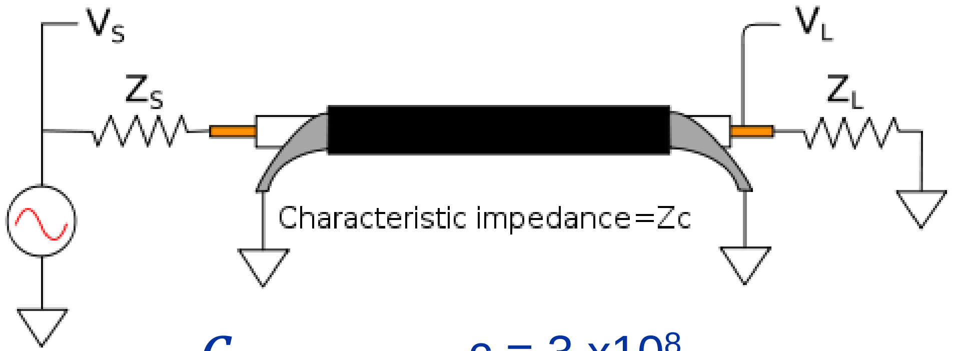
Cable length is usually defined in terms of wavelength or propagation time

If cable is 'long' then use a transmission line

- 'Short' cables are less than λ/10 !

E.g. 100 MHz signal has λ = 1.95m in RG58

- Use proper co-ax if cable length > 20 cm



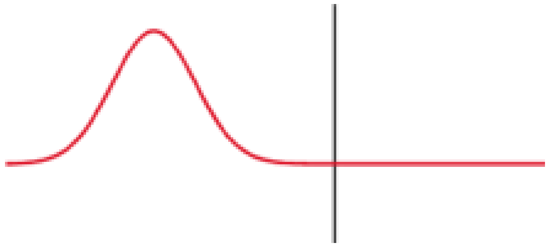
$$\lambda = \frac{c}{f} * VF$$

c = 3 x10^8
f = frequency
VF is velocity factor

VF usually between 0.60 and 0.83
E.g. RG58 VF = 0.65

RULE OF THUMB: Signals travel at 5 ns/m in co-ax

Mismatching and Discontinuities



Mismatches cause reflections of the signal

- Open circuit – reflection is in phase (0°)
- Short circuit – reflection 180°

Discontinuities (change of impedance) cause partial reflections

Some items of RF equipment do not like open or short circuit loads – always check before output is enabled!

Warning: don’t step on cables – a crushed cable will have a discontinuity!

Decibels

$$N(dB) = 10\log\frac{P}{P_0} = 20\ \log\frac{A}{A_0}$$

where P and P_0 are power quantities, and A and A_0 are amplitudes (volts)

N (dB)	Power ratio	Amplitude ratio
-20	0.01	0.1
-10	0.1	0.32
-6	0.25	0.5
-3	0.5	0.71
0	1	1
+3	2	1.41
+6	4	2
+10	10	3.16
+20	100	10
+30	1000	31.6

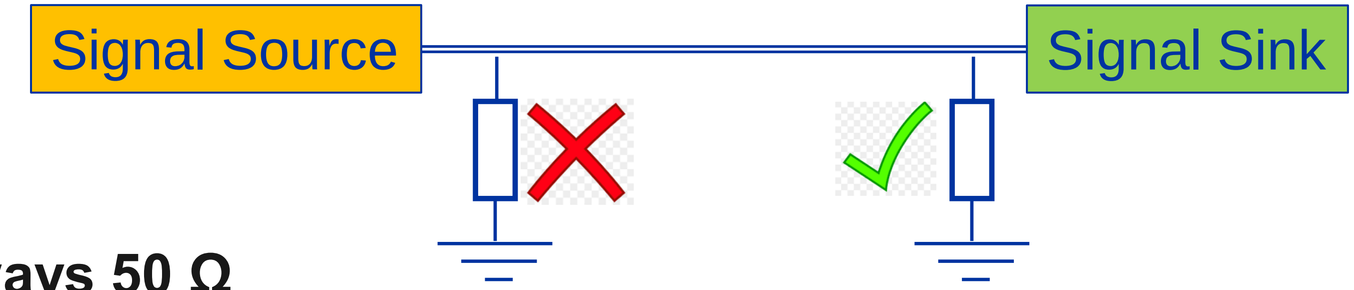
Gain, attenuation, loss etc. usually expressed in dB, often for a particular bandwidth or at a spot frequency

Q1 What is the output if a 50 mV_{rms} signal is input to an amplifier of gain 20 dB?

Q2 What value of attenuation will reduce a 4 mW signal to 1 mW?

* RF signals (above 10s MHz) usually expressed in dBm, where P_0 is 1 mW (into a 50 Ω load)

Co-axial Cables



Signal cables in the lab are almost always 50 Ω

Signal attenuation is due to resistive losses, expressed in dB/unit-length at one frequency e.g. RG58: 4.9 dB/30.5 m at 100 MHz

Signals above a few MHz require impedance-controlled connections, usually a co-axial cable. Common 50 Ω cable types are:

- RG58: good for 100s MHz; 6.3 mm diameter; loss 11.2 dB/30.5 m @ 400 MHz
- RG174: up to 100 MHz; 3.2 mm diameter; loss 26.0 dB/30.5 m @ 400 MHz
- RG213: good for low GHz; 10 mm diameter; loss 4.8 dB/30.5 m @ 400 MHz

Termination (or load, a 50 Ω resistor to ground) is often done within the equipment itself. If not, terminate as close to sink as possible

Splitting a HF signal using a T-splitter

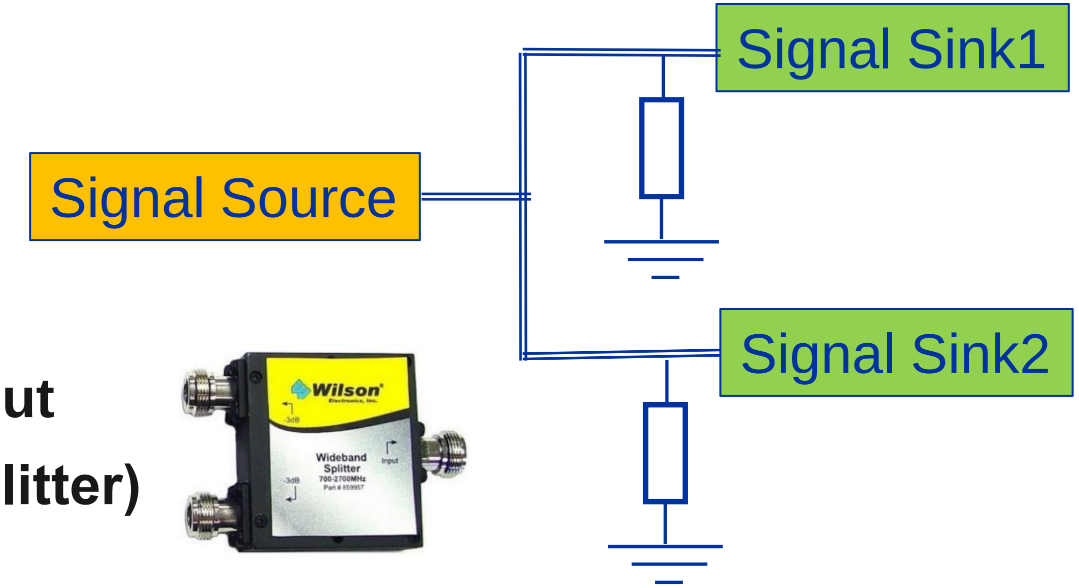
Splitting the signal can cause problems, even if terminating ‘correctly’

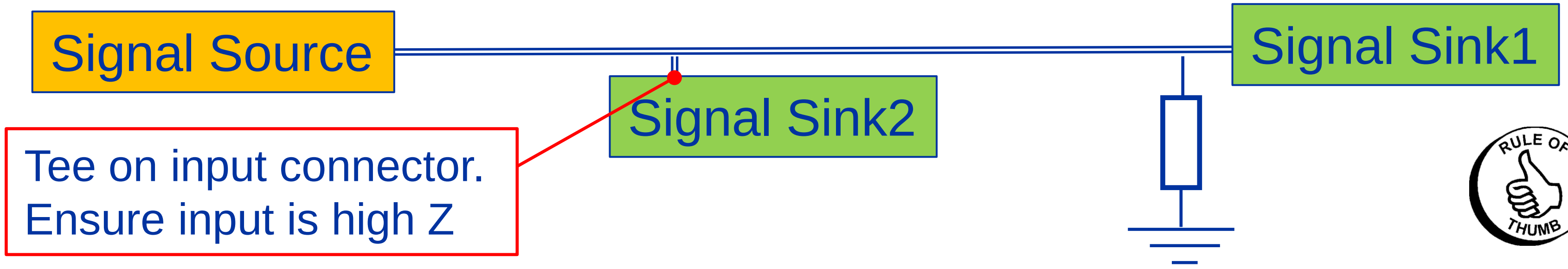
Why?

Source ‘sees’ two loads in parallel

Total load is 50║50 = 25 Ω **mismatch!**

If splitting is required, then do the following, but not at high frequency (or use a proper 50 Ω splitter)



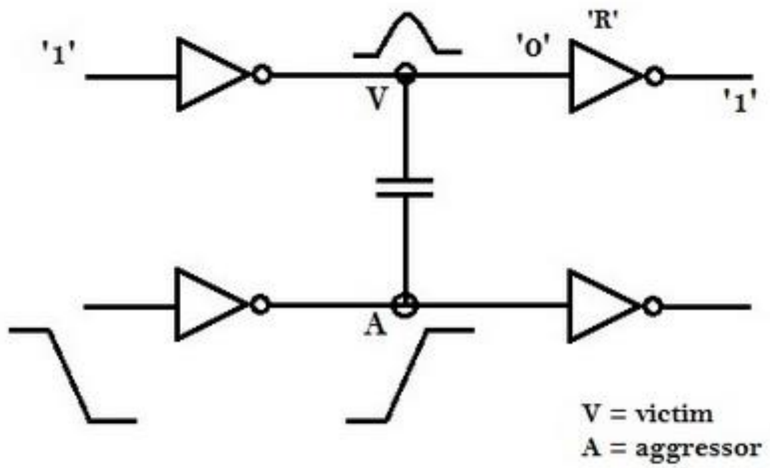


Don’t split HF signals with a T-splitter

Crosstalk

A signal transmitted on one circuit induces an (undesired) signal on another circuit

Caused by the electric or magnetic fields of a changing current



Capacitive crosstalk – aggressor causes error in victim circuit

Crosstalk can be minimized by:

- Avoiding parallel runs of cable
- Increasing distance between cables ($E \propto {}^{1}/_{r^2}$)
- Separating large current-carrying wires from signal cables
- Cross cables at 90° ($Xtalk \propto \cos\theta$)

Signal Bandwidth

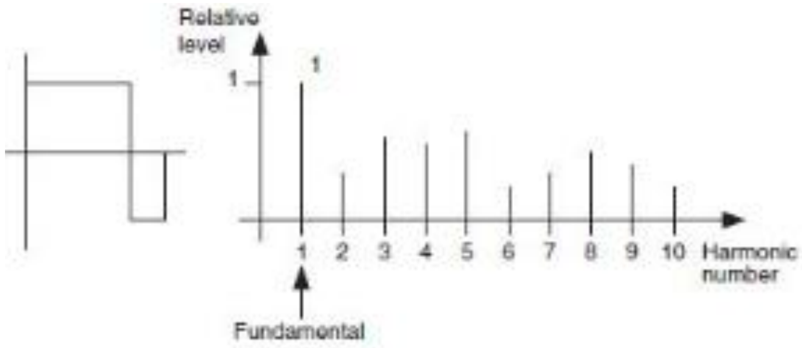
RULE OF THUMB: $BW\ (GHz) = 0.35/t_{rise}\ (ns)$

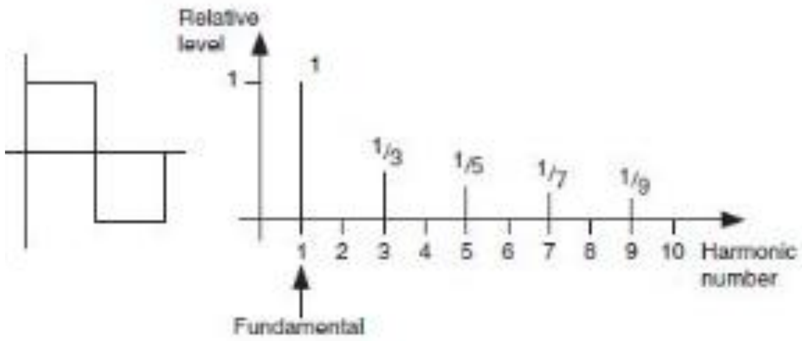
A sine wave is a pure frequency

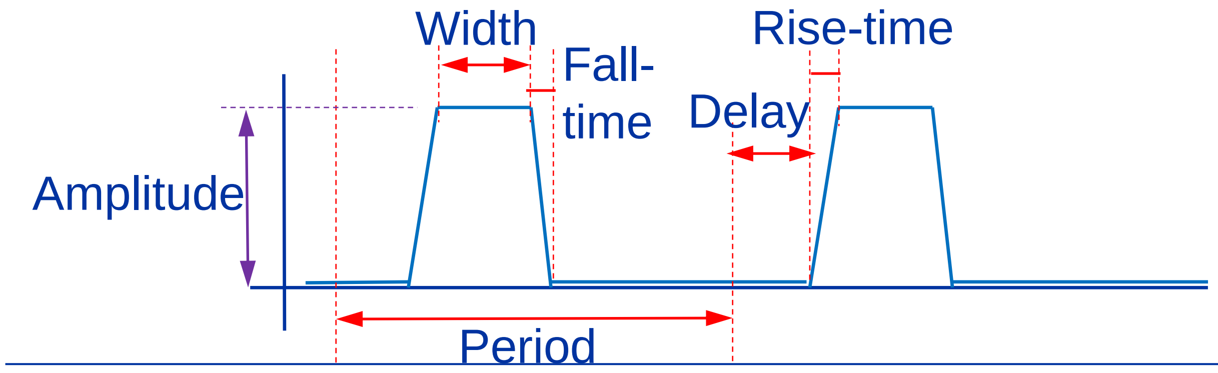
A square wave can be represented by a Fourier series of odd harmonics, with a rise-time set by the highest harmonic used

Pulse spectra are similar

- A fast rise-time implies higher frequency content so ensure cables/equipment have sufficient bandwidth to maintain it



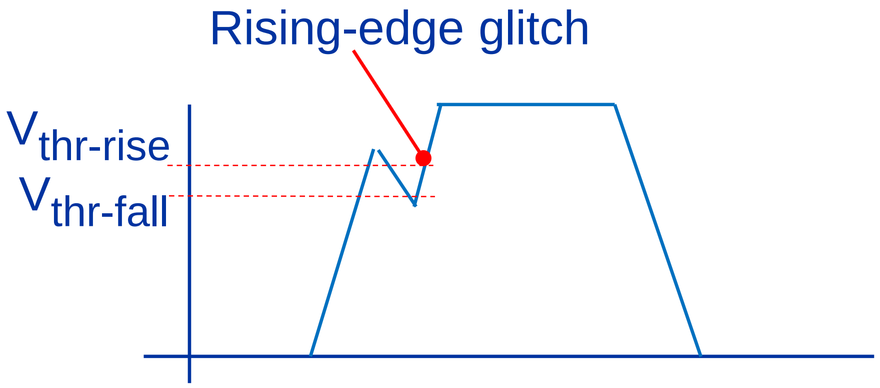




Triggering

Digital triggers are either edge- or level-defined

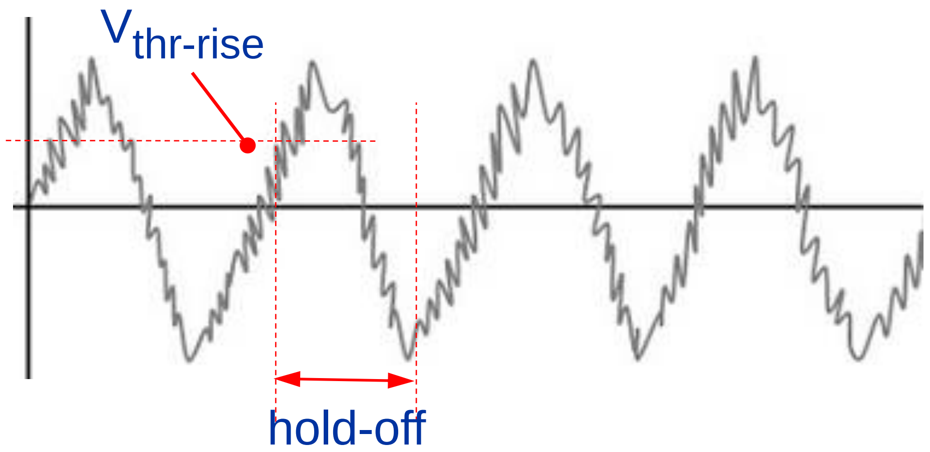
- Edges are equivalent to event-based triggers
- Level-based triggers require polling (clock)



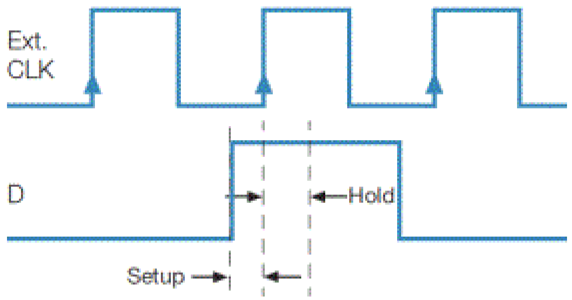
Ensure the trigger edge has no glitches

- May be counted as multiple edges!
- How can it occur? Z mismatch….

- Analog triggering can often suffer from noise, making the trigger-point unreliable
  - Use sufficient hysteresis (rising trigger level is greater than falling trigger level)
  - Often used in non-periodic systems
  - Can use 'hold-off' time to slow trigger rate



Trigger Problems



Avoid triggering when signal of interest is changing

- Ensure setup and hold times are met (few ns)

Skew is the time difference between two events that would ideally occur at the same time

- If distributing triggers, clocks and/or signals check cable propagation time

Solutions – measure with scope, adjust delay (cable or source)

- Its often easier to delay several signals (with extra cable) than to advance one signal

Signal Acquisition

Analogue signal coupling is either AC or DC

- DC operates from 0 Hz to ….
- AC operates from some 100s Hz or kHz, depending upon equipment
  - Usually, no 50Ω load when using AC coupling on scope and DAQ cards

If using AC-coupled mode, ensure DC level is within equipment limits

At high frequency (RF) coupling is often be done by transformer (lowest frequency is usually 100s kHz to MHz)

Digital signals may be isolated using opto-electronics, particularly when attached to HV equipment

Ground Loops

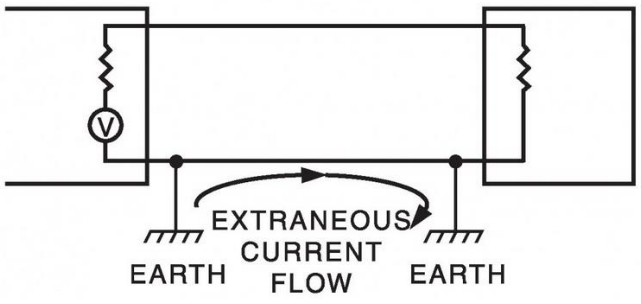
Definition: The interconnection of electrical devices that results in there being multiple paths to ground, so a closed conductive loop is formed

Electrical power wiring creates stray magnetic fields that induce a current in the ground loop (magnetic induction)

- The current causes a voltage drop across the loop, which is added to the input
- Most ground loops will pick up 50 Hz mains 'hum'

Solutions to ground loop problems

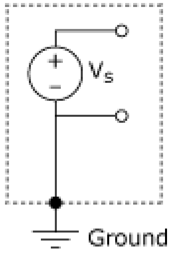
- Break the ground loop – disconnect the signal shield at one end.
- Ferrites can reduce 10s kHz noise (SMPSUs), by blocking current from travelling on the cable shield
- Use single-point (star) grounding
- Use differential signal measurements
- Use transformer or optical isolation
- DO NOT REMOVE THE EARTH-PIN OR EARTH-WIRE FROM EQUIPMENT

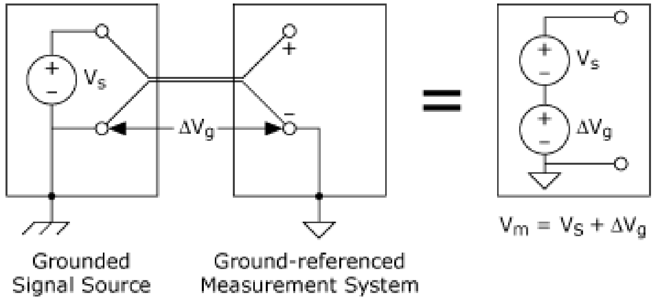


Analogue Signal Connection

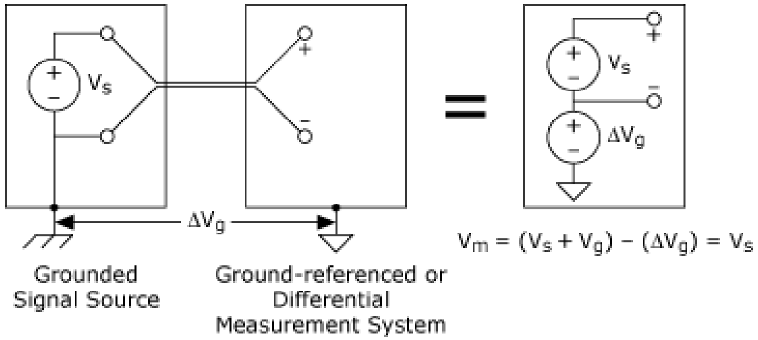
Two general categories of signal source: grounded and ungrounded (floating)

Grounded source





- Single-ended (SE) measurement
- Potential difference (ΔV_g) between source and measurement grounds adds to measurement uncertainty
- Can be several mV, often at mains freq (50 Hz)



- Non-referenced single-ended (NRSE) measurement
- No ground loop, so only measures signal of interest
- Most DAQ cards have an AI SENSE pin for this type of measurement

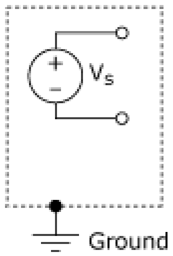
Only use SE measurements if signal >1 V, cabling is short (<1 m) & signals can share common ref at source

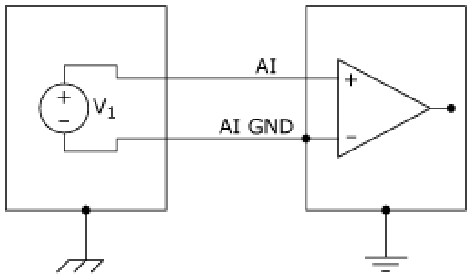
Images taken from NI white-paper 3344

Floating Sources

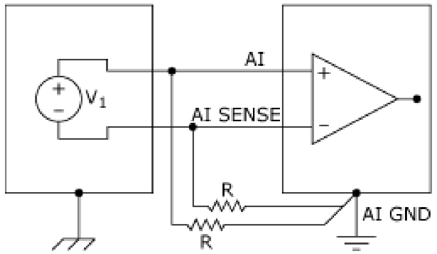
Sources include thermocouples, battery systems, isolation amplifiers, transformers

Ungrounded source

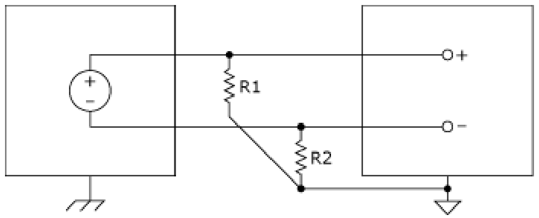




- Referenced single-ended input (RSE)
- But susceptible to noise pick-up on cable shield



- Non-referenced single-end (NRSE)
- Less susceptible to pick-up
- AI SENSE shared between multiple channels
- $10\ \mathrm{k}\Omega < R < 100\ \mathrm{k}\Omega$



- Differential measurement
- Resistors required to provide DC path to ground for bias currents (from inside ADC)

Always use differential measurement for small (<1V) signals

Images taken from NI white-paper 3344

ADC Parameters

$$f_s > 2BW$$

Sample rate

- Ensure sample rate is greater than twice maximum frequency expected (Nyquist criterion)
- Aliasing occurs for signals whose frequency is about the sample rate
- Many ADCs have an anti-alias filter (AAF), *occasionally* with controllable parameters

Resolution

- Resolution $Q = \frac{voltage\ span}{2^M}$ where M is the number of bits
- Eg PXI-6251 has a 16-bit ADC, with a 0.3 mV resolution for its +/-10 V range

To adequately reconstruct a sine wave ensure at least 10 samples per cycle are acquired

Effective Number of Bits

ENOB

- Effective Number of Bits (ENOB) is a measure of the dynamic range of an ADC once noise and distortion are taken into account
- $ENOB = \frac{SINAD - 1.76}{6.02}$ where SINAD is a measure of the total noise and distortion of the measuring circuit (all values in dB)

$$SINAD = \frac{P_{signal} + Pnoise + Pdistortion}{P_{noise} + Pdistortion}$$

Example

- PXI-6251 has total uncertainty (noise) of 0.192 mV on +/-10 V range
- ⇒ SINAD = 80 dB
- ⇒ ENOB = 13 bits

ENOB is around 85% of the actual number of bits

Hardware selection

Low-cost devices (small number of channels, low resolution)

Image: DATAQ INSTRUMENTS, Model DI-1100

Image: MEASUREMENT COMPUTING, Model USB-201

Image: ADVANTECH, Model USB-4704

USB, 4 Diff AI, +/- 10 V, 40 kHz, 12-bit

USB, 8 SE AI, +/- 10 V, 100 kS/s, 12-bit

USB, 8 SE AI, +/- 10 V, 48 kS/s, 14-bit

Hardware selection

Modular devices with more capabilities

Image: KEYSIGHT, Model U2356A

Image: KEYSIGHT, Model U2781A

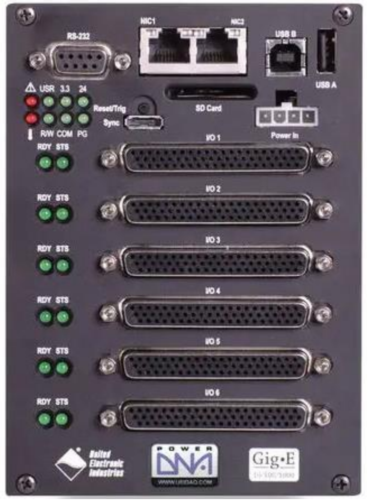


Image: UEIDAQ, Model DNA-PPC8-1G-02

USB, 64 SE/32 Diff AI, 500 kHz, 16-bit

+/- 10V, +/- 5 V, +/- 2.5 V, +/- 1.25 V
Trigger sources
2 AO, 12-bit, +/- 10 V
24 DIO

USB Modular Product Chassis

Up to 384 channels
Star trigger bus
10 MHz reference clock
6 slots

Gigabit Ethernet- based I/O DAQ

6 slots
Real-time: 1000 I/O scans /ms
80 different I/O boards available
Windows, Linux and RT OS

Hardware selection

Industrial grade DAQ systems

Image: DEWESoft, Model SIRIUS Modular

Image: ni.com, Model PXIe-1095

Image: Gantner instruments, Model RAXX

USB/EtherCAT Industrial Modular DAQ

Up to 1 MS/s per channel
Wide range of sensor inputs
Dual 24-bit delta-sigma ADC
+/- 1000 V galvanic isolation

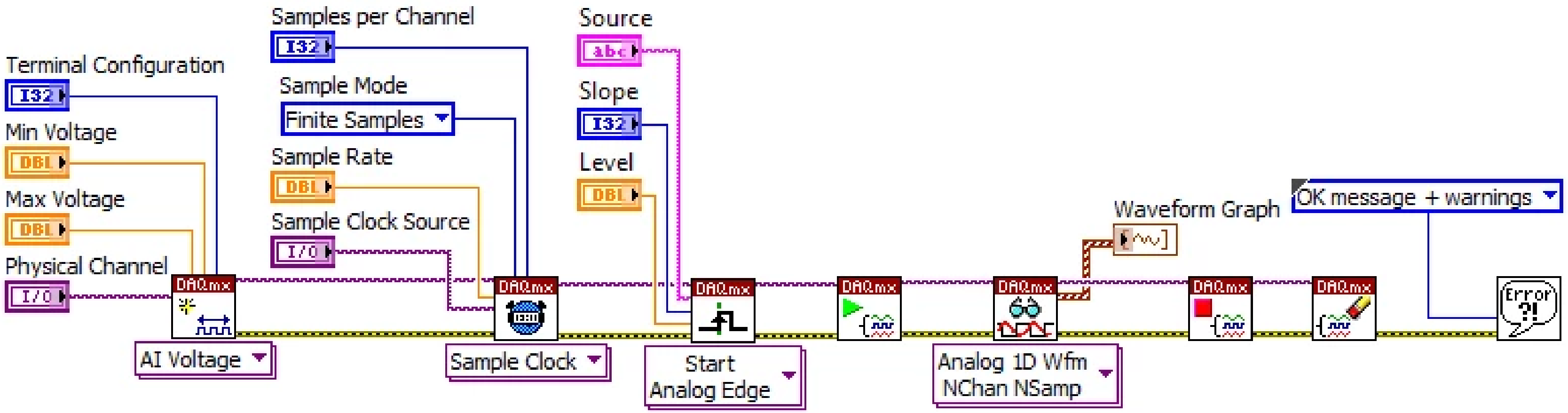
PXIe Modular System

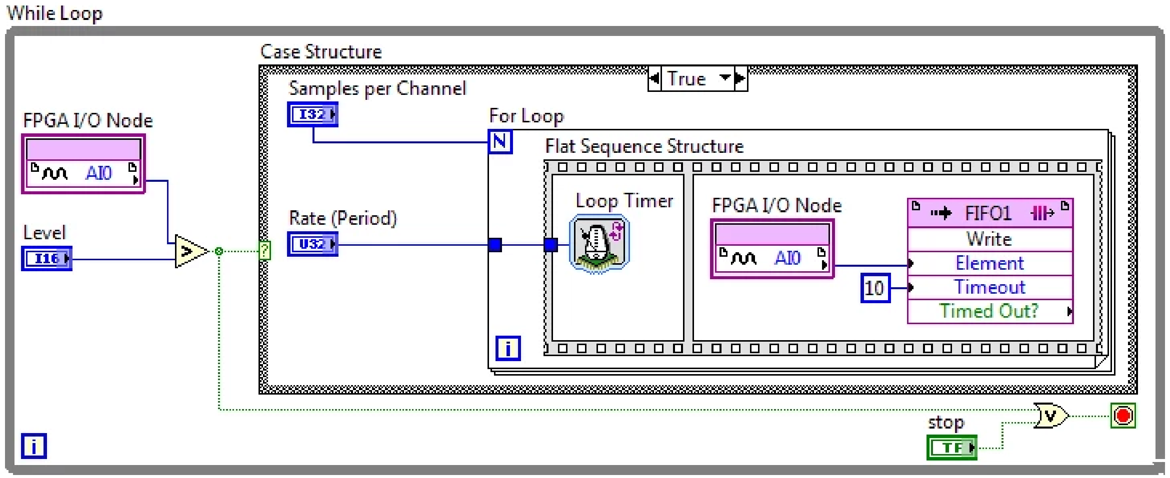
Up to 18 slots
➢ 1500 diversity modules
Redundant and hot swap powers capabilities

DAQ Modular System

13 slots
➢ 100 diversity modules
Up to 24-bit ADC resolution
Up to 100 kS/s / channel

FPGA VS Triggered DAQ

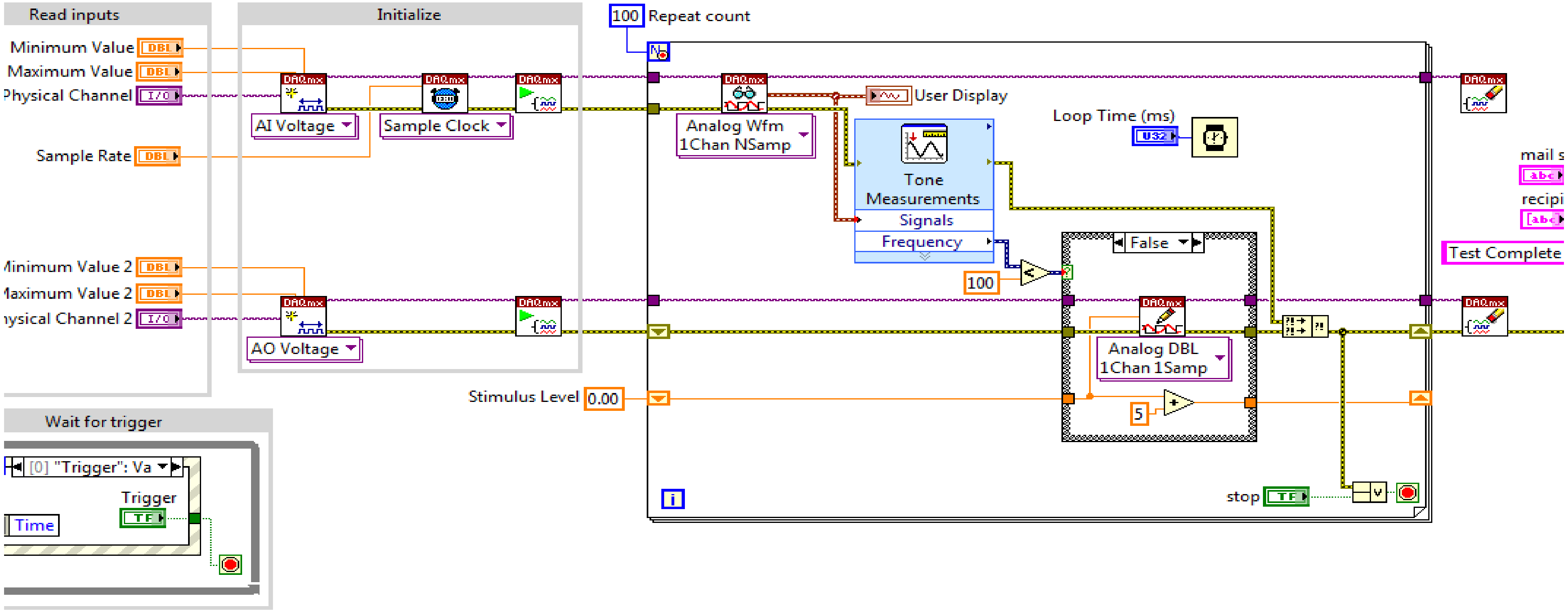




FPGA VS Triggered DAQ

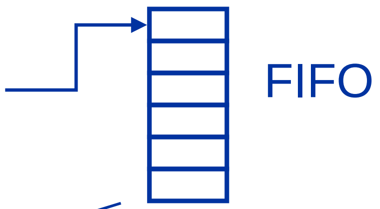
Benefits	**Flexibility**: Enables customization of triggering and the ability to introduce custom signal filtering. **Execution**: Implementation is done entirely in hardware, allowing for real-time and deterministic performance. **Counter**: Can be implemented on any digital lines, providing flexibility	**Simplicity**: Extensive driver and library support in LabVIEW, making it easy to get started with just a few pre-built VIs. **Price**: Generally, offers more cost-effective options compared to FPGA solutions.
Drawbacks	**Price**: FPGA solutions typically come with a higher price **Complexity**: Requires additional programming and design considerations, adding complexity to the development process.	**Limited Flexibility**: Less customization options compared to FPGA for specialized hardware tasks. **Execution**: Performance is dependent on the CPU, potentially impacting real-time capabilities.

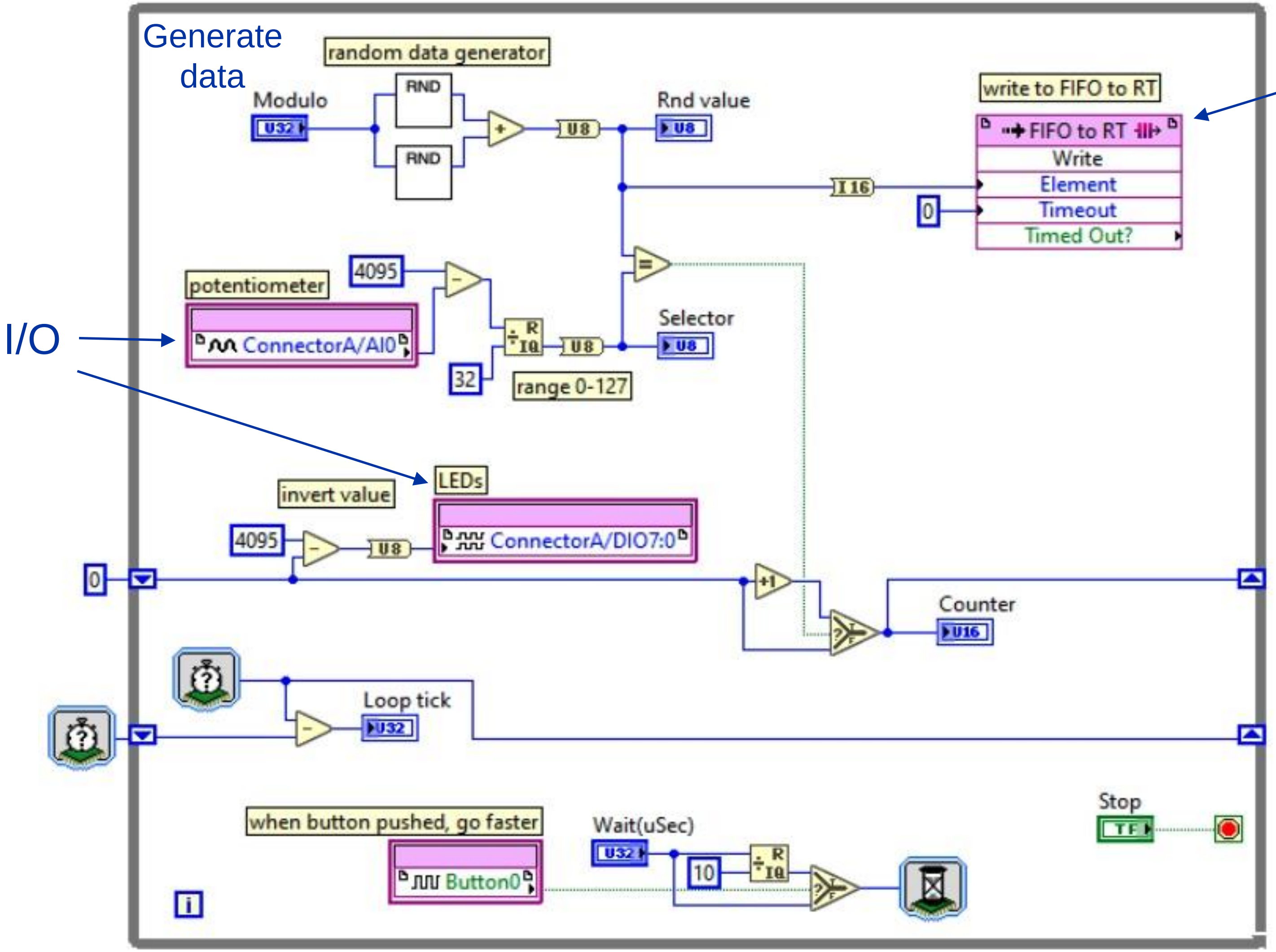
LabVIEW RT - DAQmx



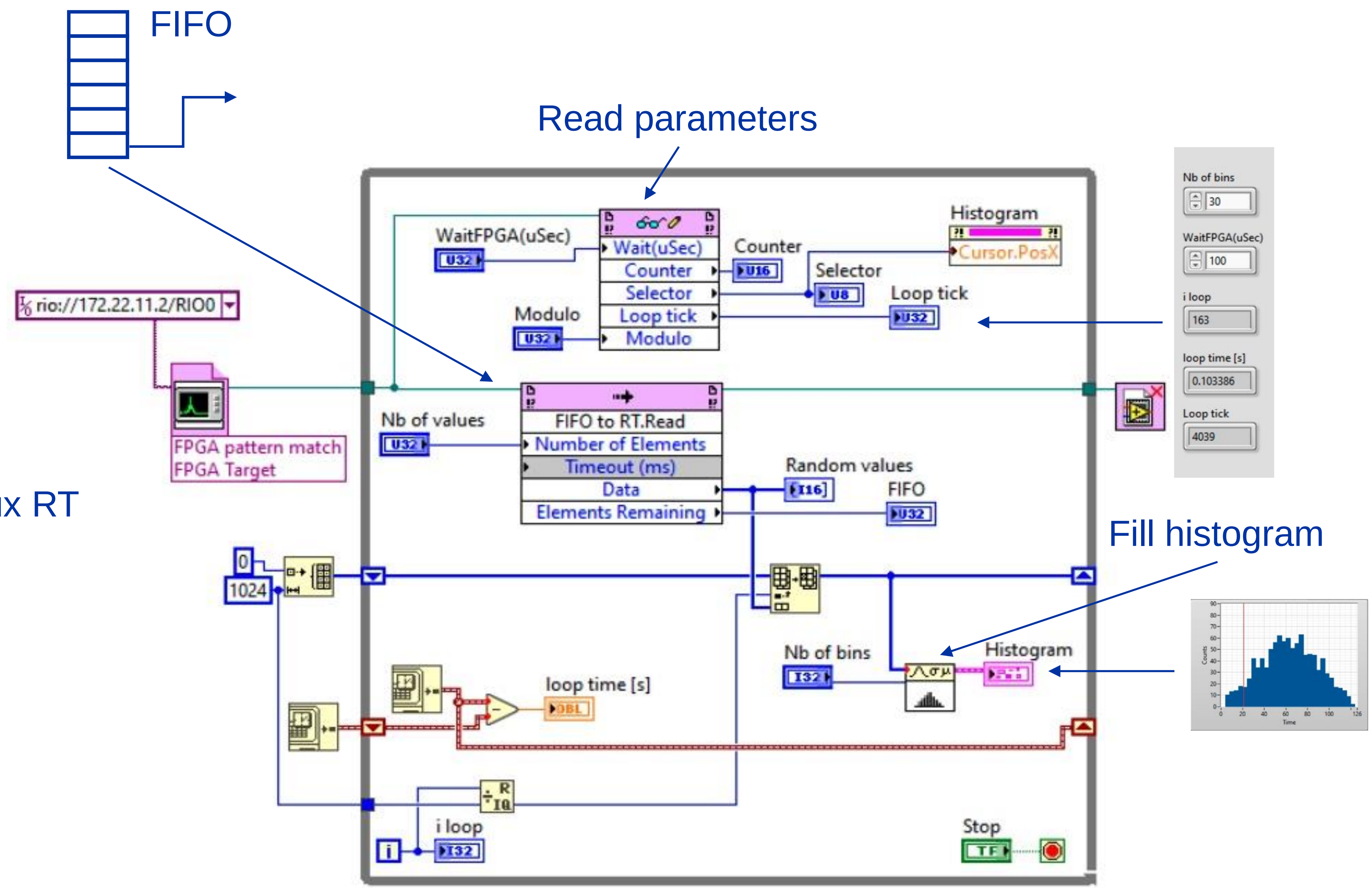
A graphical, dataflow-based programming language
for parallel data acquisition and control systems

FPGA target


FIFO

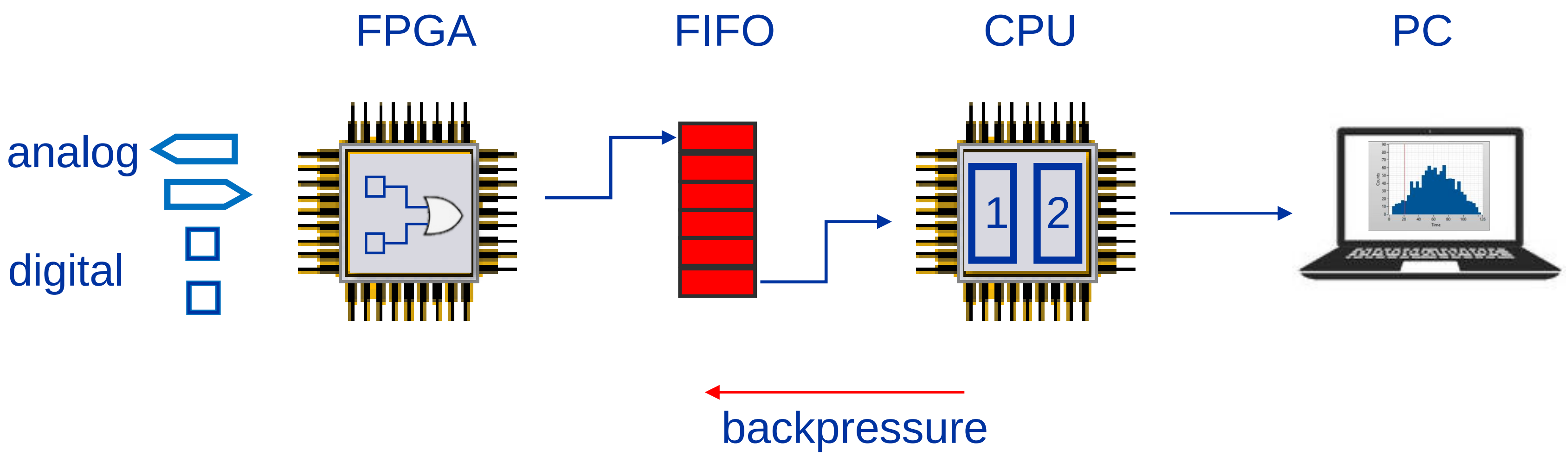

Generate data
random data generator
Modulo
U32
RND
RND
U8
Rnd value
U8
write to FIFO to RT
FIFO to RT
Write
Element
Timeout
Timed Out?
I16
0
4095
potentiometer
ConnectorA/AI0
Selector
U8
32
range 0-127
I/O
invert value
LEDs
4095
U8
ConnectorA/DIO7:0
0
+1
Counter
U16
Loop tick
U32
when button pushed, go faster
Button0
Wait(uSec)
U32
10
Stop
TF
i

RT target



ARM running Linux RT

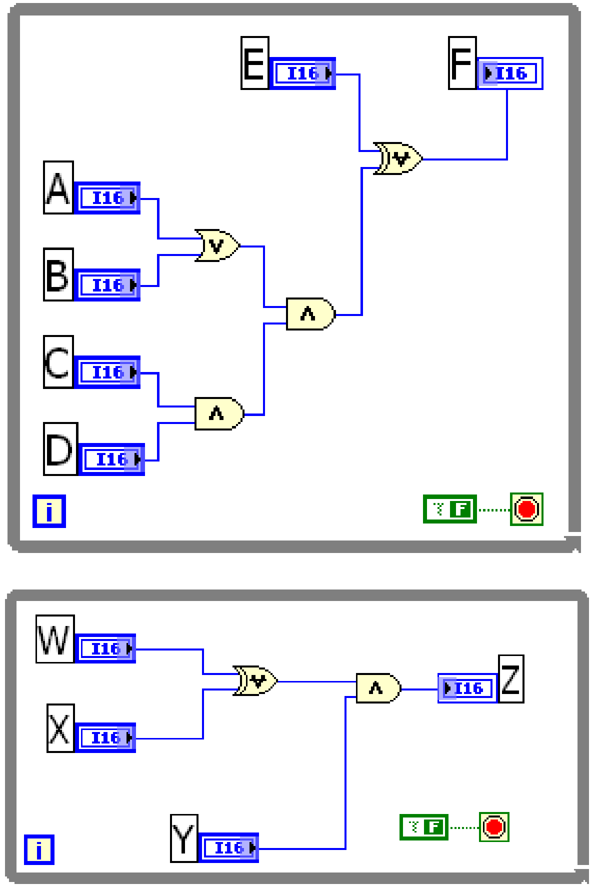
Backpressure from ARM processor

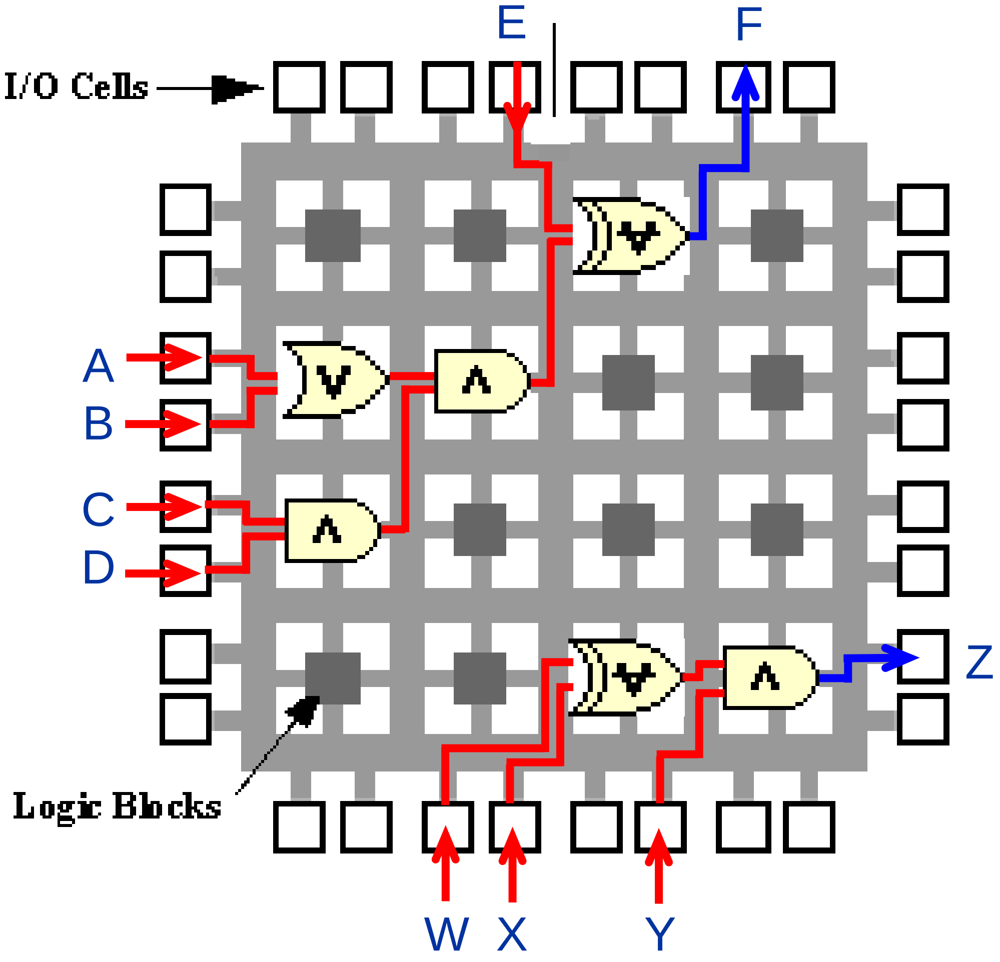


1. If CPU too slow to empty FIFO
2. FIFO will fill up
3. When FIFO full, data will be lost

FPGAs = Parallel Dataflow Systems

F = {(A+B)CD} ⊕ E



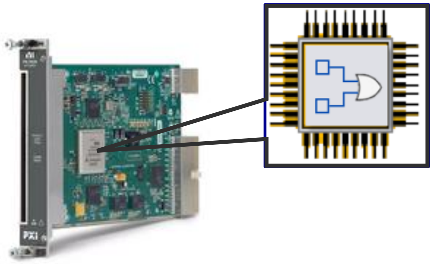


Hardware in magnet TBs

Magnet protection


Potaim cards


uQDS crate


PXIe FPGA card

Magnet instrumentation

Instrumentation connectors

DAQ patch panels

Signal filtering & DAQ

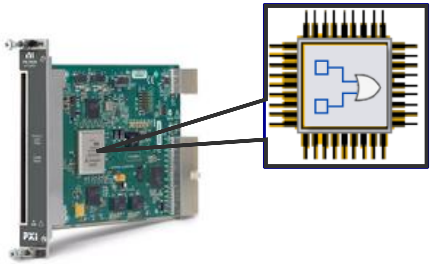

Low pass filtering


Modular HF/LF DAQ system

Interlocks


Interlock PLC


Safety matrix


PXIe FPGA card

Hardware protection

High voltage, high current = Lots of energy = Lots of noise

Consideration has to be made if the protection should only cover the DAQ or is it also protection the sample under test

Fresca magnet = 5MJ, LHC magnet = 3MJ , 1kg of TNT 4MJ

-> How much is that??

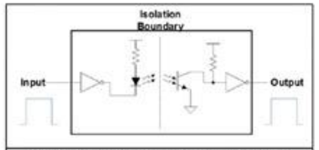
1 Big Mac = 550 kcal = 2300 kJ

1 LHC magnet at nominal current = 1300 Bic Macs.

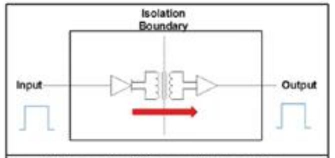
Hardware Protection – Galvanic Isolation

Implementing Galvanic Isolation for Analog Inputs on DAQ Cards:

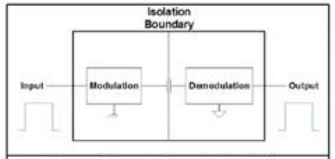
1. Identify the voltage/current levels of your signals.
2. Consult the manufacturer's documentation for maximum thresholds
3. Determine which analog inputs require galvanic isolation.
4. Choose the appropriate isolation technique
   (e.g., optocouplers, digital isolators, transformers).
5. Install the isolated components, following manufacturer's instructions.
6. Ensure proper grounding to minimize ground loops and interference.
7. **Properly test and validate the effectiveness of the isolation**
8. Verify signal integrity, accuracy, and noise levels under various cond
9. Adjust and optimize the isolation setup as needed.



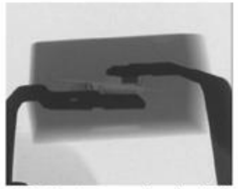
Optocoupler Galvanic Isolation

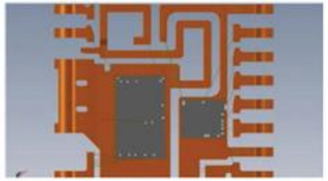


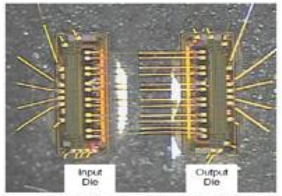
Magnetic Galvanic Isolation



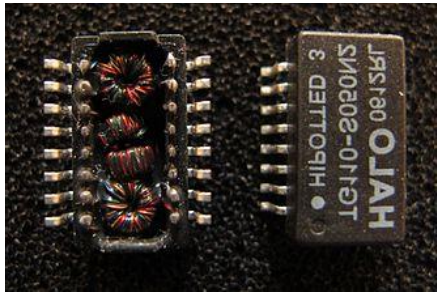
Capacitive Galvanic Isolation


1A:Optocoupler isolation


1B:Magnetic isolation



1C:Capacitive isolation



https://www.powersystemsdesign.com/articles/capacitive-isolation-the-future-acdc-power-conversion/22/13381
https://en.wikipedia.org/wiki/Galvanic_isolation

Storage

- **Things to consider:**
  - Data volume
  - Data lifetime
  - Transfer speed, latency and throughput
  - Precision
  - Read versus write speed
  - Budget
  - What technology is already used
  - What standards are already in place
  - Environment
  - Local or remote
  - Etc..

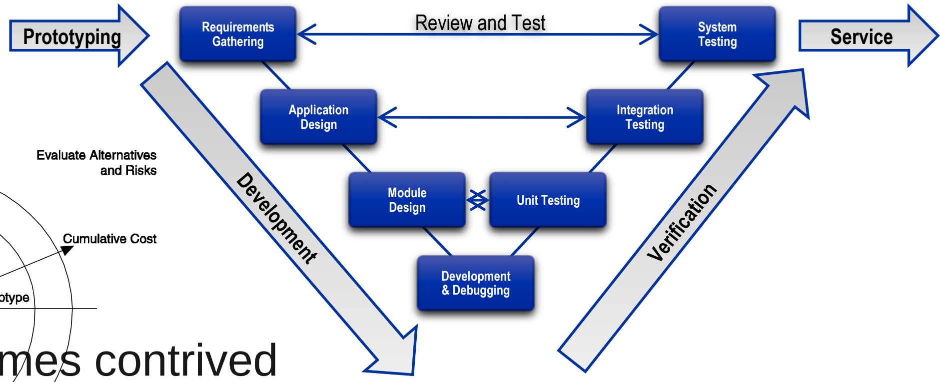
CERN data Centre

USB Storage

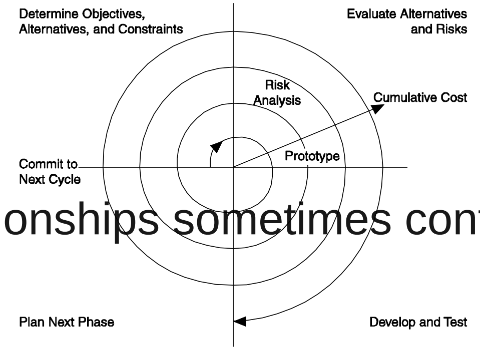
Software Engineering Process Model

- **Waterfall**
  - Advantages: documentation, audit trail, accountability
  - Disadvantages: static requirements, high overhead

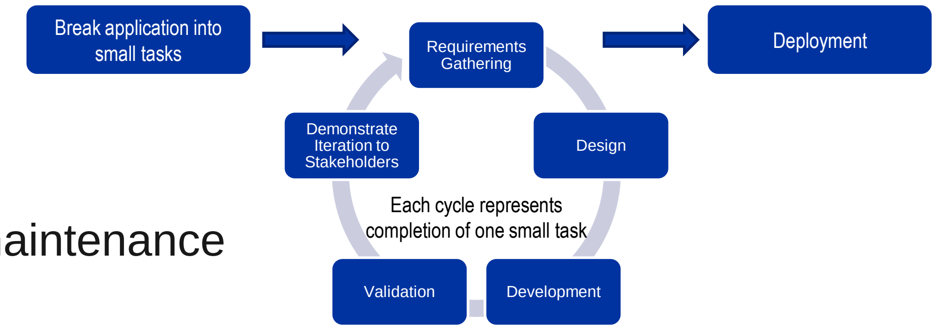
- **V-model**
  - Advantages: Tie between design and test
  - Disadvantages: needs well-written requirements, relationships sometimes contrived



- **Spiral model**
  - Advantages: Risk-based approach to development, iterative development
  - Disadvantages: Integration issues



- **Agile model**
  - Advantages: “Light-weight” process, iterative development
  - Disadvantages: Co-location generally required, works better for maintenance



Source Control

GitLab, as a source control platform for LabVIEW programs

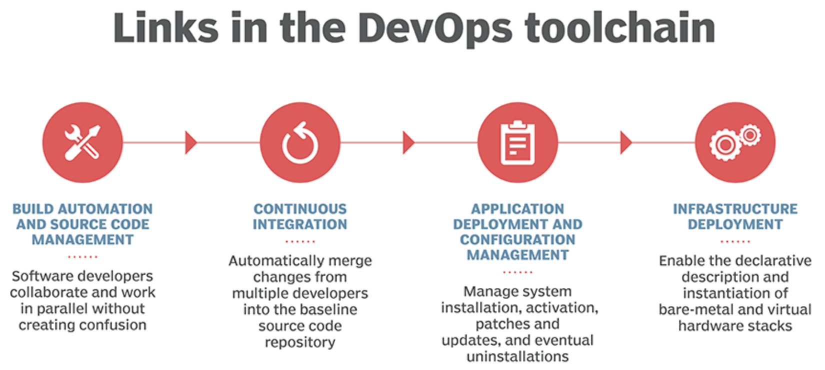
- Provides version tracking, collaboration, and code integrity. It allows multiple developers to work on LabVIEW code simultaneously, managing different versions, facilitating collaboration, and ensuring code integrity and history.

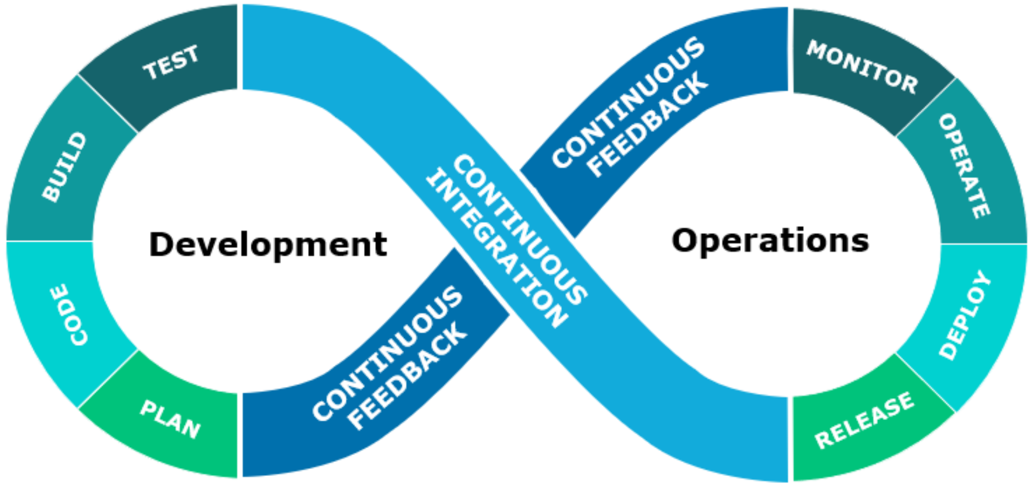
Benefits of Source Control	Drawbacks of Source Control
Version control: Allows tracking and managing different versions of LabVIEW programs, facilitating collaboration and avoiding version conflicts.	Administration: Properly configuring and managing source control settings can require careful attention and administration.
Rollback and history: Allows easy rollback to previous versions and provides a detailed history of changes made to the LabVIEW code over time.	LabVIEW Binary format: Handling branching, merging, and resolving conflicts in a LabVIEW environment can be more complex compared to text-based programming languages.
Traceability: Enables tracking changes made to the LabVIEW code, including who made the changes and when, facilitating troubleshooting and auditing.	

Dev Ops / Configuration Management

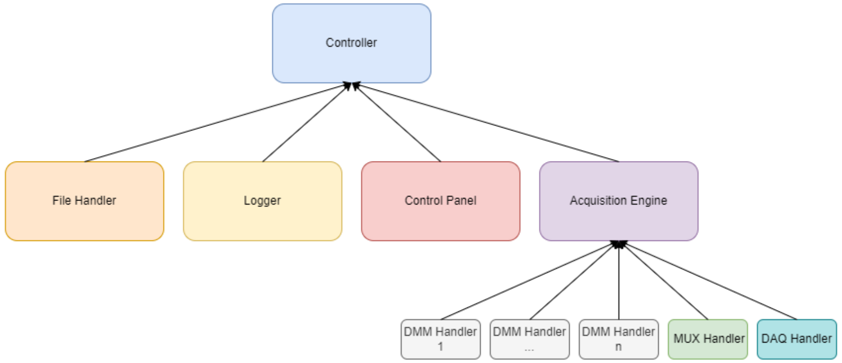
Activities designed to monitor and assure fluent evolution of a software product

- Source code control (e.g. GIT)
- CI/CD pipeline engines
- Artifact repositories





System architecture

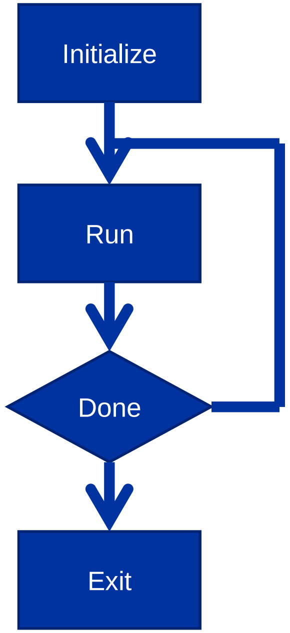


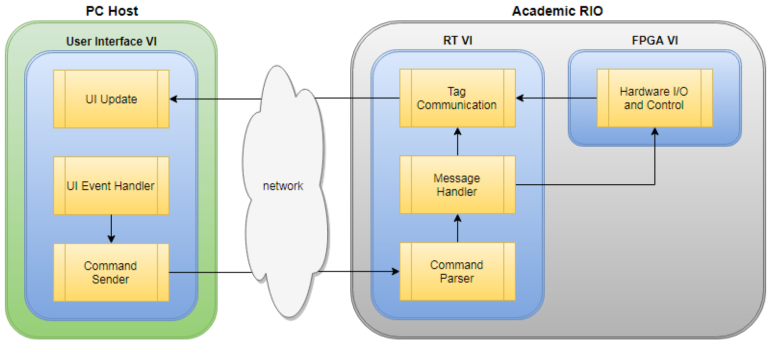
How is it represented?

- Prototypes/Skeleton
- Documentation
- Diagrams

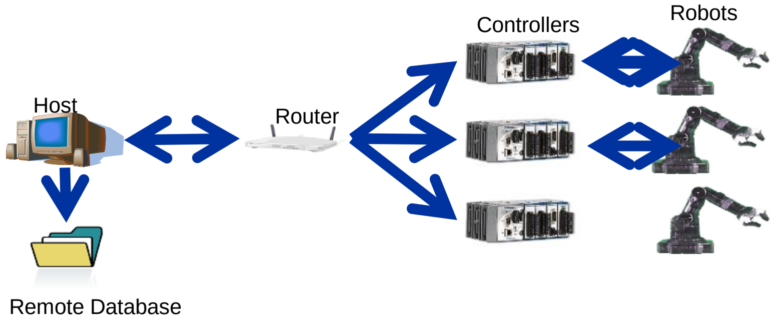
How is it used?

- To communicate with stakeholders
  - Builds confidence in investment
  - Helps to encapsulate requirements and identify gaps in them
- To guide development
  - Answers “Where are we going?”
  - Defines processes, communication paths, modules, and algorithms
  - Provides a framework to fill in
- To guide test
  - Identifies areas to focus on for integration testing
  - Identifies potential trouble spots for white-box testing
- To guide debugging
  - Shows which processes and modules have access to specific data items
- To guide maintenance
  - Provides a primer for future developers

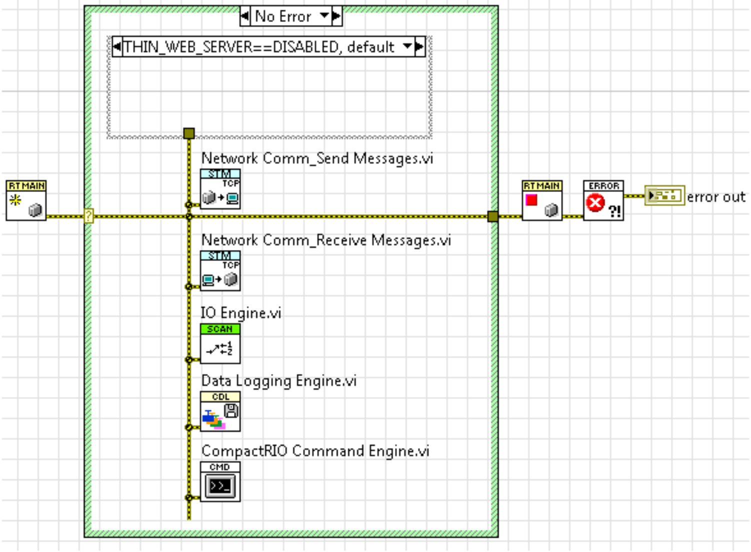




Graphic adapted from Fig 1.3 in *NI LabVIEW for CompactRIO Developer's Guide*

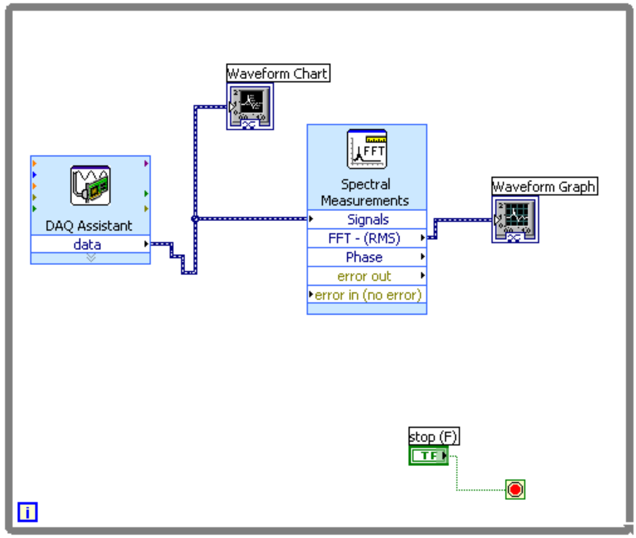


Building a prototype – “Spikes”



Advantages of Prototyping

- Risk mitigation
- Evaluation of requirements
- Rapid development (minimal software engineering process)
- Communication to stakeholders
- Evaluation of design alternatives

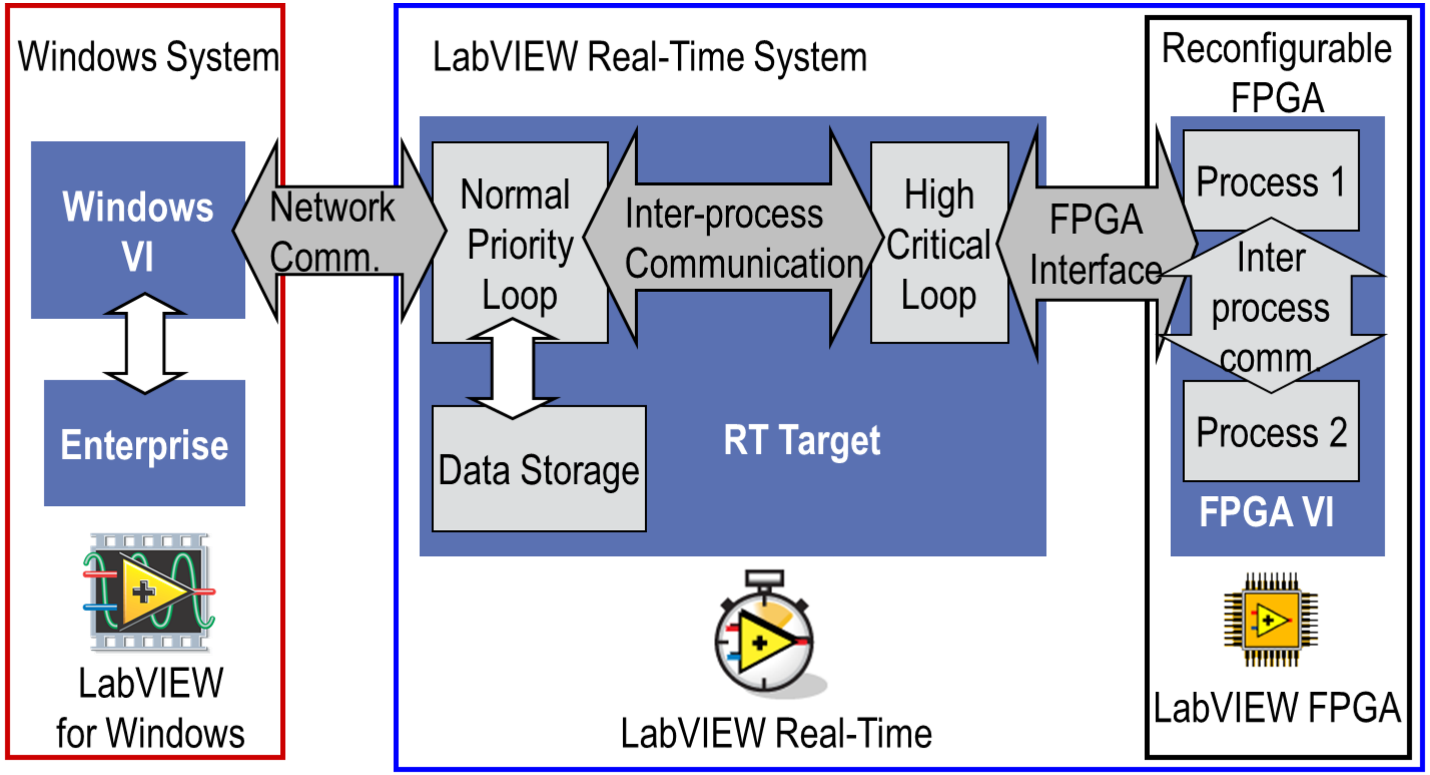


Creating a Prototype is not the same thing as developing.

Best practices - Communication

Considerations

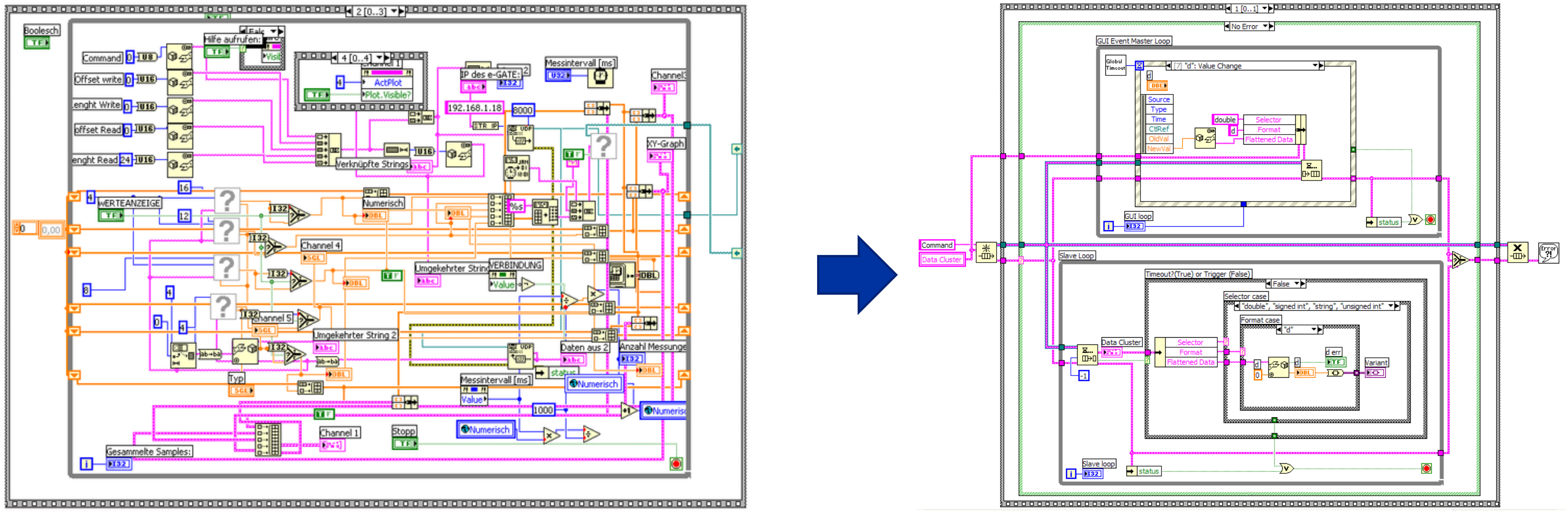
- Type of transfer
- Performance
  - Latency
  - Throughput
- Ease of implementation
- Scope/Scalability



Best practices - Modularity

Goals

- Decoupling
- Cohesion
- Encapsulation
- Scalability
- Testability



Best practices – Design Patterns

What is a Design Pattern?

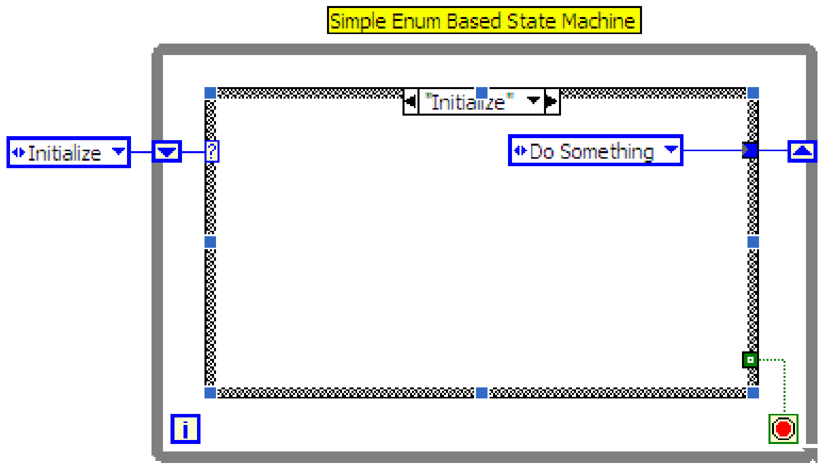
- A well-established solution to a common problem.

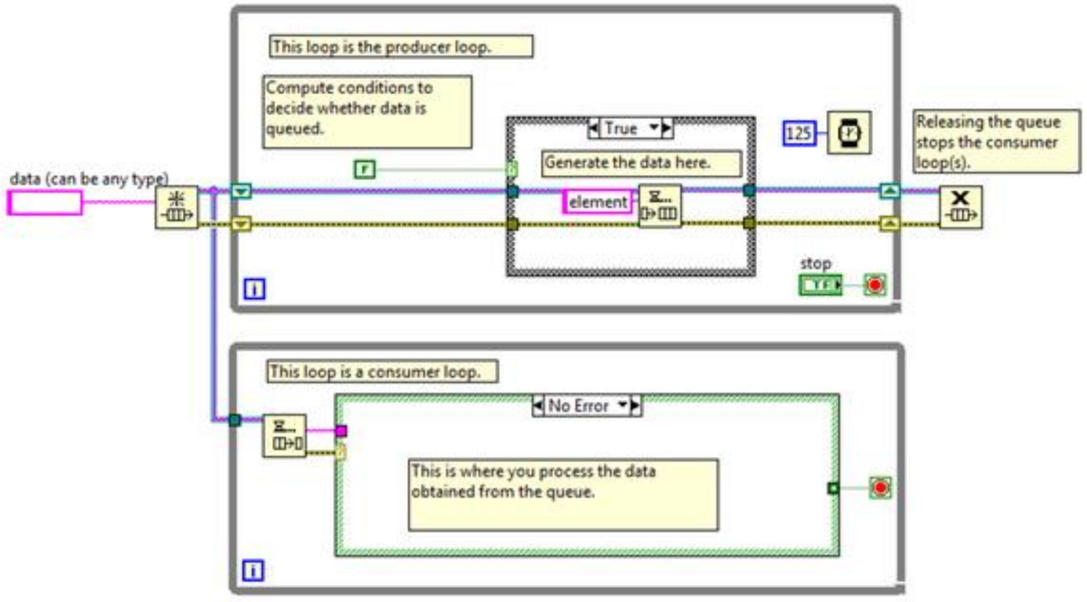
Why Should I Use One?

- Save time and improve the longevity and readability of your code.

How does it help?

- Simplifies and increases consistency of code
- Enforces good coding practices (scalability, modularity)
- Enables parallel execution
- Simplifies introduction of error handling
- Takes care of internal communication within the application

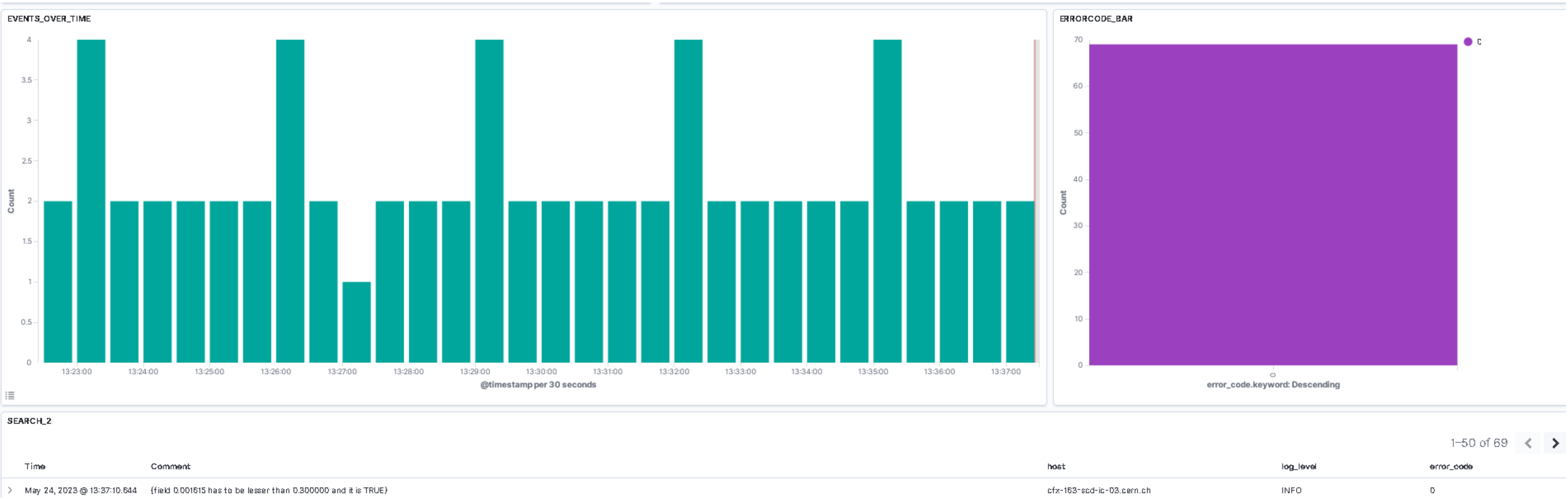


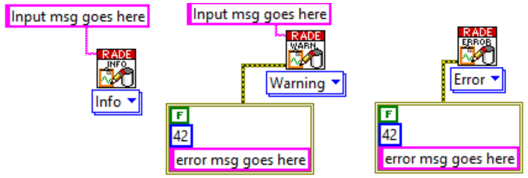


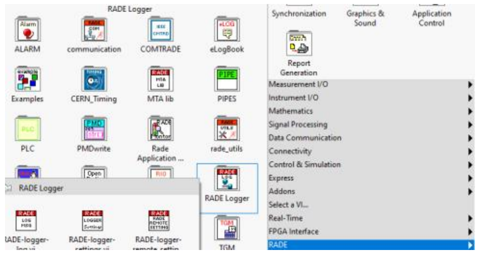
RADE-Logging – OpenSearch dashboard

RADE Logging - based on OpenSearch

- Powerful Search Capabilities: OpenSearch provides robust search capabilities, allowing you to effectively search and analyse your logs.
- Scalability: OpenSearch is designed to handle large volumes of log data efficiently
- Flexibility: OpenSearch offers flexibility in terms of data ingestion and integration with various logging agents (Logstash)
- Extensibility: OpenSearch is an open-source project



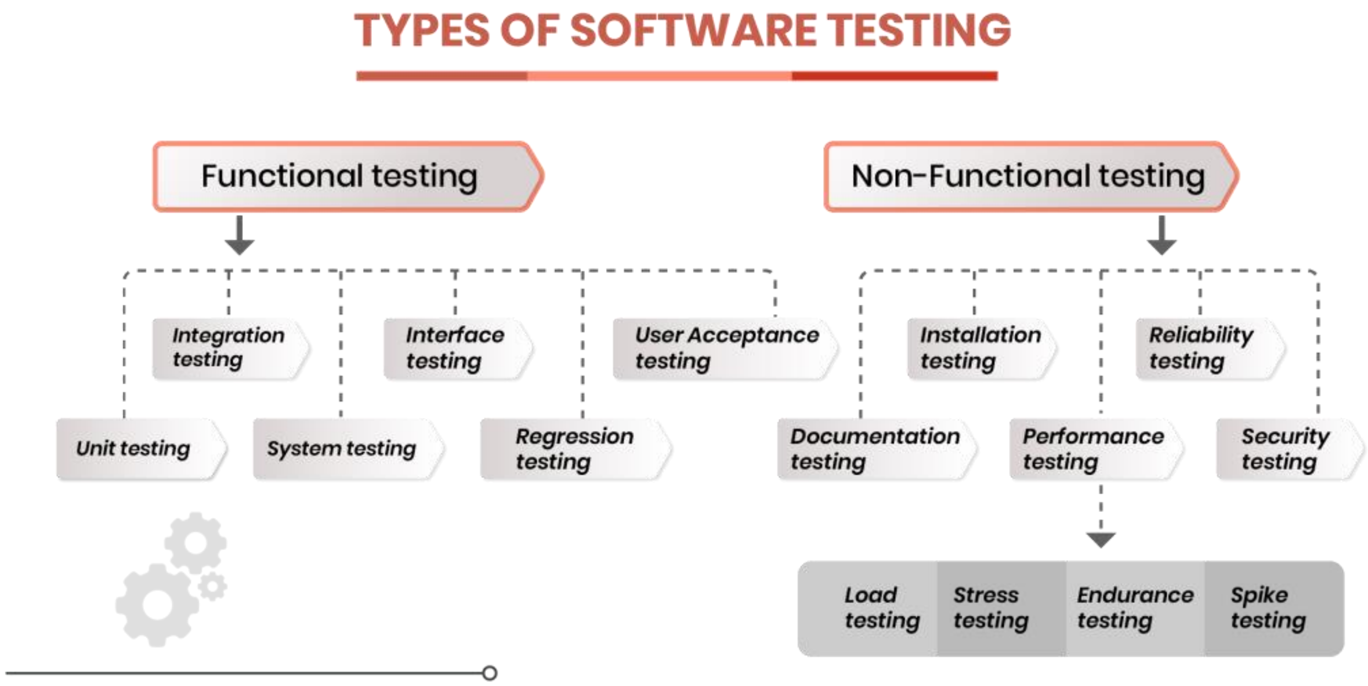




Best practices - Validation

Types of Validation?

- Code Reviews
- Static Code Analysis
- Unit Testing
- Integration Testing
- System Testing



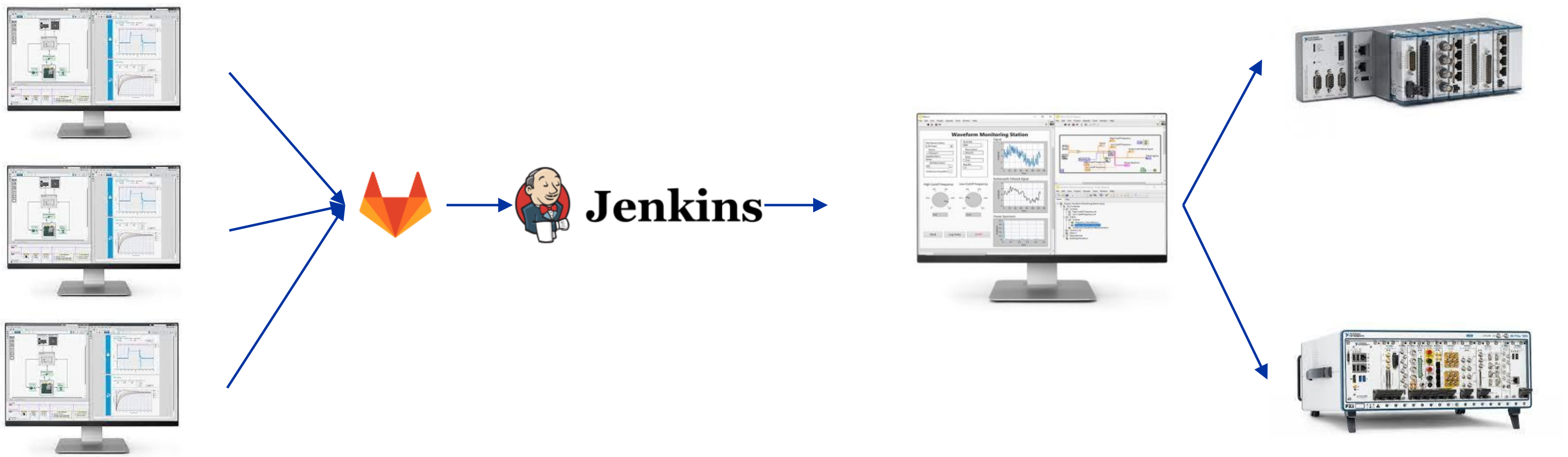
Team-Based development

Monolithic systems

- Team-based approach allows for close collaboration among team members. Developers can work together on a single, centralized codebase, enabling easier coordination, code sharing, and faster communication. This approach is beneficial for smaller teams working on projects that do not require extensive distribution of work or parallel development.

Distributed systems

- Communication and coordination become crucial, requiring well-defined interfaces, clear documentation, and regular communication channels. Parallel development and merging of code from different team members across distributed locations may require additional effort to manage conflicts and ensure code consistency.



Current Situation

Target