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PyLog-HLS4ML Integration: Introducing higher level of automatic design in HLS4ML

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HLS4ML is an influential Python package that creates firmware implementations of machine learning algorithms uses high-level synthesis (HLS) technique. While most of the templates are hand-written in HLS4ML, we want to further automate this manual design process by introducing PyLog, an algorithm-centric Python-based FPGA programming and synthesis flow, into the current HLS4ML flow and therefore providing a more efficient design pathway as well as initial design space explorations while maintaining the same level of performance compared to the original manual design. We hope this effort could help improve the scalability as well as the usability of HLS4ML.

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