

Machine learning evaluation in the Global Event Processor FPGA for the ATLAS Phase 2 Level 0 trigger upgrade

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During the next update of the High-Luminosity Large Hadron Collider (HL-LHC) of ATLAS, a new global trigger subsystem will be installed into the L0 Trigger. New and improved hardware and algorithms will be deployed during the upgrade to increase the performance of the trigger system. The global trigger subsystem consists of various components, including the FPGA-based Global Event Processor (GEP), which processes the data through the trigger algorithm. Within the GEP, data will be pipelining through different Algorithm Processing Units (APU), which handle individual subtasks of the overall trigger. We present our work in creating an APU specification and sample APU as a guide to future APU developers. We also present a redesign of the APU interface to follow the AXI-stream protocol, which allows streaming computations that overlap operations at multiple pipeline levels, potentially improving overall throughput. Finally, we present our work deploying HLS4ML and FwX (two high-level synthesis tools for machine learning) into the APU development. HLS4ML is a design tool for generating a deep neural network (DNN) algorithm model with ultra-low delays, and has been developed specifically to support the needs of high-energy physics experiments, while FwX is another tool for generating the boost decision tree models. Our goal is to demonstrate that the application of HLS4ML to APU development is practical, and we have already implemented Gluon Tagger model using convolution neural network (CNN) for the APU. The performance of the Gluon Tagger APU is tested using a test vehicle and a sandbox provided by the ATLAS developers. The next step is developing another new algorithm using a deep neural network.

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