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Benchmarking HLS4ML vs. SystemVerilog

Monday 10 July 2023 19:00 (2 hours)

High-level synthesis (HLS) offers the promise of simpler and easier hardware development, but at a cost. We consider the application of high-level synthesis to machine learning applications, seeking to quantify the resource and performance costs of this technique within the widely used HLS4ML framework. By creating carefully optimized SystemVerilog versions of identical HLS4ML designs, we demonstrate that the HLS designs are very competitive with hand-optimization techniques. We also identify weaknesses in the existing tools, and develop work-arounds to help provide significant quality improvements.

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