UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

cherenkov telescope array

The LST Advanced SiPM Camera

M. Heller on behalf of SiPM Camera WG - 13/12/2023

Courtesy of D. Kerszberg

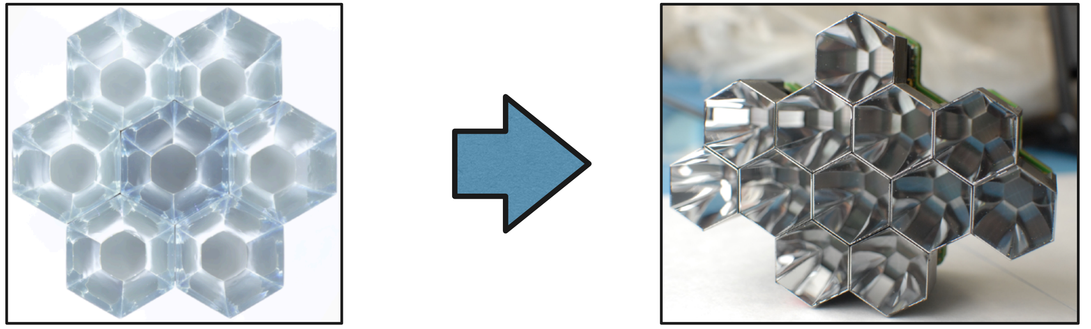
The Advanced SiPM Camera

- The proposed design should take full advantage of the SiPM characteristics
  - ✦ Gain in duty-cycle, robustness, stability, self-calibration, etc…
  - ✦ Utilise Swiss experience in using SiPM for IACT (FACT, SST-1M)

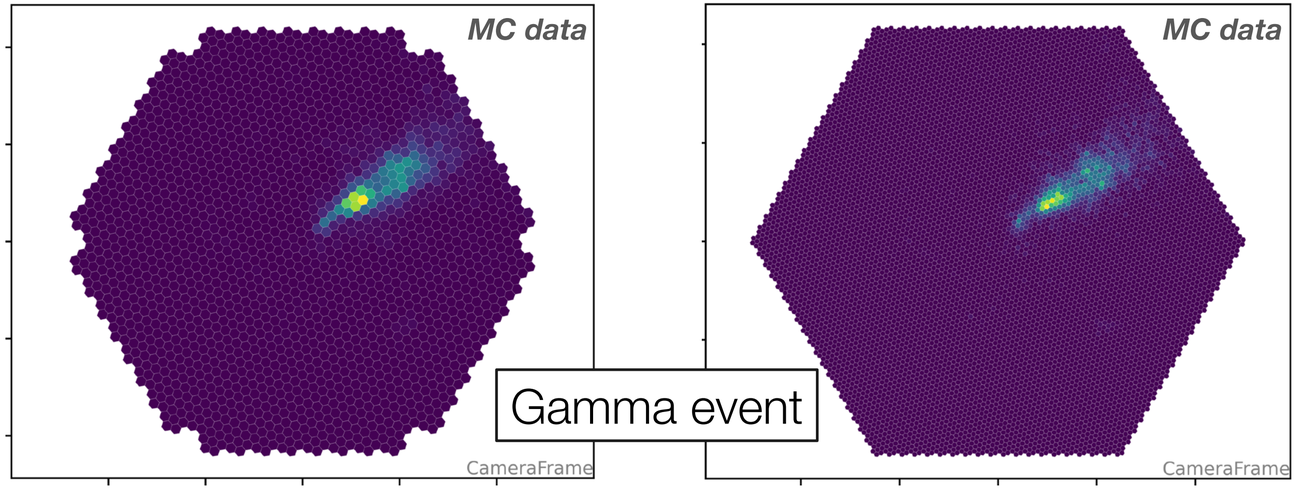
- The Advanced SiPM Camera must:
  - ✦ outperform the existing camera over the entire energy range
  - ✦ be upgradable/reprogrammable

- Baseline design:
  - ✦ Decreasing pixel size **from 0.1° to 0.05°**
    - ◉ **4 times more pixels !**
  - ✦ Going for **fully digital readout**

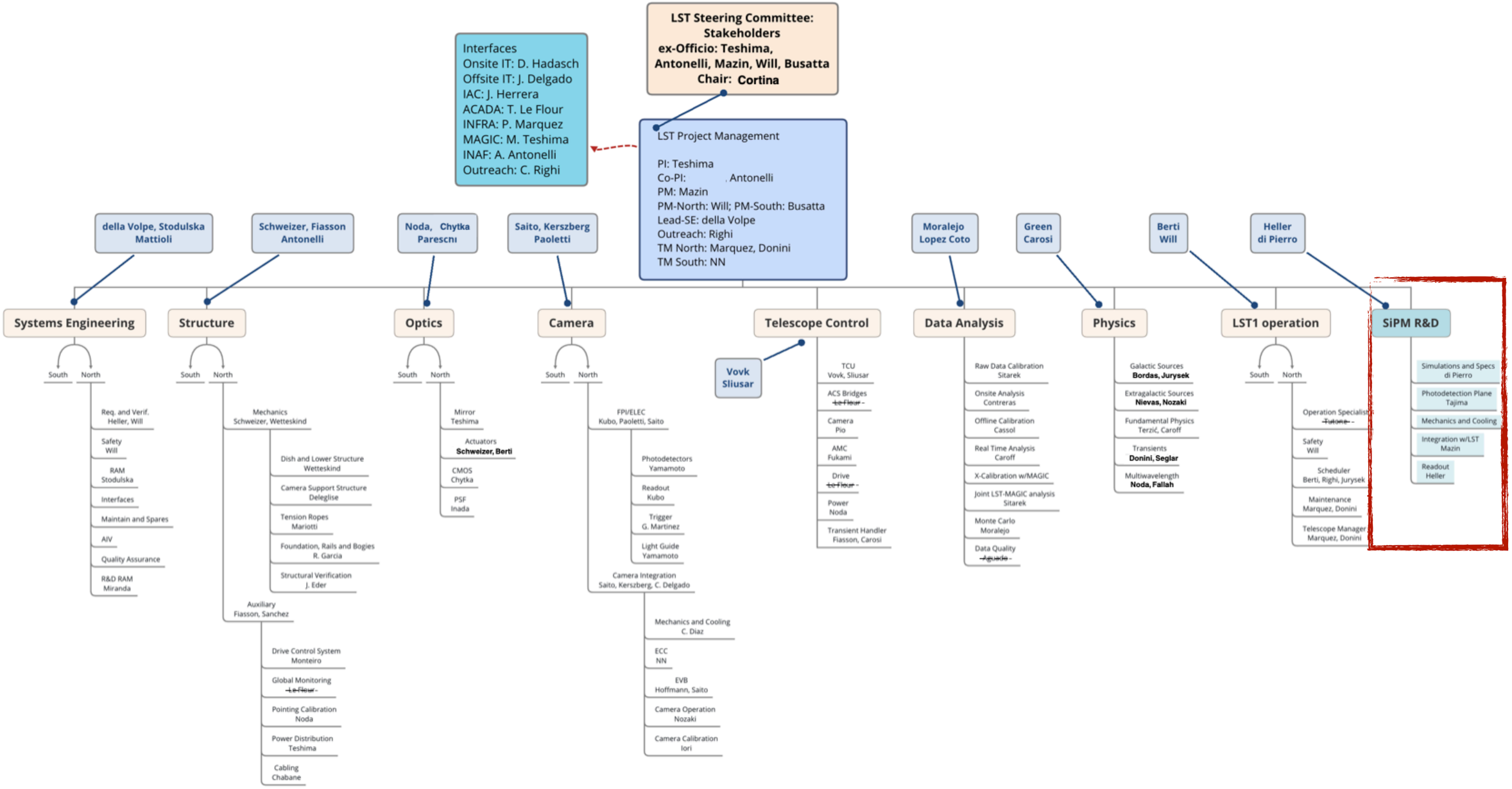
- Many challenges to tackle:
  - ✦ High power consumption
  - ✦ High data throughput
  - ✦ High cost



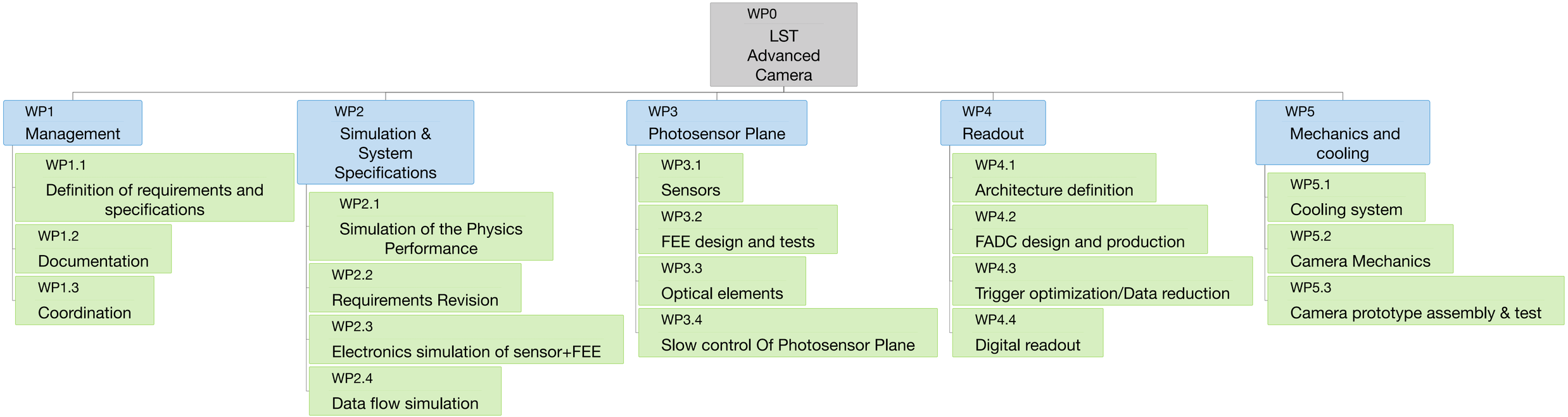
LST PMT camera **(0.1°)** LST SiPM camera (**0.05°**)



The Advanced SiPM Camera in LST+



A project within a project

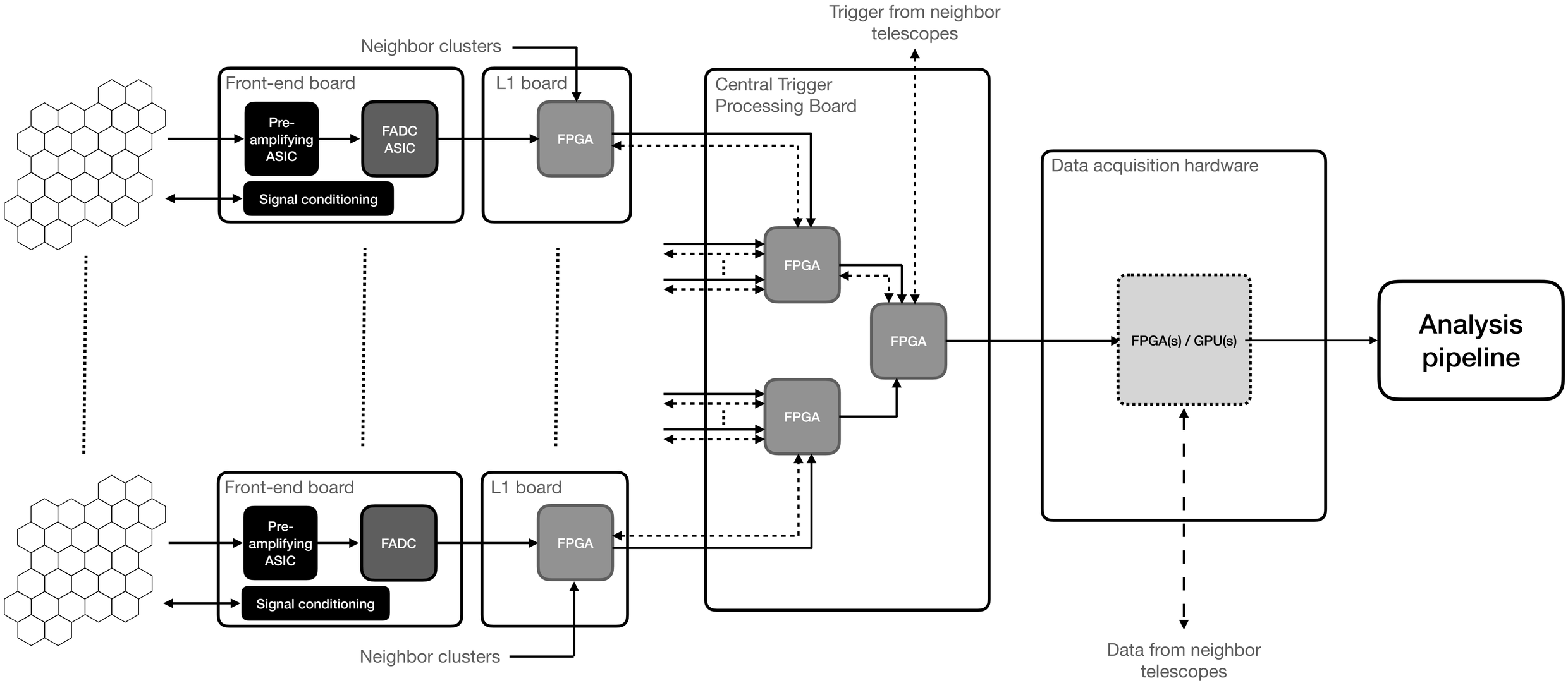


- Critical work packages which were not covered a year ago are starting to be addressed:
  - ✦ Timing (synchronisation, clock distribution)
  - ✦ Mechanics

- Increasing effort on data analysis with both classical and artificial intelligence pipeline (See T. Miener's talk)

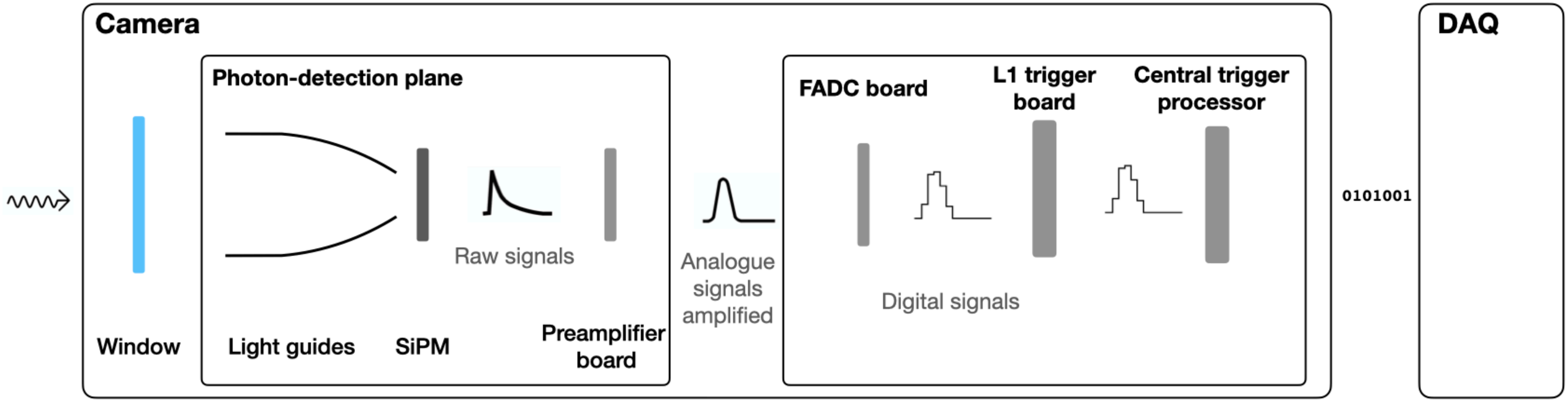
Camera readout architecture

Simplified view



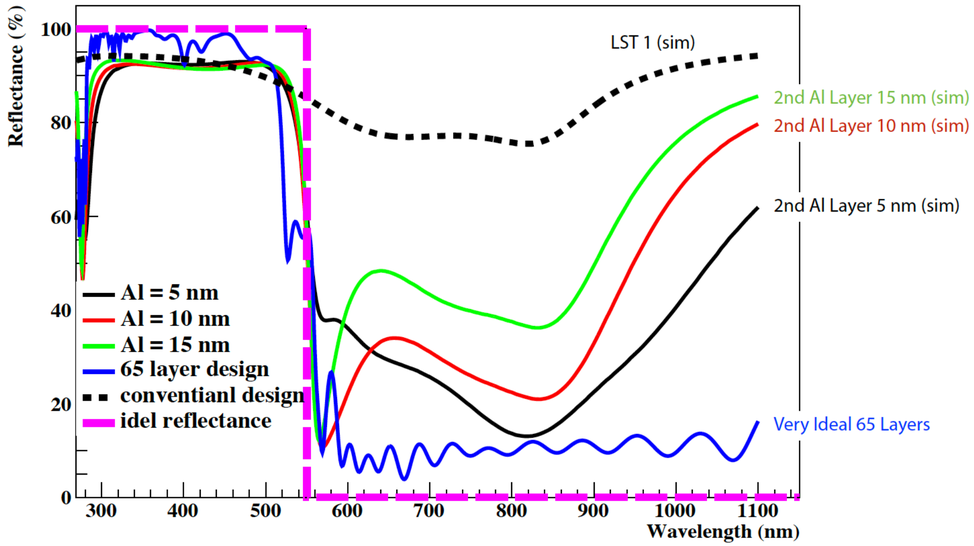
Camera readout architecture

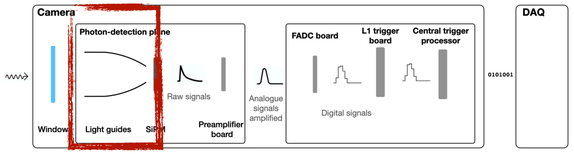
Even more simplified…

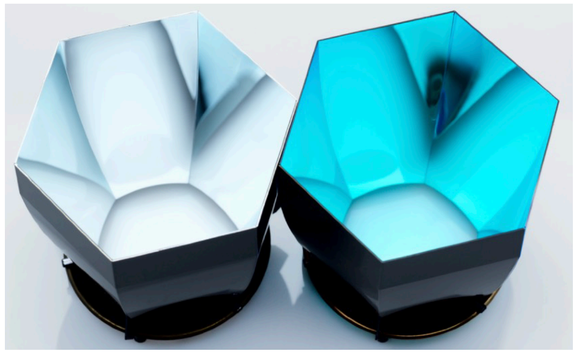


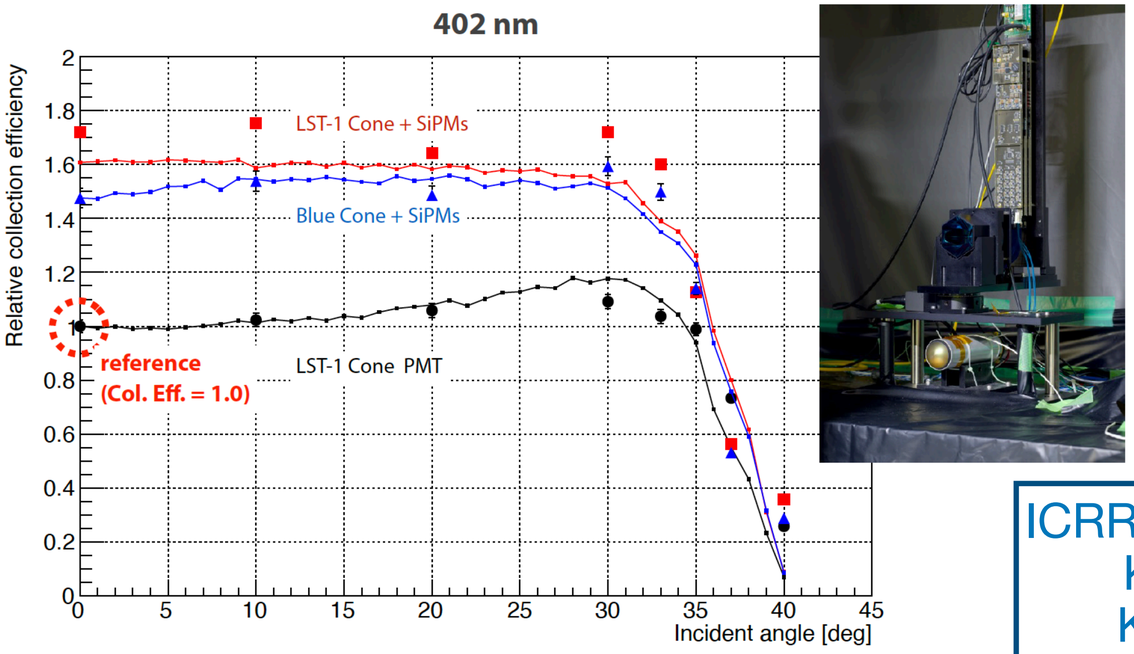
Light guides

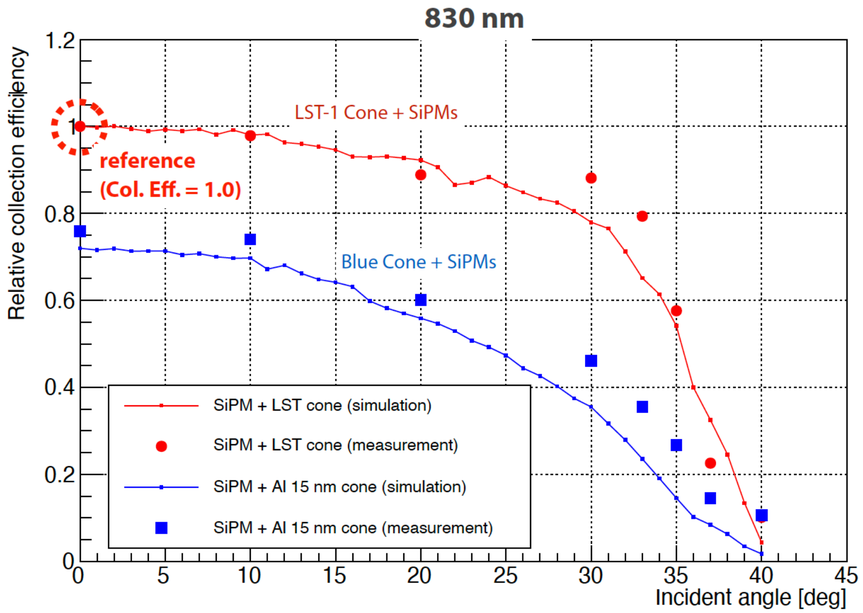
- In order to increase background reduction, study of "blue" light guides
- Prototype shows 40% absorption > 550 nm









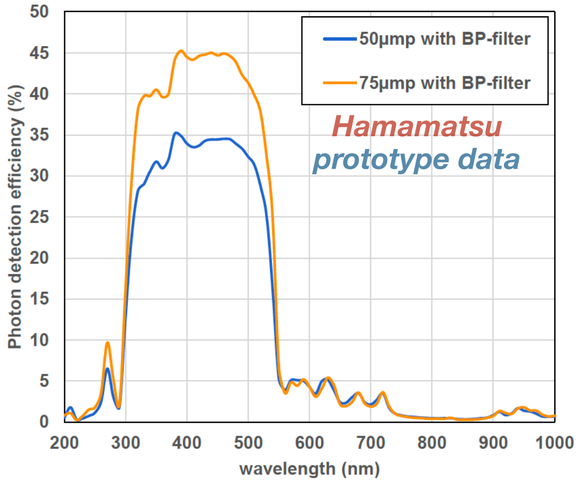


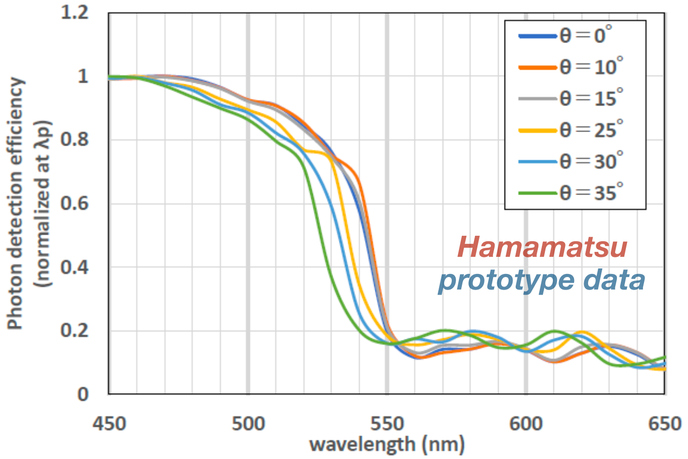
ICRR, University of Tokyo
Kyoto University
Konan University
ISEE, Nagoya University

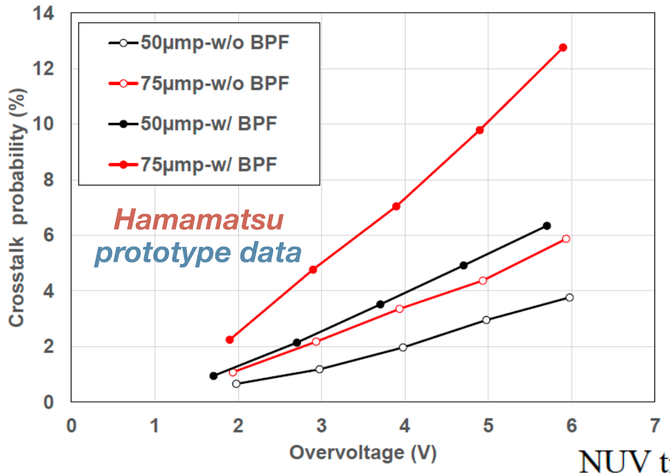
A. Okumura, ICRC 2021

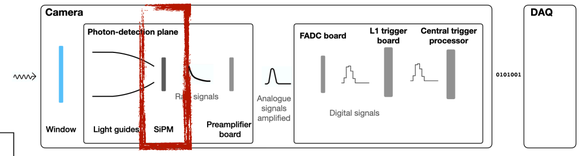
Light sensors

Hamamatsu, Japan

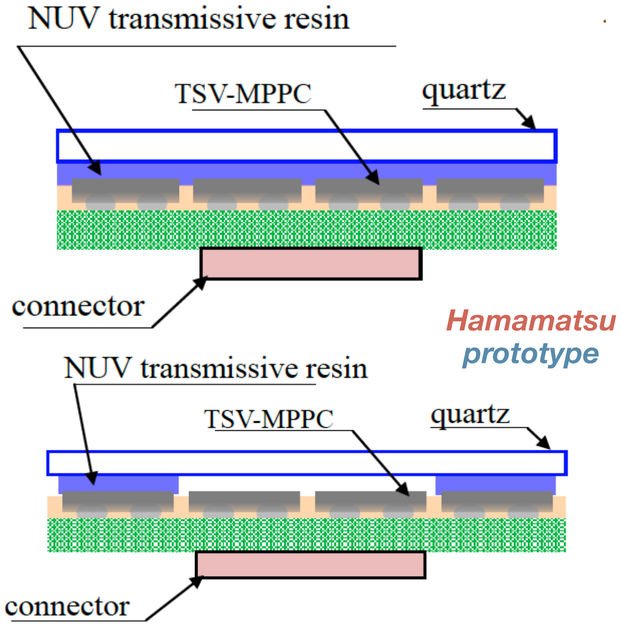








- In collaboration with UNIGE, development of tailored sensors for IACTs
- Recent update from Hamamatsu:
  - ✦ UV sensitivity:
    - ◉ Achieved by improving wafer processing for lattice defects reduction in the photoelectric conversion layer
  - ✦ Sensor coating
    - ◉ New run for on-sensor coating with high transmissivity in the UV, first sensors expected for March 2024
    - ◉ Increase of optical cross talk (x2) confirmed, but at working point, still < 8%
  - ✦ R&D on packaging to minimise optical losses and increase sensor robustness



Pre-amplifying stage

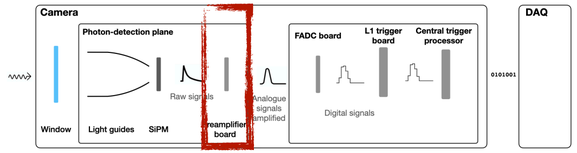
University of Geneva
Universitat de Barcelona
Universitat Politecnica de Catalunya

- Key specifications:
  - Power consumption: 40 mW per pixel
  - Dynamic range: 1-250 p.e with single p.e. resolution
  - Signal-to-noise ratio of 5
  - Fast response: 3-5 ns FWHM

- Key features:
  - Active summation
  - Slow integrator for night sky background monitoring

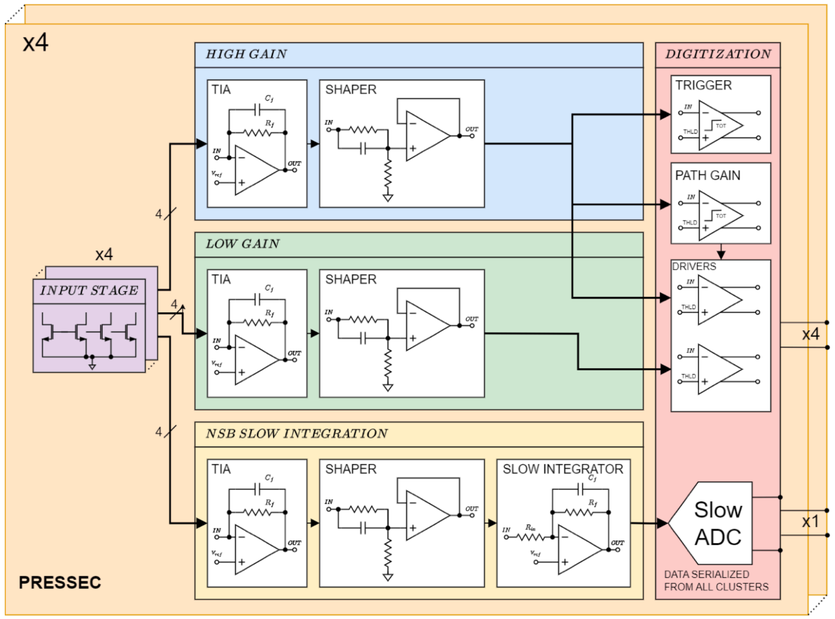
- One prototype ASIC (FANATIC) submitted in October to test the output drivers design
  - Swiss companies involved for chip packaging (Altatec, Hybrid SA)

- Active collaboration to integrate all blocks into a single ASIC (PRESSEC)



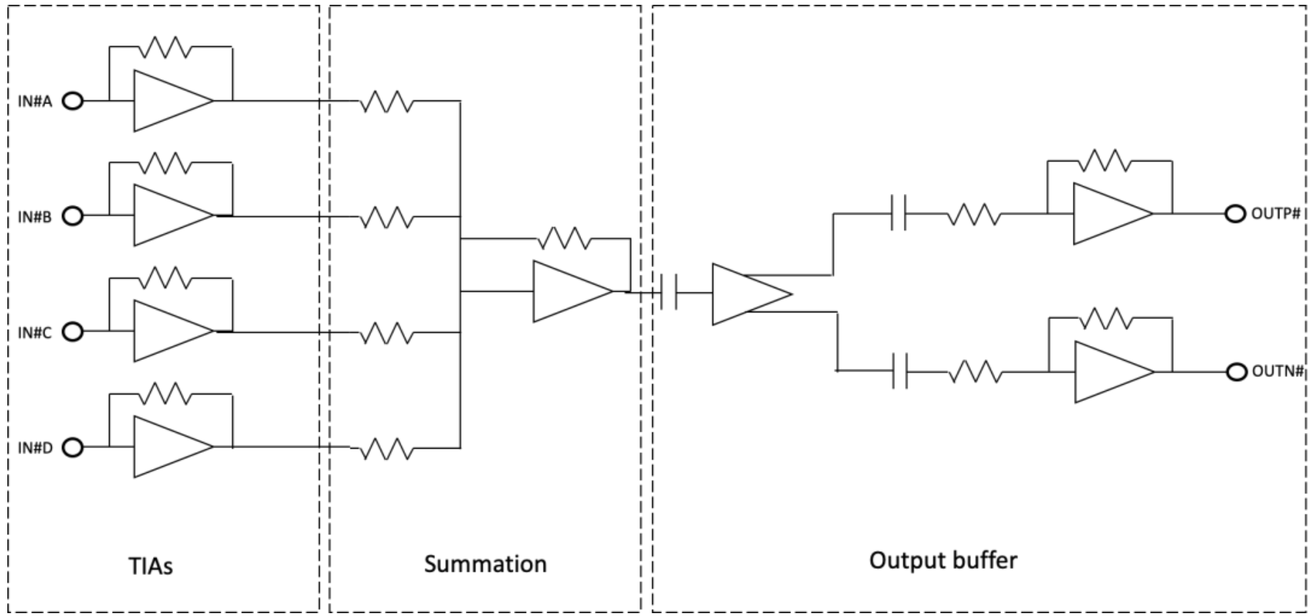
PRESSEC ASIC

Preamplifier **R**eadout **E**lectronics for **S**umming **S**iPMs **E**nhanced **C**ircuit



FANATIC ASIC

Fast **ANA**log **T**ransimpedance amplifier **I**ntegrated **C**ircuit



L. Giangrande (UNIGE), D. Gascón, R. Manera (UB), P.Altet, X.Aragones, S. Gómez, D. Mateo (UPC)

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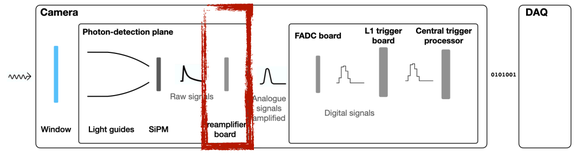

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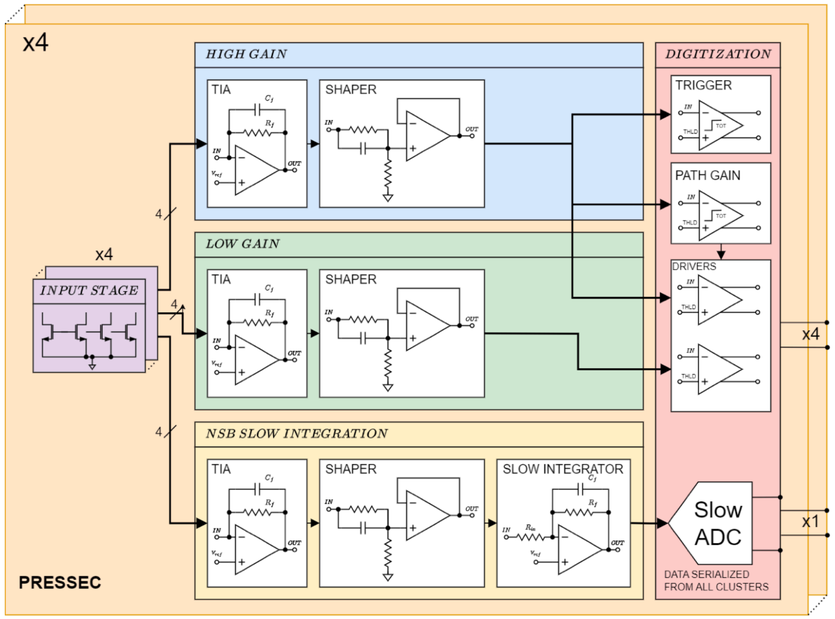

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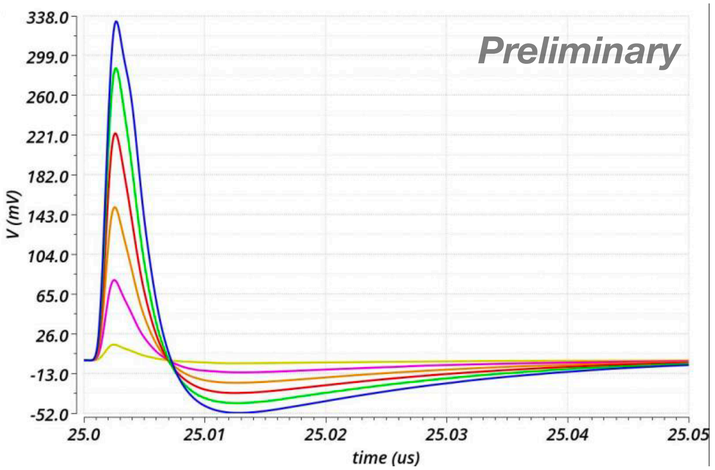

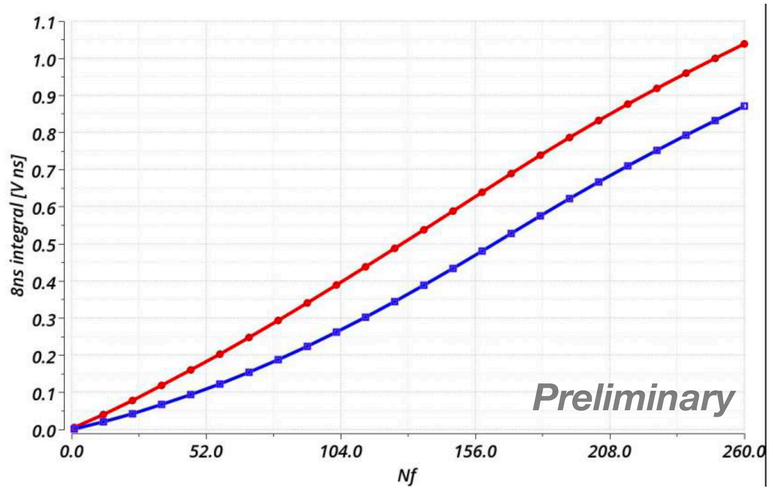

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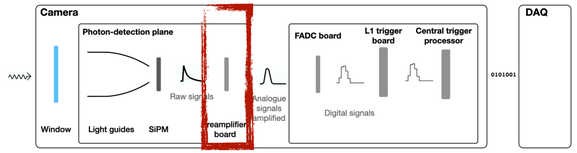

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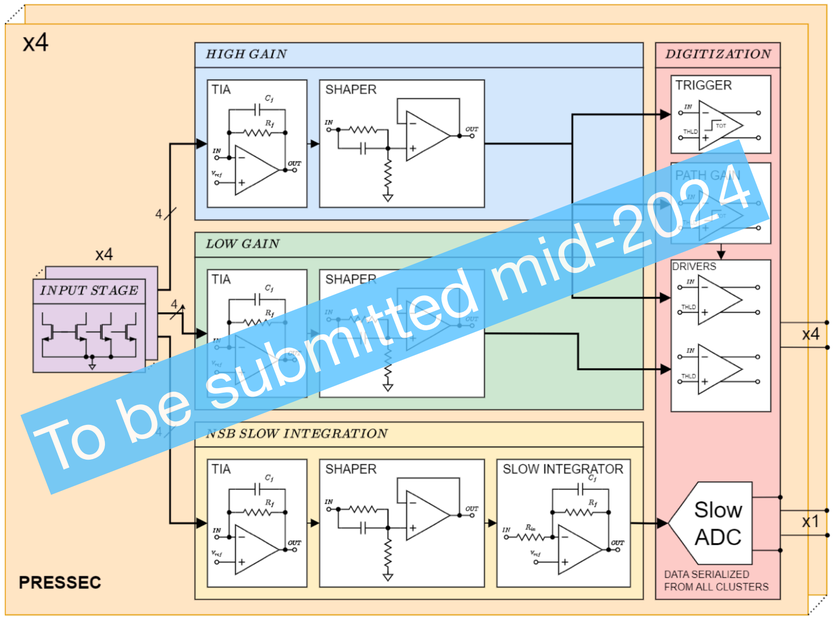

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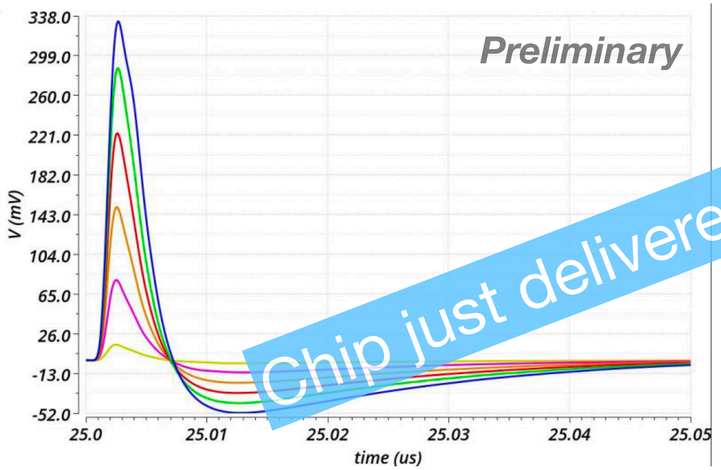
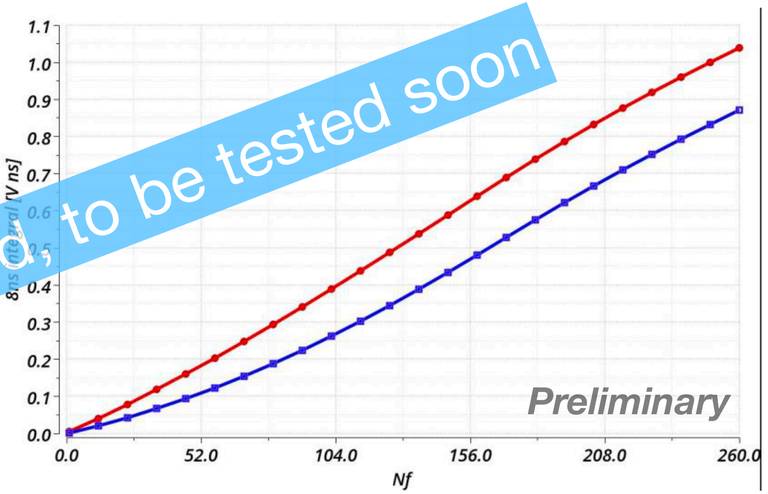




To be submitted mid-2024

Chip just delivered, to be tested soon

FADC ASIC

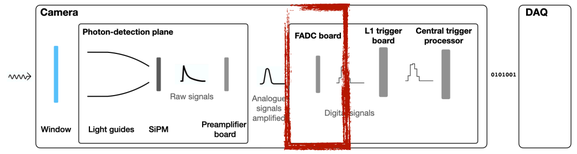
- Digital acquisition requirements:
  - ✦ Power consumption per pixel: 200 mW
  - ✦ Effective resolution (ENOB): 10 bits
  - ✦ Sampling rate: 0.8-1 GSps

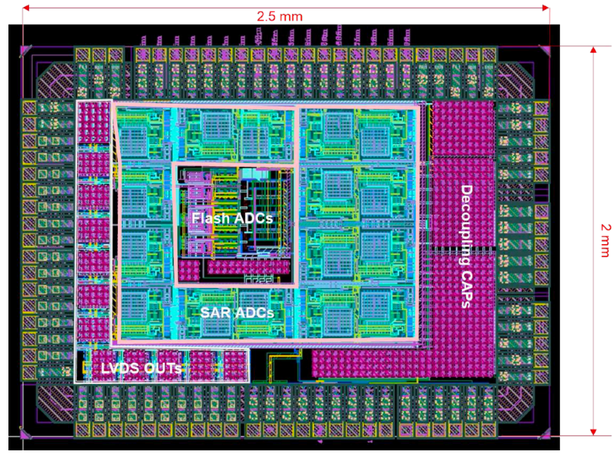
- 3 stages pipeline ADC topology:
  - ✦ 3bit FLASH
  - ✦ 3x (3bit FLASH)
  - ✦ 16x (6bit SAR)

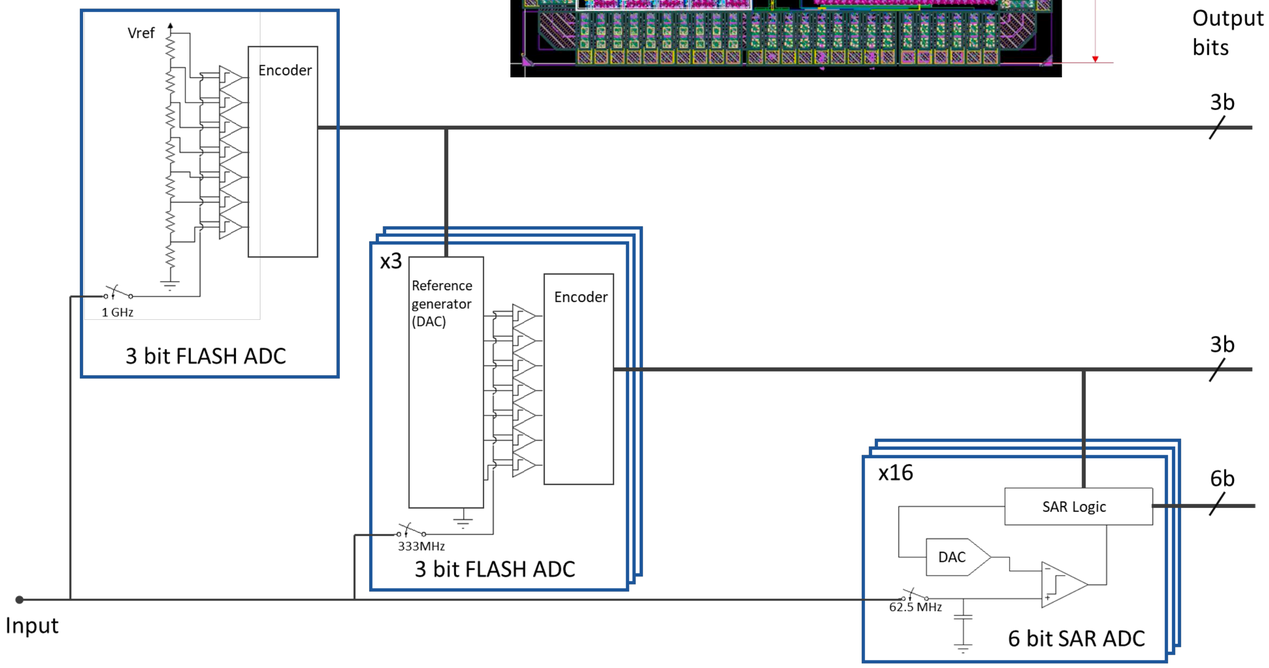
- Output data delivered in parallel by 12 LVDS drivers

- Post layout simulation indicate performance within specifications

- Swiss companies involved in packaging of the chip







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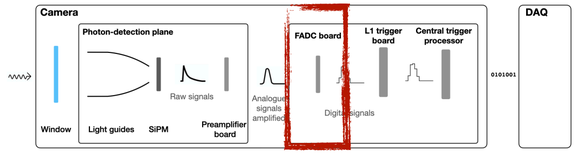
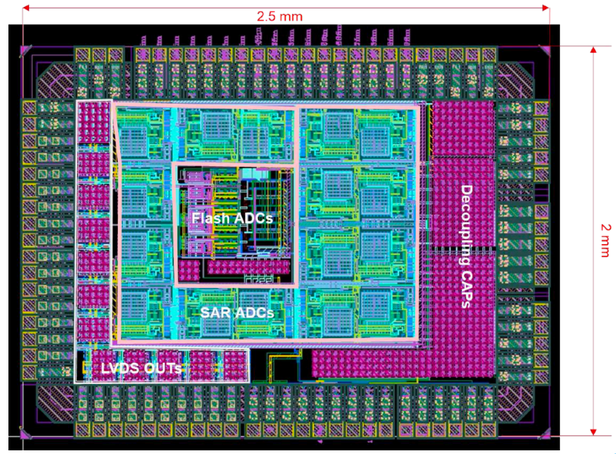
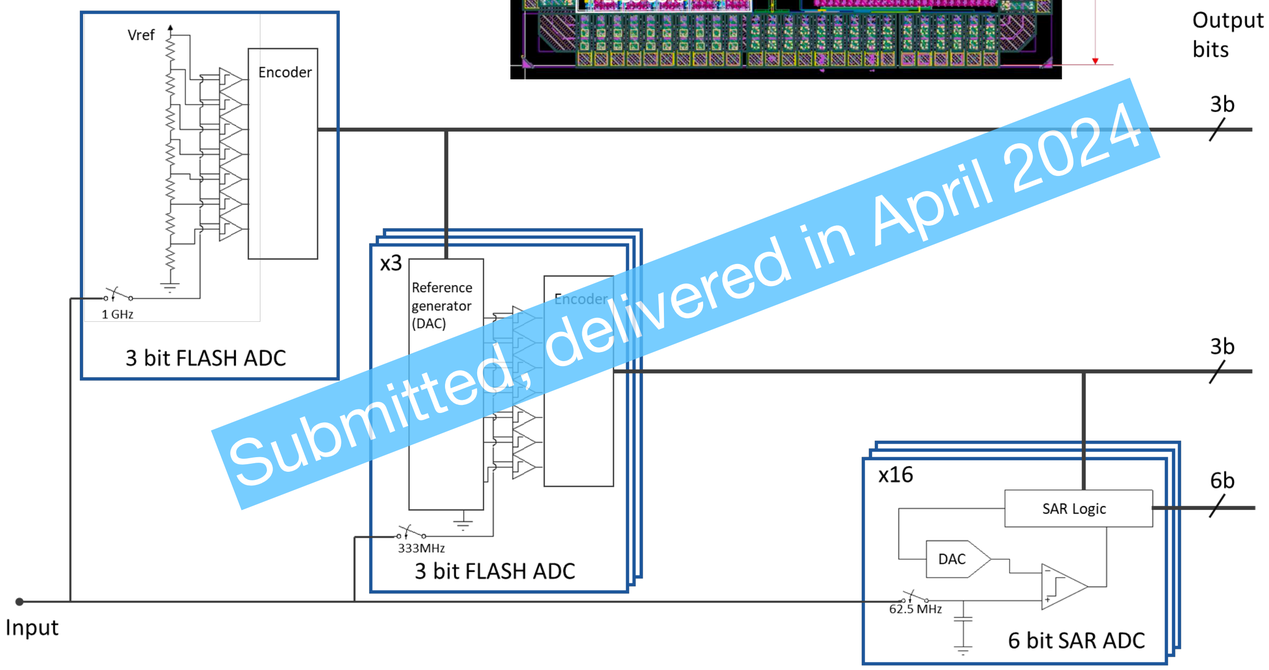






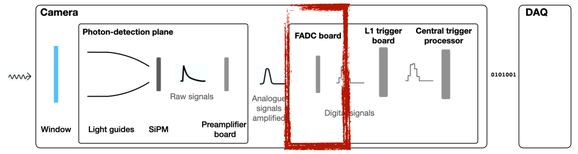
Submitted, delivered in April 2024

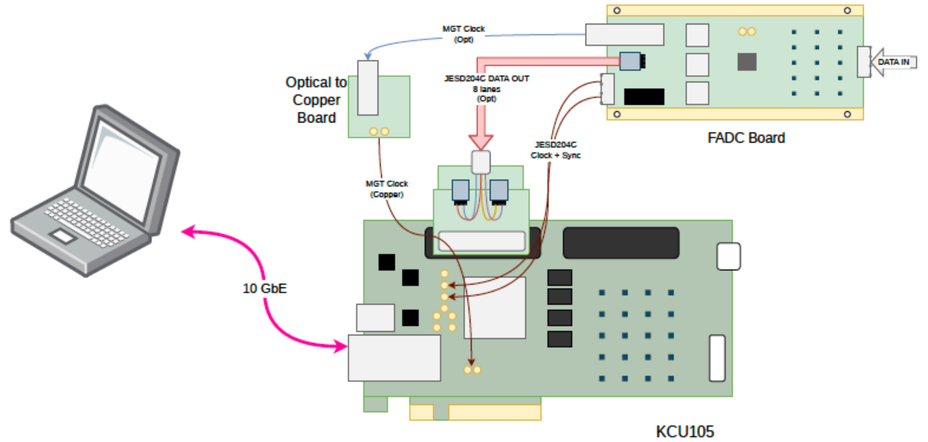
FADC board

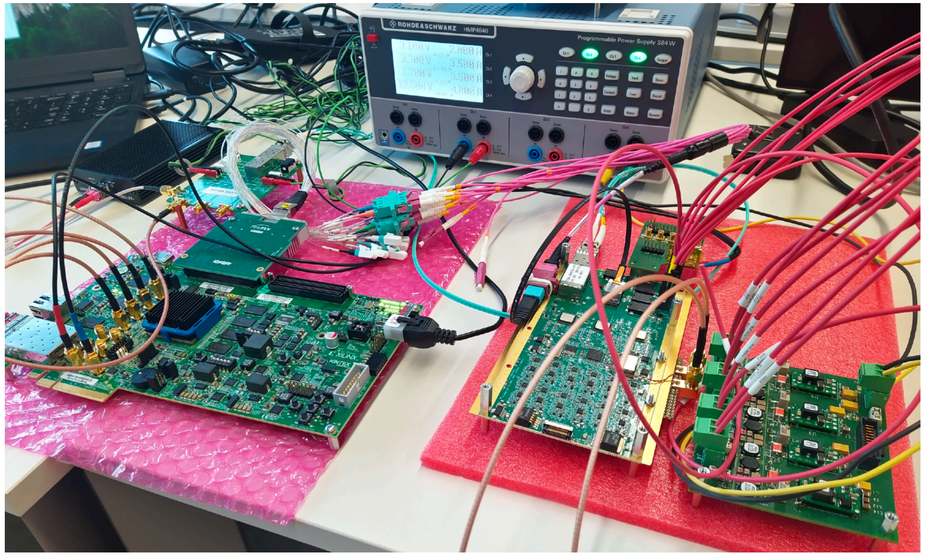
- Functionalities:
  - Manage operation and synchronisation of FADCs
  - Forward FADC continuous data stream to Optical links

- Specifications:
  - **Readout: 9 bits, 1 Gps**
  - **12 input channels** per board (3 ADC09QJ1300)
  - 1 LMK04828 to supply sampling clock and synchronization signals
  - Input clock from SFP or local oscillator
  - Firefly connection @ 12 Gbps for data transport to backend
  - JESD204C protocol

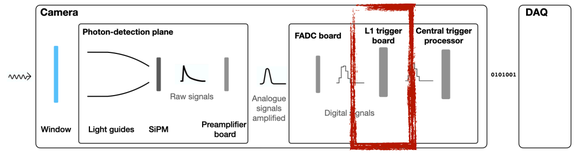
- Status:
  - ADCs and PLL correctly configured via SPI
    - 8 bit @ 1 Gsps (soon 9 bit)
  - JESD204C links locked for all lanes
  - **Data successfully acquired on PC via 10 GbE for all links !**







L1 board

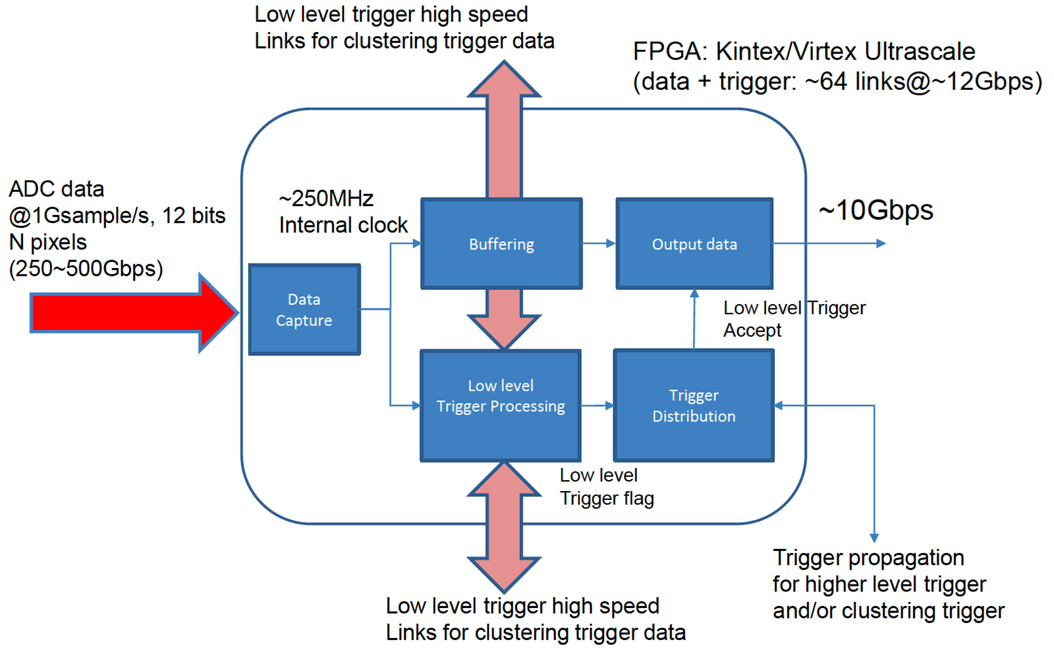


- Functionalities:
  - ✦ **Capture and buffer FADC stream**
  - ✦ Perform **low level trigger** (see L. Burmistrov's talk)
  - ✦ Send to Central Trigger Processor only "triggered events"

- Proof-of-concept test bench being setup, only control software remains to be developed:
  - ✦ Two sets of 4 channel commercial modules (Kintex KCU105, ADC12QJ1600EVM)
  - ✦ Arbitrary waveform generator
  - ✦ High performance scope

- Focus on **firmware development** related to data capture, i.e. implementation of JESD204C protocol

- First power estimate is **25 W per board**

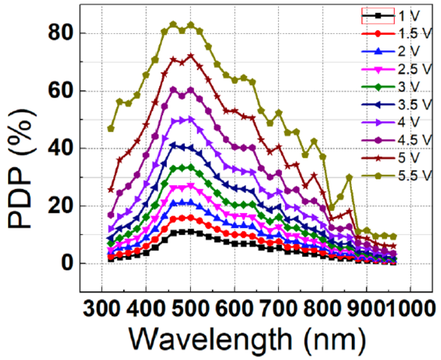


The future: all-in-one

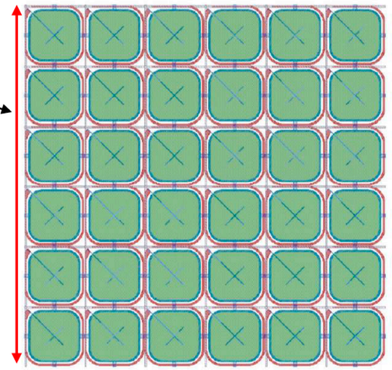
EPFL AQUA
ETHZ

UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

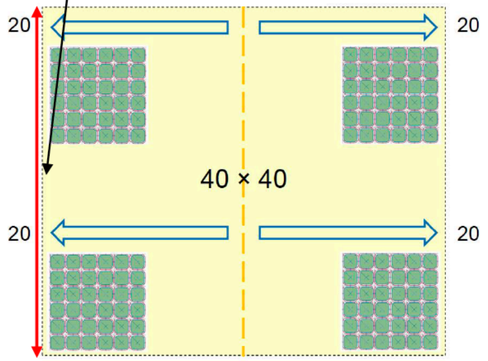
SPAD
- aqua SPAD #31
- PDP = [10, 35]% @ [320, 500]nm @ 3.3V excess bias

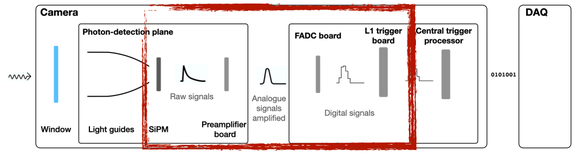


CHANNEL
- 6 × 6 Quad SPAD
- Side = 216 µm
- Fill factor **FF** = 47 %
- **PDE**
  = FF × PDP
  = 5 ÷ 16 %



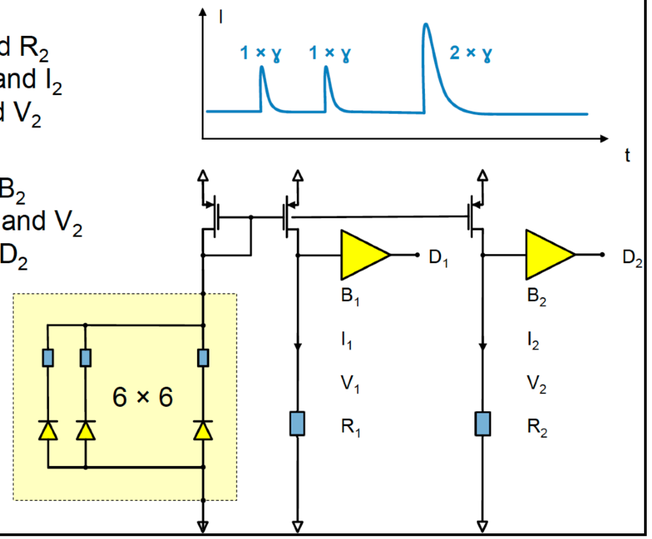
PIXEL
- 40 × 40 = 1'600 channels
- Side = 8,64 mm
- Total area = 74,65 mm²





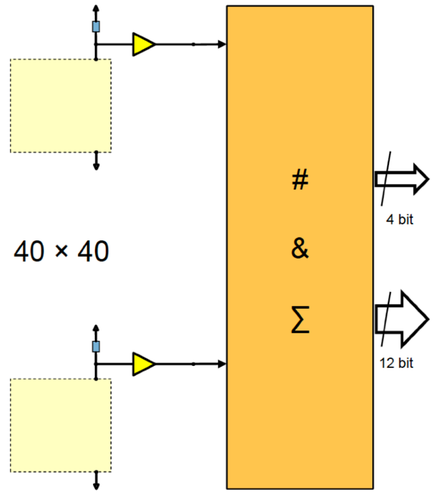
Comparator

- The resistors R_1 and R_2 convert currents I_1 and I_2 into voltages V_1 and V_2
- The buffers B_1 and B_2 digitize voltages V_1 and V_2 into signals D_1 and D_2

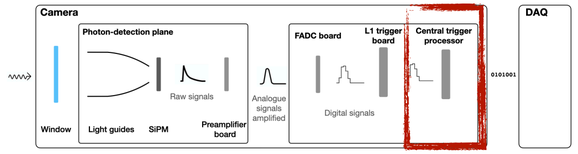


Architecture

- The comparator outputs are counted (#) and summed (∑)
- A binary tree adder implements the summing
- A 4 bit bus outputs the result every 4 ns (L0 trigger)
- A 12 bit bus outputs the result on demand (L1 trigger)



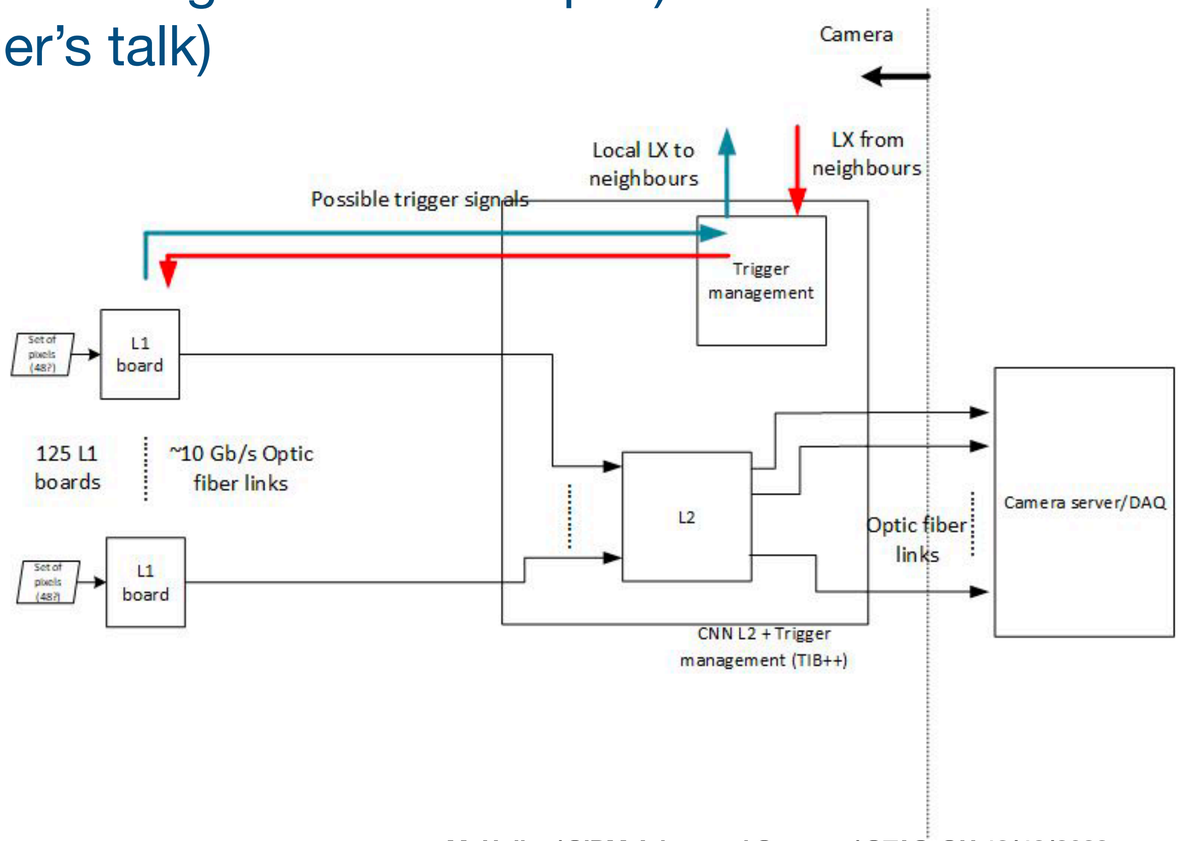
Central Trigger Processor board



- Functionalities:
  - ✦ Collect data from events passing L1 trigger condition
  - ✦ Perform **partial event building**
  - ✦ Manage trigger hardware triggers (optical link with neighbour telescopes)
  - ✦ **Level 2 trigger** with AI algorithms (see T. Miener's talk)

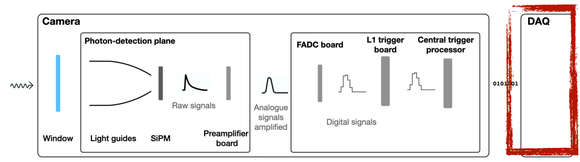
- Short term plans:
  - ✦ Firmware core and algorithmic test bench
  - ✦ Manufacture PCB to test optical transceivers with a FPGA

- First board power estimate ~17 W



Data Acquisition and Advanced Trigger

UZH
UNIGE



- Functionalities:
  - ✦ Assemble events from all telescopes
  - ✦ Perform **stereo software trigger** and potential data volume reduction (gamma/hadron separation)

- See Tjark's Miener talk for network developments toward application to trigger

- Final hardware not identified, but:
  - ✦ The DAQ will rely on an **Intel-based FPGA** network card (e.g. PCIe400)
  - ✦ **Intel is supporting the development**, unique use case with "small" images but very high event rate
  - ✦ Porting algorithms to FPGA requires adaptations (Pruning, quantisation, etc..)
    - ◉ Mainly two different software tools available: Olverlay AI suite (Intel), HLS4ML (CERN)

- **Connection with Swiss industries** for tailored network card development and for firmware development:
  - ✦ Enclustra as principal contact

- **Collaboration between UNIGE and HEPIA on:**
  - ✦ Artificial intelligence network development
  - ✦ DAQ firmware development

C. Abellan Betetan, I. Bezshyiko, G. Hijano Mendizabal (UZH), T. Miener (UNIGE)

M2TECH Project

Second attempt at INFRA-TECH call

- Many benefit for the advanced SiPM camera:
  - ✦ Consolidation of the R&D program:
    - ◉ Combine ASIC for improved power consumption and performance
    - ◉ Generalise the design to the so-called “FlexiTile" to make the other research infrastructure benefit from
  - ✦ Important funds for European collaborators (Spain, Italy, France)
  - ✦ LST know-how will be injected in M2TECH for high return
  - ✦ Current status (to be validated):
    - ◉ About 40 FTEs requested
    - ◉ Additional funds for R&D

Programme: Horizon Europe (HORIZON)

Work programme: Research Infrastructures 2023-2024 (Introduction p.6)

Destination (context): Next generation of scientific instrumentation, tools and methods and advanced digital solutions (INFRATECH, Work programme p.103)

Call for proposals: R&D for the next generation of scientific instrumentation, tools, methods, solutions for RI upgrade (HORIZON-INFRA-2024-TECH-01-01, Work programme p.108)

Type d’action: HORIZON Research and Innovation Actions (RIA)

Granting Authority: European Commission

Call opening date: **6 December 2023**

Call deadline for submission: **12 March 2024**

Budget for the call: 62 M€
Budget per project: 5-10M€
Indicative nbr of grants: 7

C. Richard (LAPP)

Research Infrastructures involved:
CTAO, LST, MAGIC, ET, VIGO, KM3NeT

Conclusion

- Continuously growing **Swiss and international community** working on the development of the advanced SiPM cameras
- All aspect of the developments covered or to be covered very soon
- Current funds only cover R&D phase
  - ✦ Will suffice to build few elementary blocks of the camera, but …
  - ✦ … success of additional fund requests required to maintain the development pace