The monolithic ASIC for the high precision preshower detector of the FASER experiment at the LHC

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Outline

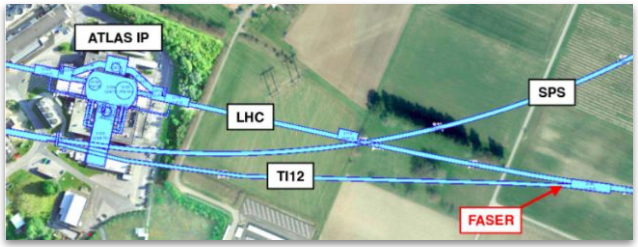
- The FASER experiment
- The new preshower detector
- Final detector ASIC
- Pre-production detector ASIC
- Tests & Results of the final ASIC
- Conclusions

First phase of installation of FASER in the LHC tunnel

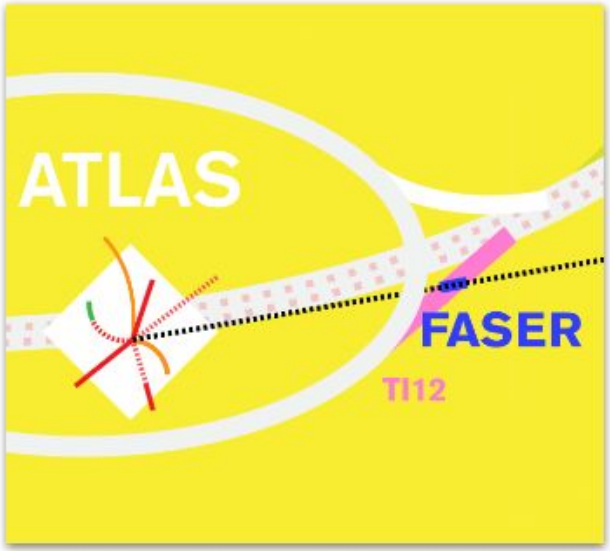
FASER & the upgrade of the preshower detector

The FASER experiment at the LHC

- First operation Run 3!
- Location: 480 m from the ATLAS Experiment
- Designed to search for long-lived particles (LLP) produced at the LHC
- LLPs pass through the LHC infrastructure/rock without interacting and will decay into visible Standard Model particles, detected in ForwArd Search ExpeRiment (FASER)
- Energy scale 100 GeV until few TeV

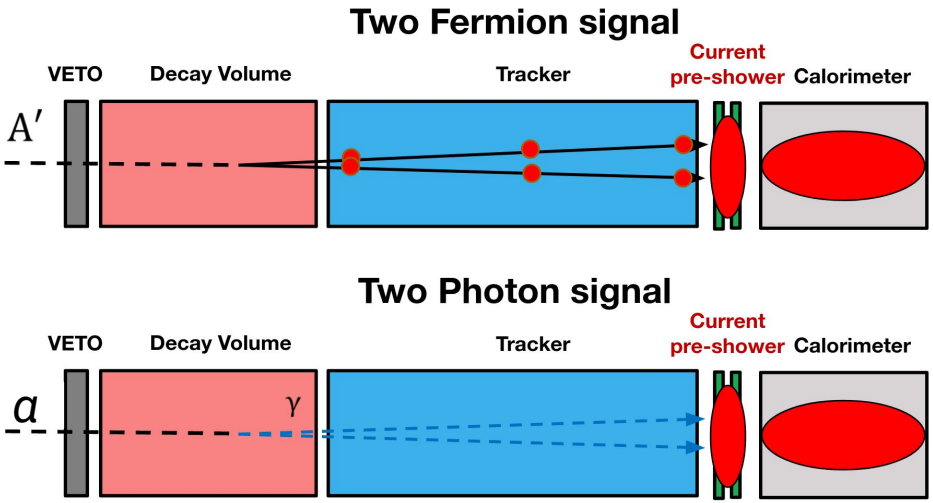


First phase of installation of FASER in the LHC tunnel

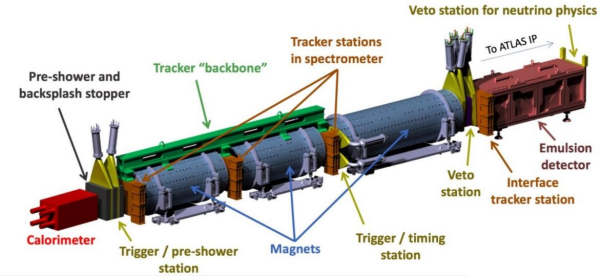


Picture taken from symmetry magazine. Artwork by Sandbox Studio, Chicago with Ana Kova.

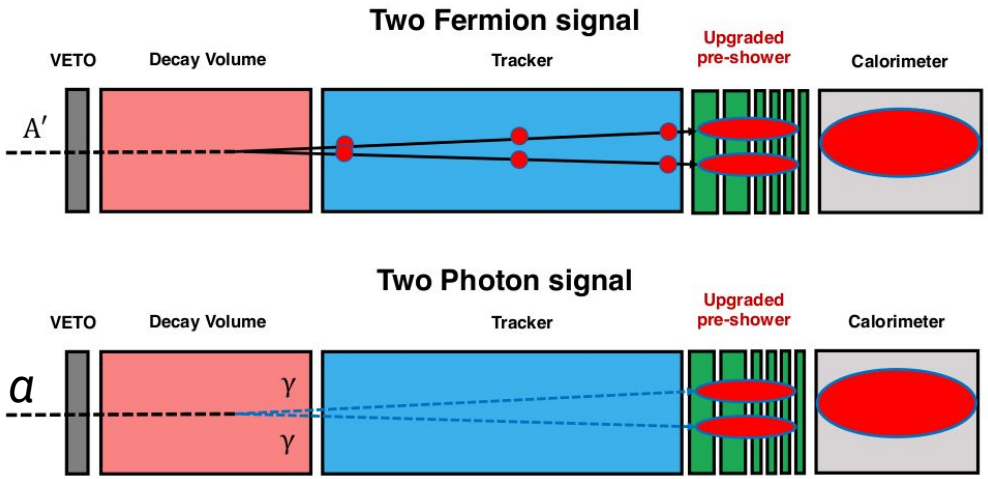
The current preshower detector



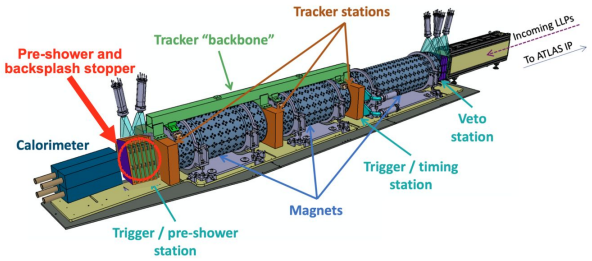
NO XY granularity



The new preshower detector



High Granularity Detector



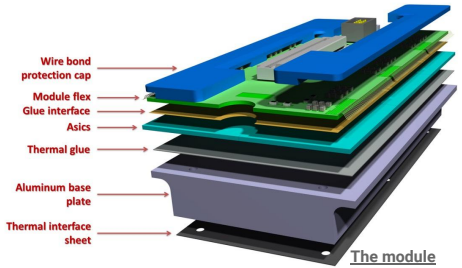
Independent measurement of two very collimated photons

Technical proposal of the new preshower detector of FASER

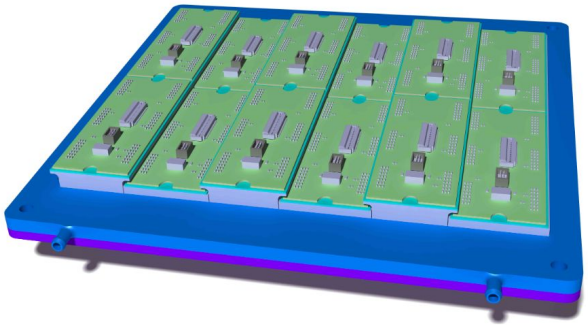
The goal of the new preshower detector

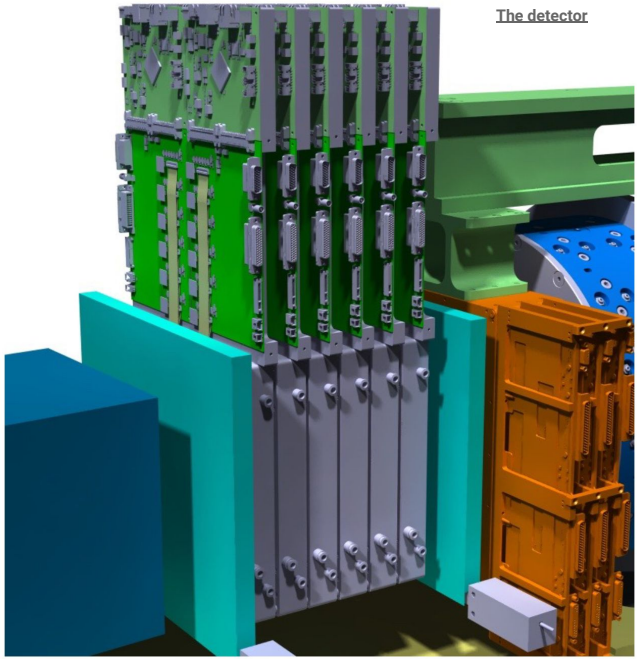
Our signal: 2 photons with **200 μm separation**

- **High granularity** preshower
- **Sample** and **reconstruct** EM shower



The module

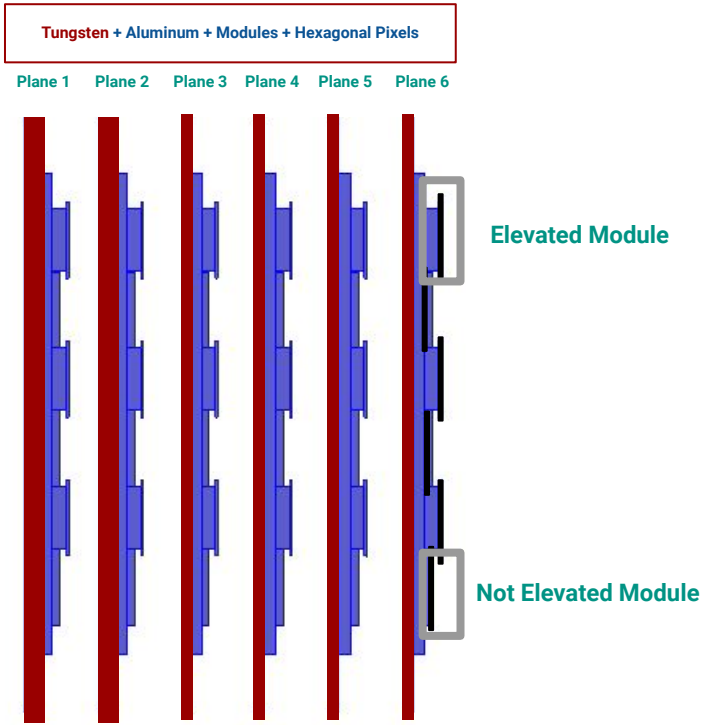

The plane

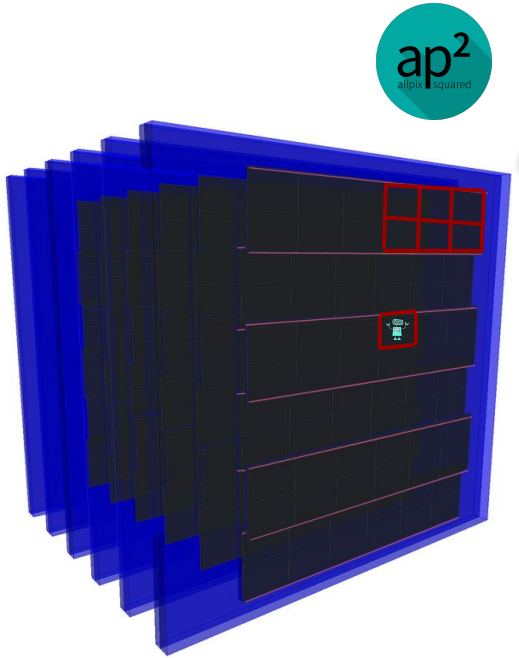

The detector

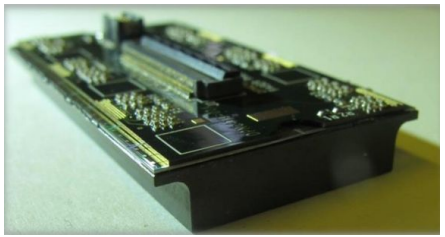
- 6 Layers of silicon planes with tungsten layers in between
- Each silicon plane is divided by 12 modules
- Targeting data taking in 2024/25, during LHC run 3 and during HL-LHC

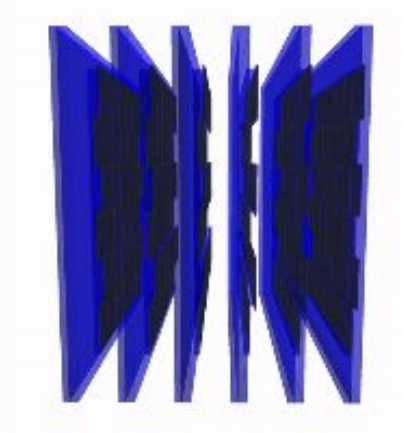
Technical proposal of the new preshower detector of FASER

The new preshower detector: Simulation



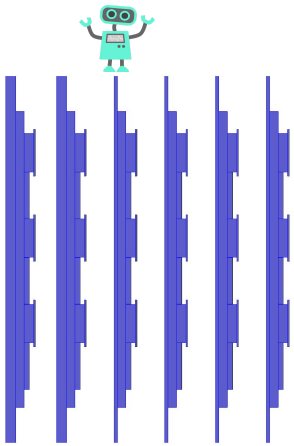






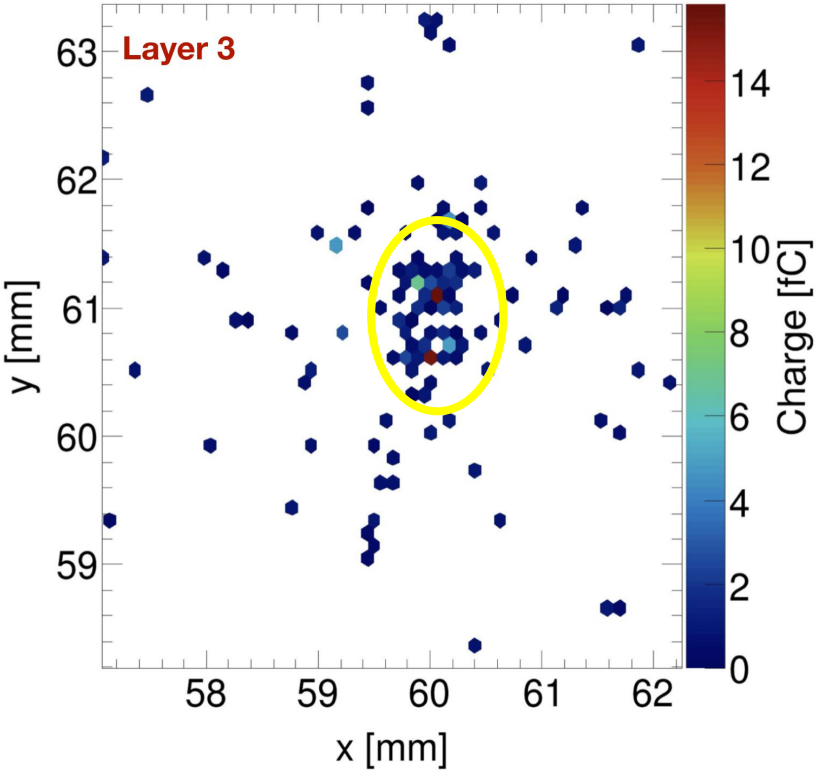
The new preshower detector: Simulation

PLANE 3



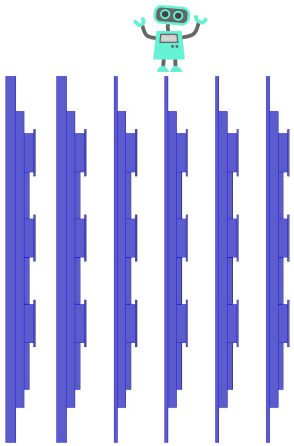
E1= 1 TeV
E2= 1 TeV
d=500um

High dynamic range for charge measurement



The new preshower detector: Simulation

PLANE 4



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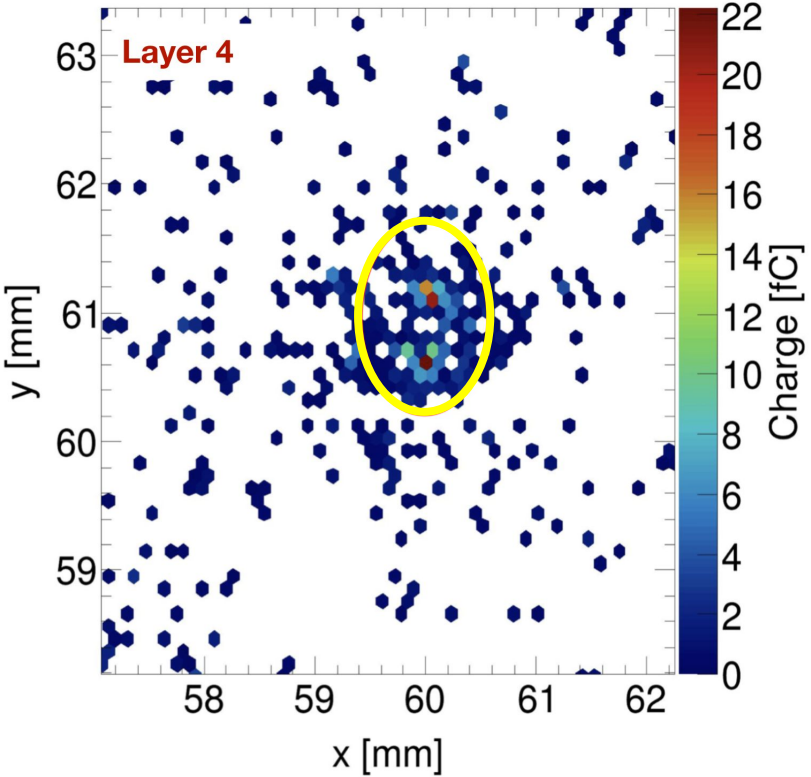
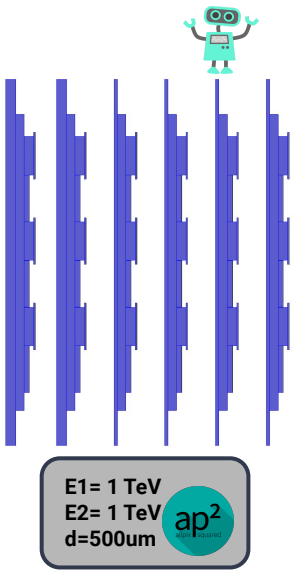
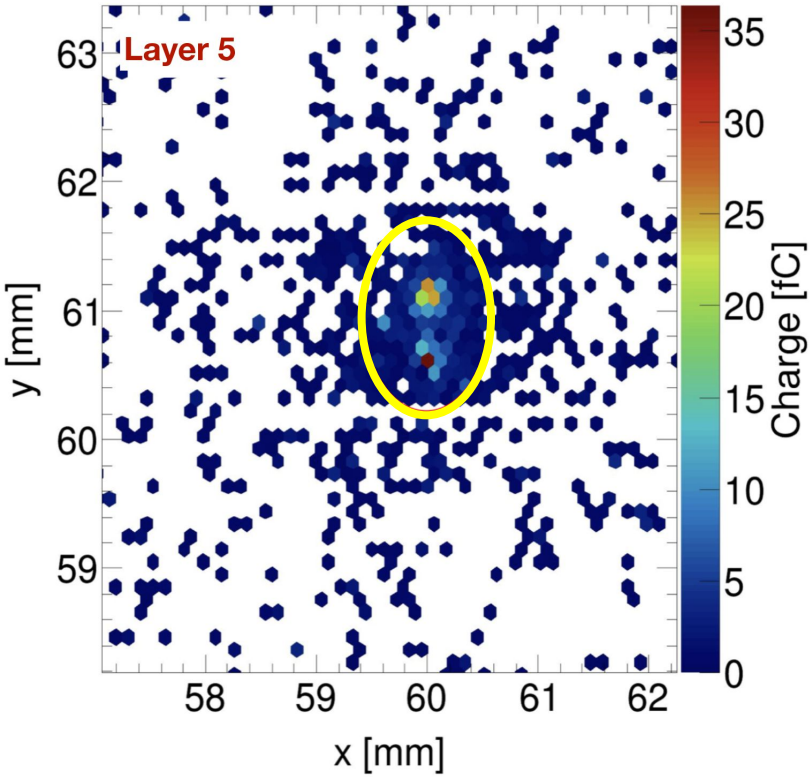


The new preshower detector: Simulation

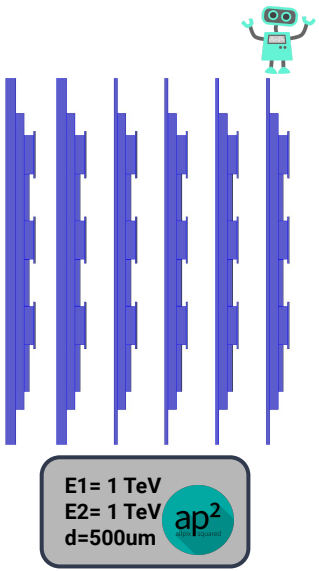
PLANE 5

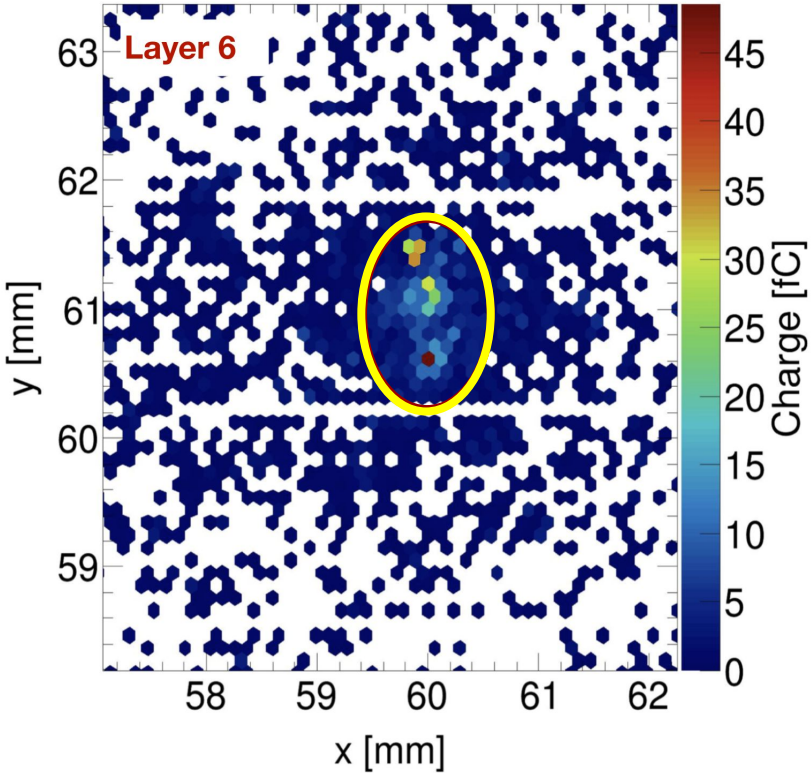




The new preshower detector: Simulation

PLANE 6





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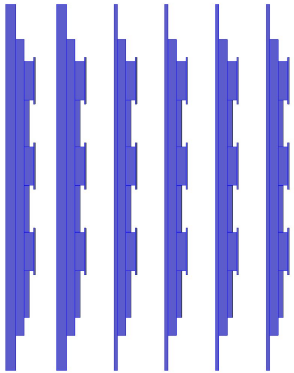

E1= 1 TeV
E2= 1 TeV
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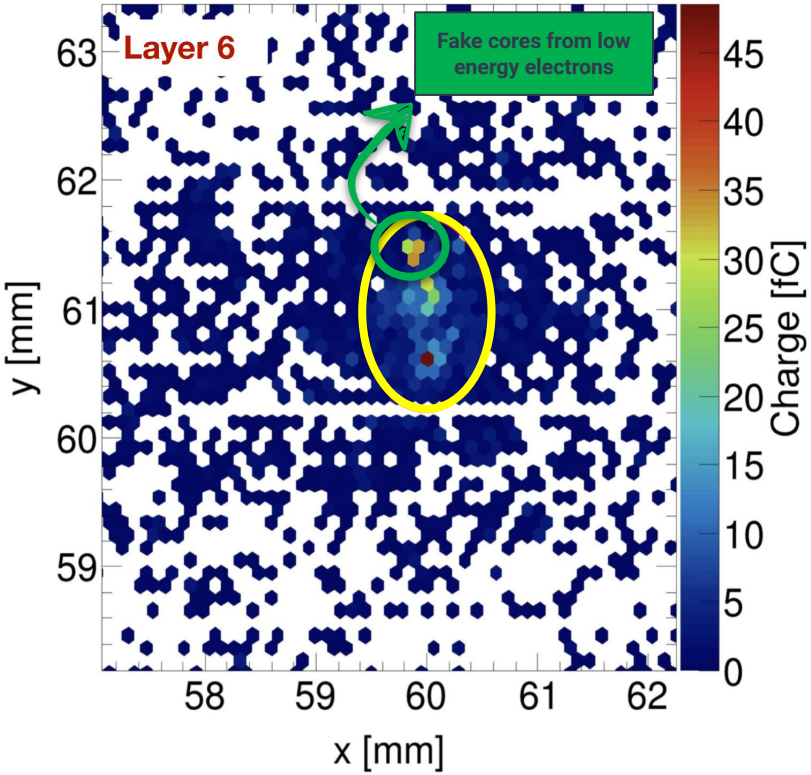
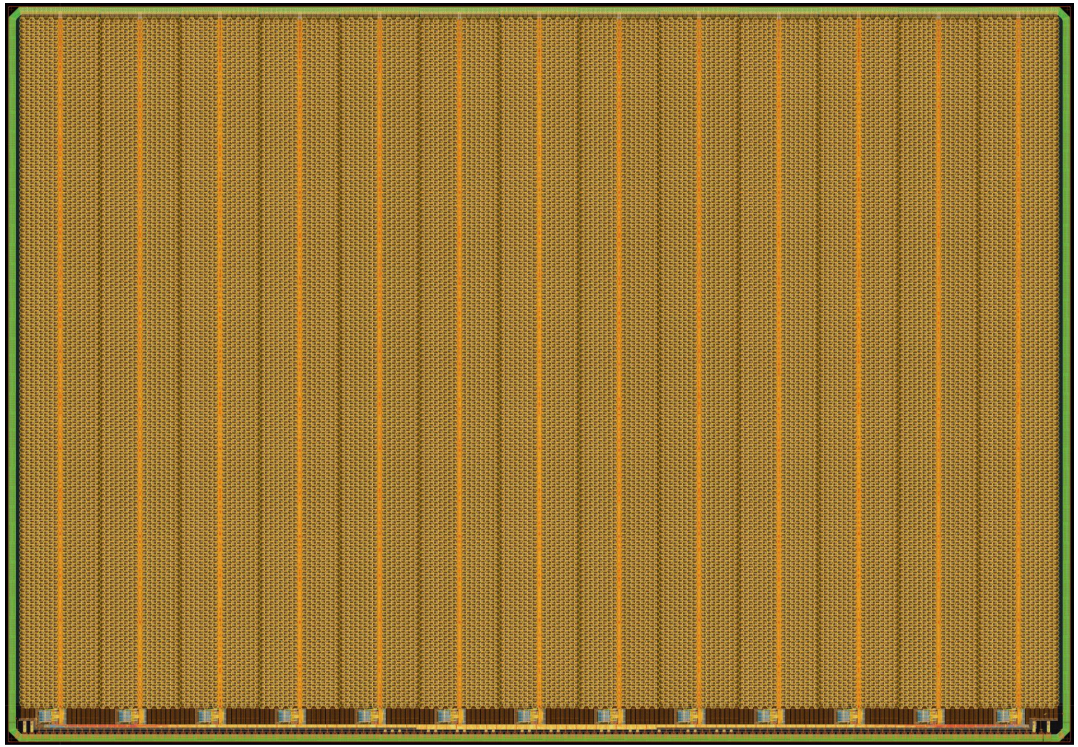
Very large occupancy

Why 6 planes?
Why pixelated sensors?



Production ASIC

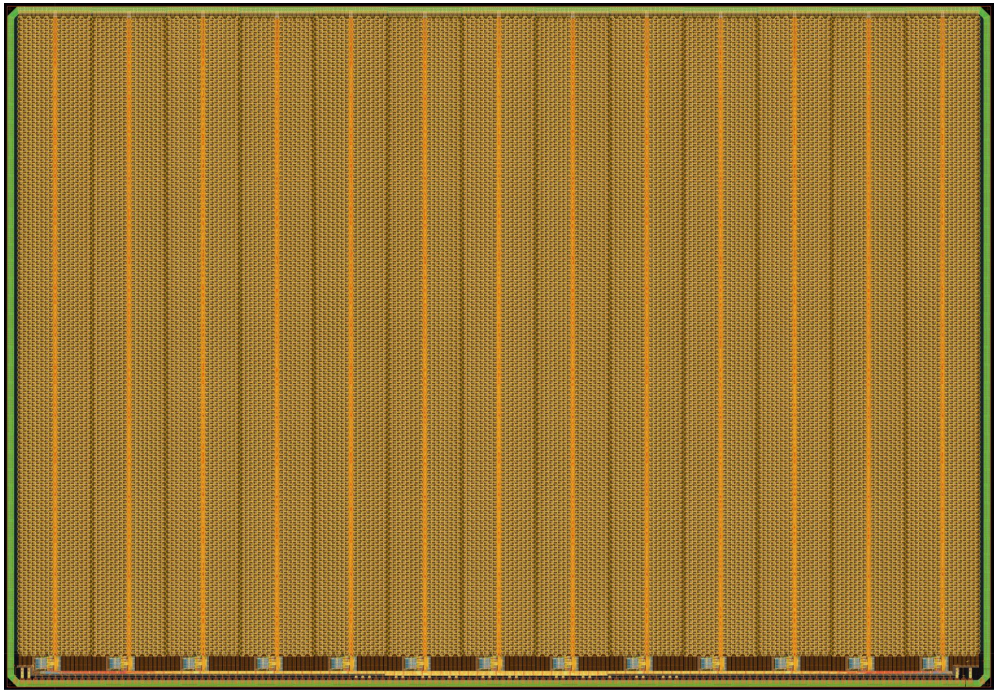
Monolithic ASIC architecture



Received last month!

Monolithic ASIC architecture

- First large-area monolithic detector in SiGe BiCMOS
- Chip size of 2.2 x 1.5 cm^2, with matrix of 208 x 128 pixels (**26’624 total pixels**)



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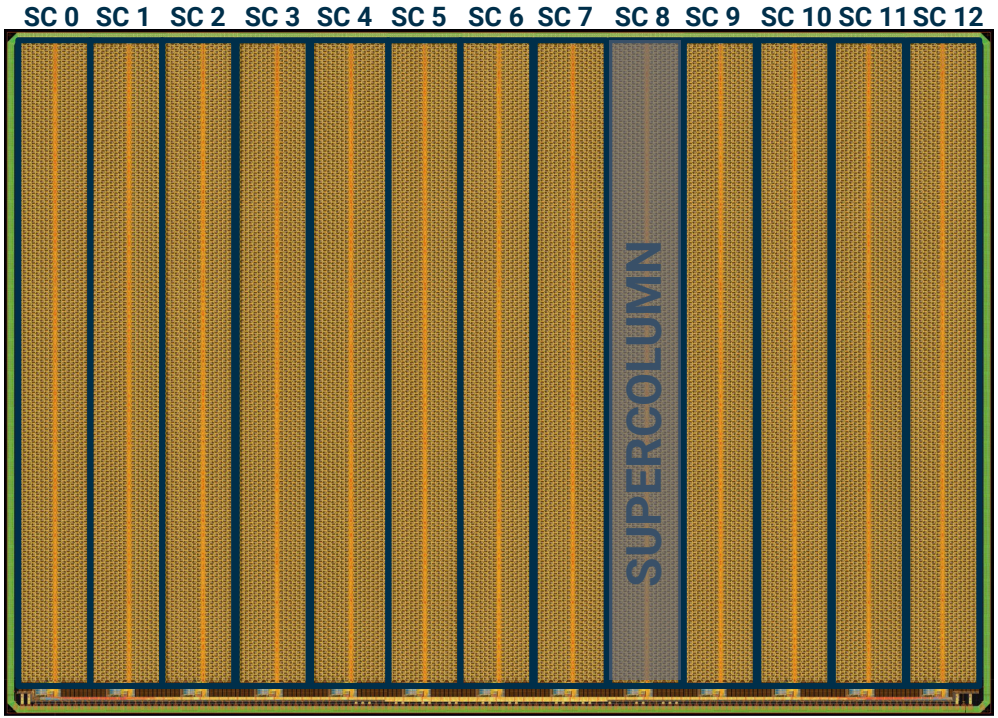
- 13 **Supercolumns** (SC)



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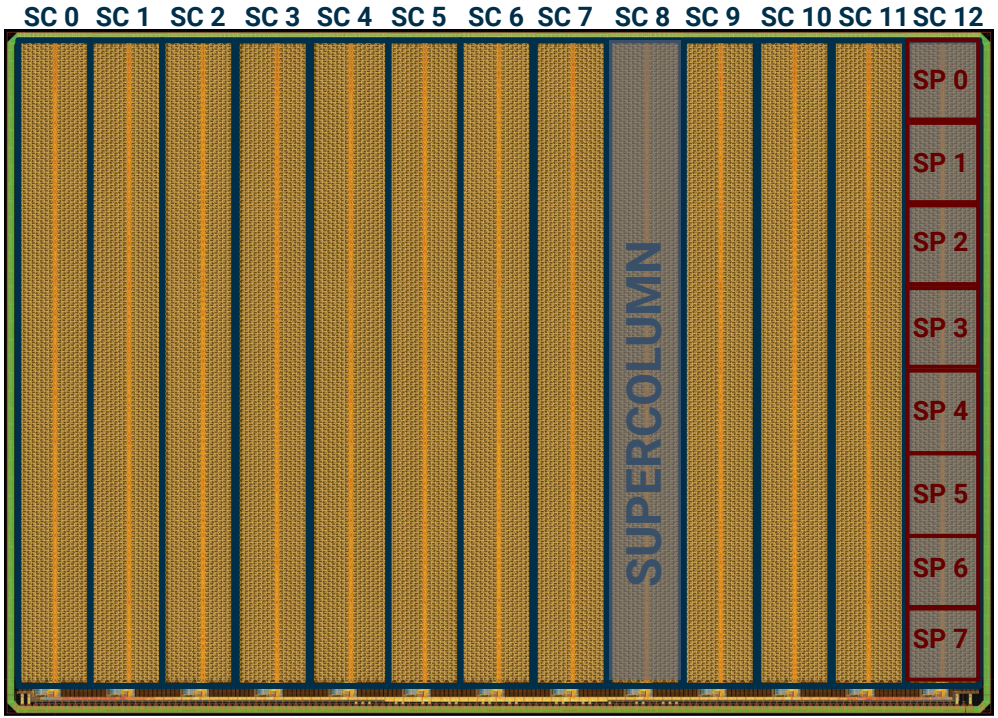
- Each Supercolumn has 8 **Superpixels** (SP)



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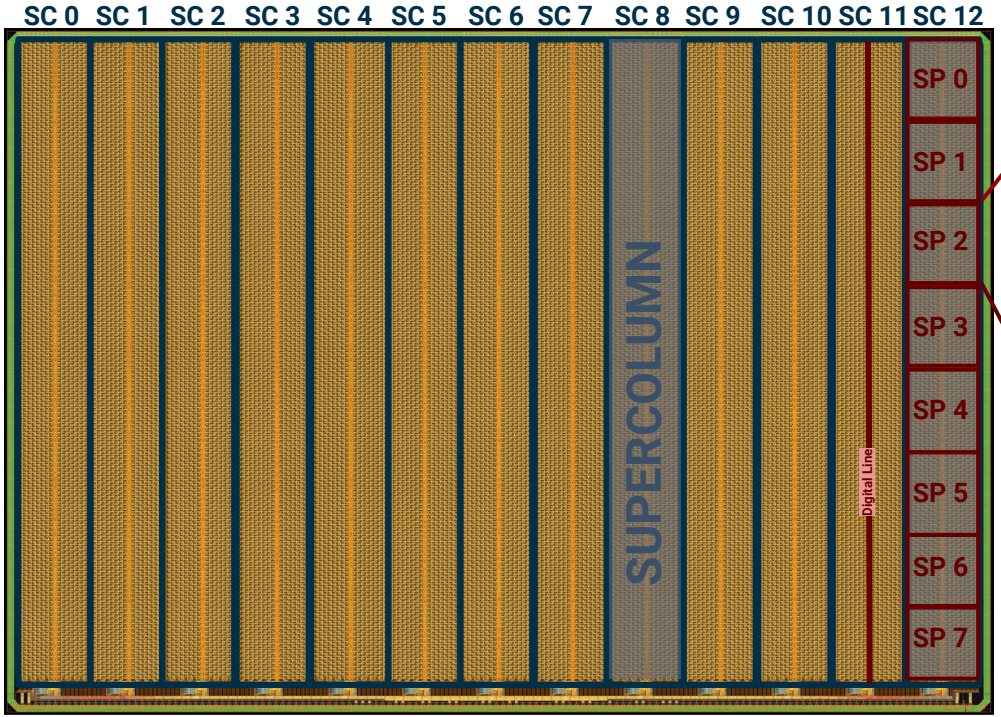
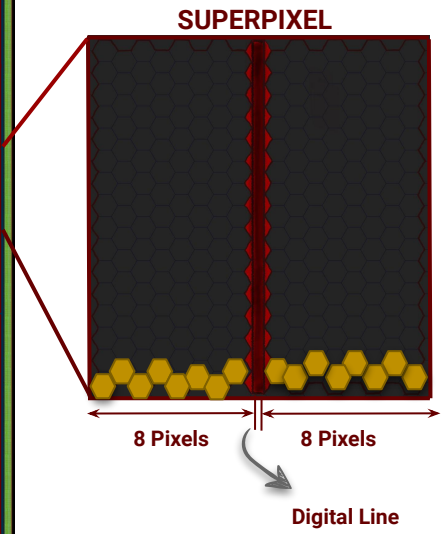
- First large-area monolithic detector in SiGe BiCMOS
- Chip size of 2.2 x 1.5 cm^2, with matrix of 208 x 128 pixels (**26'624 total pixels**)
- 13 **Supercolumns** (SC)
- Each SC has 8 **Superpixels** (SP)
- Each SP has **16x16 pixels**
- 1 **Digital Line** in the middle of each SC





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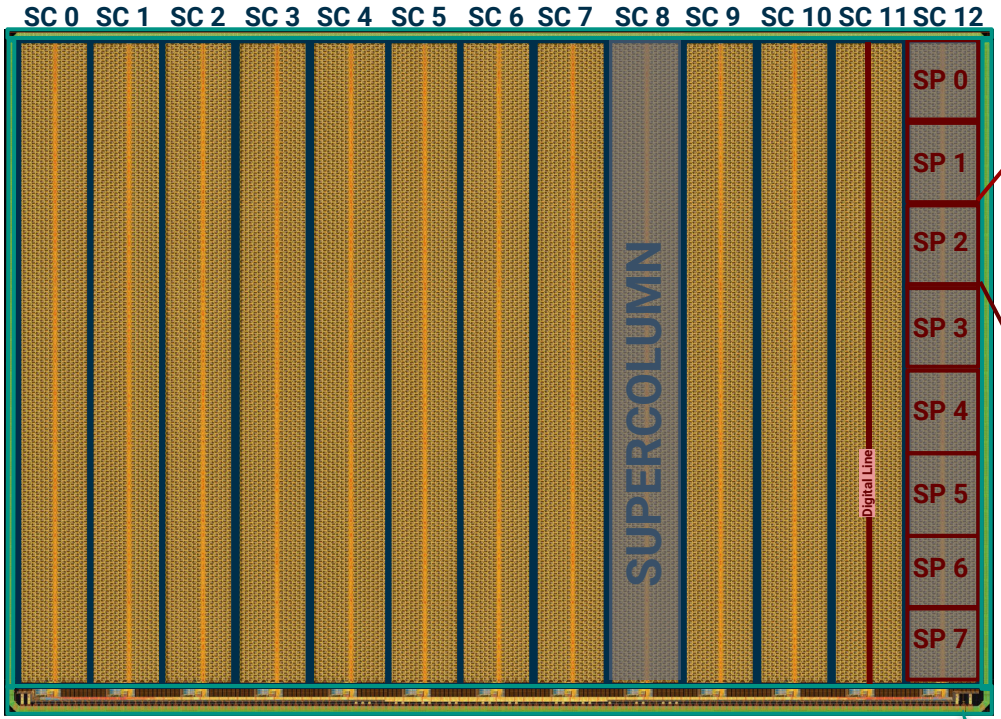
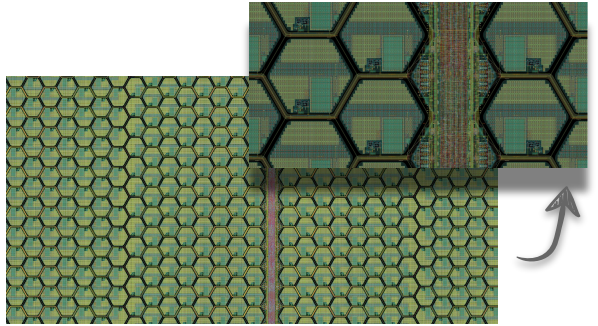
- 13 **Supercolumns** (SC)
- Each SC has 8 **Superpixels** (SP)
- Each SP has **16x16 pixels**
- 1 **Digital Line** in the middle of each SC, in the middle (40 µm width), which is inactive
- Dead are in the **periphery**:
  - 720 µm on the readout side
  - 270 µm on the guard ring sides



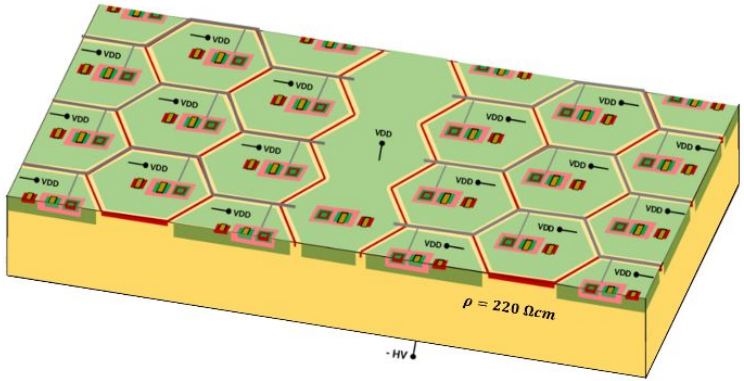
Monolithic ASIC: Sensor

- Monolithic ASIC in 130 nm SiGe BiCMOS technology from IHP microelectronics (design in collaboration between CERN, University of Geneva and KIT)
- The charge needs to be measured for each pixel: acts as an **imaging device**
- **High-resistivity** (220 Ω · cm) substrate, about 130 µm thickness
- Hexagonal pixels integrated as **triple wells**, pixel capacitance of 183 fF



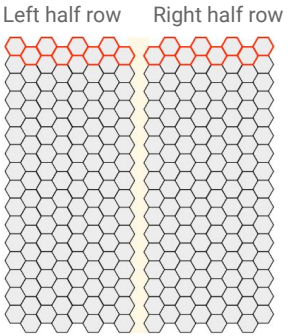
Main Specifications

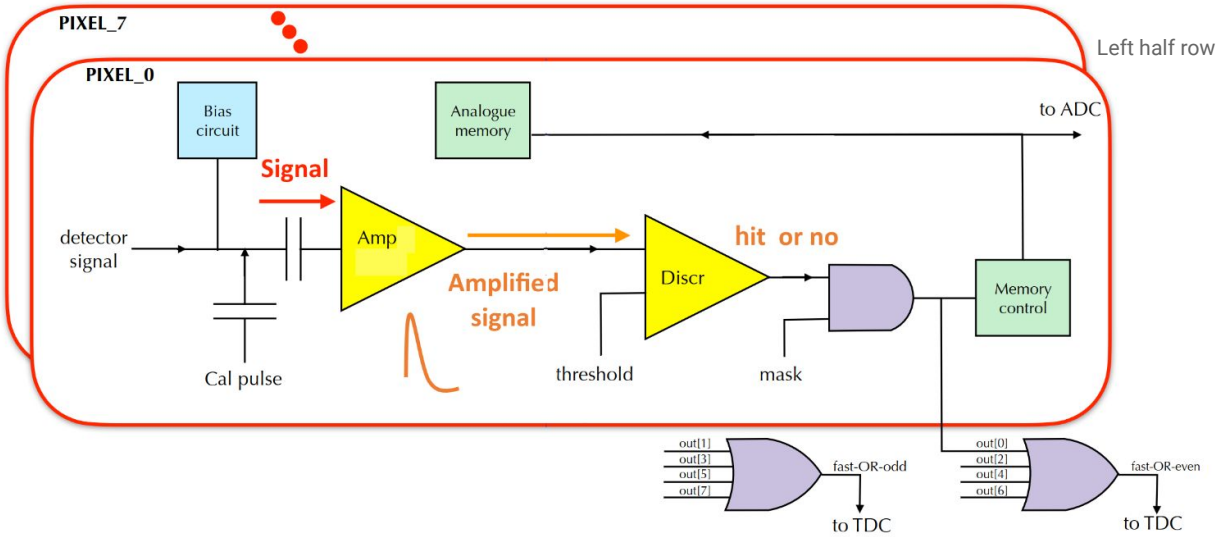
Pixel size	65 um side (hexagonal)
Pixel dynamic range	From 0.5 to 65 fC
Cluster size	O(1000) pixels
Readout time	< 200 µs
Power consumption	< 150 mW/cm^2
Time resolution	<1 ns



Monolithic ASIC architecture: Pixel

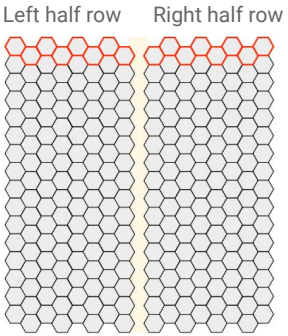
- **Charge measured per-pixel, simultaneously for different superpixels**

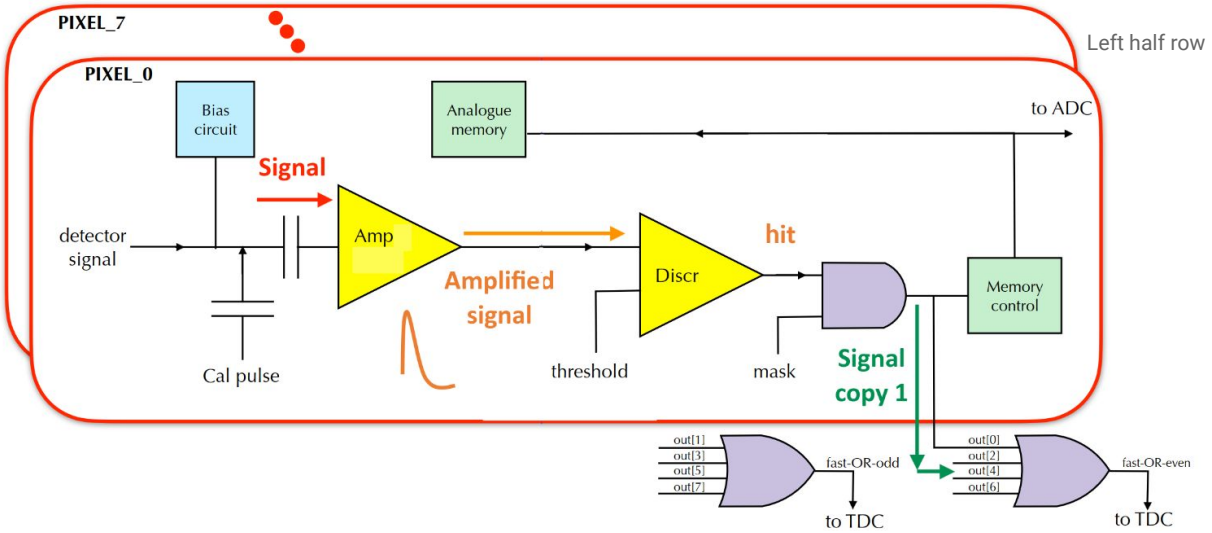




Monolithic ASIC architecture: Pixel

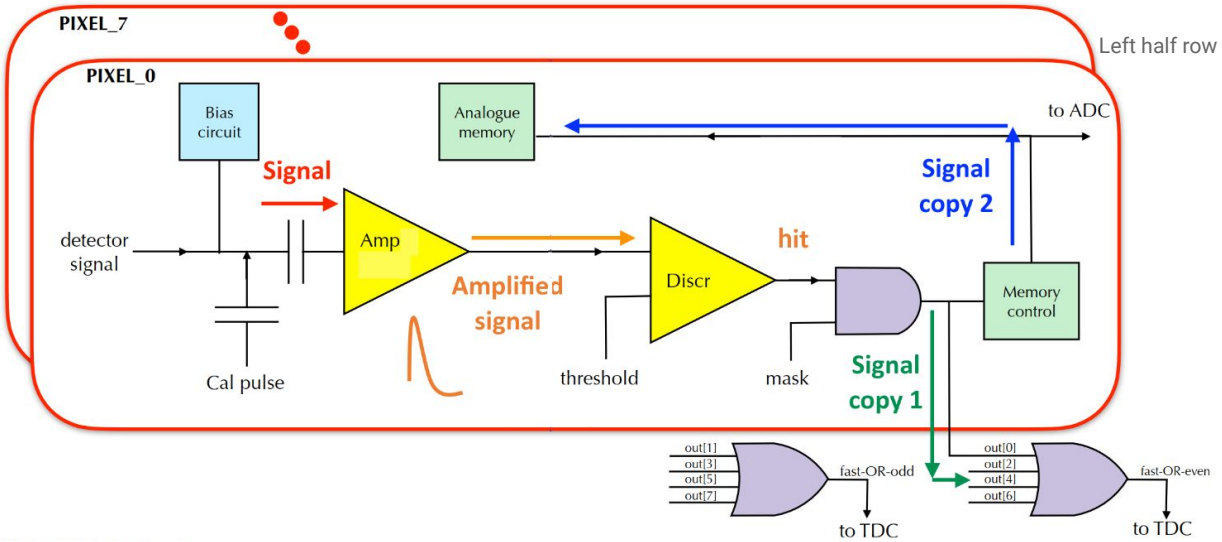
- **Charge measured per-pixel, simultaneously for different superpixels**
  - Hit above threshold generates signal sent to periphery via fast-OR

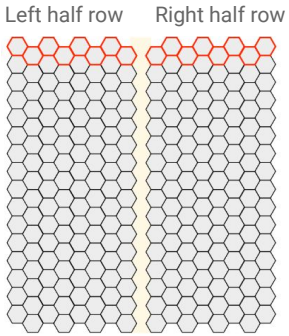




Monolithic ASIC architecture: Pixel

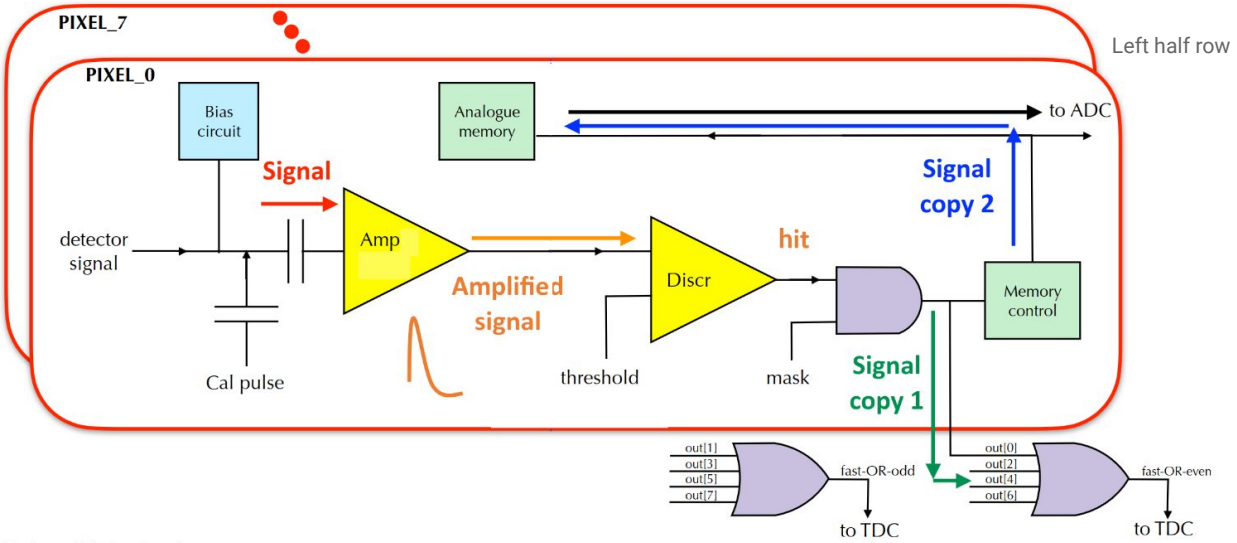
- **Charge measured per-pixel, simultaneously for different superpixels**
  - Hit above threshold generates signal sent to periphery via fast-OR
  - Charge is stored via pixel's analog memory



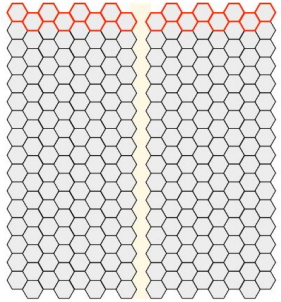


Monolithic ASIC architecture: Pixel

- **Charge measured per-pixel, simultaneously for different superpixels**
  - Hit above threshold generates signal sent to periphery via fast-OR
  - Charge is stored via pixel's analog memory
  - After some delay, readout starts supercolumn after supercolumn



Left half row



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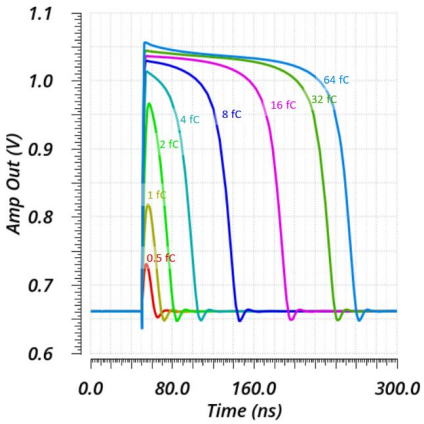
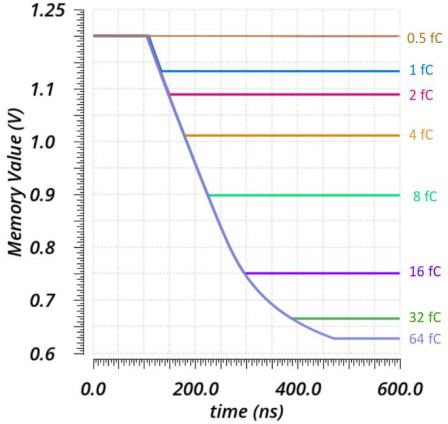
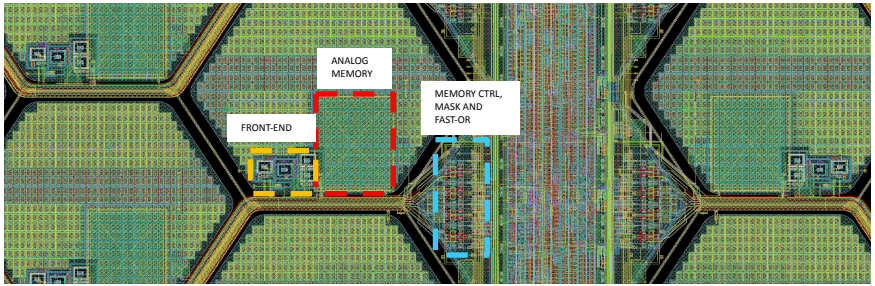
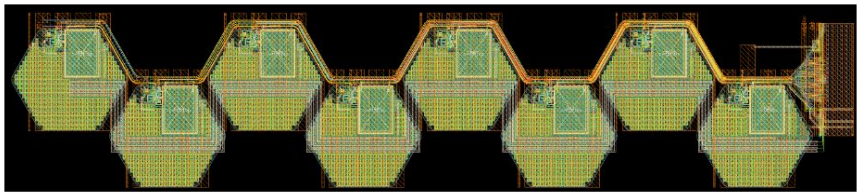




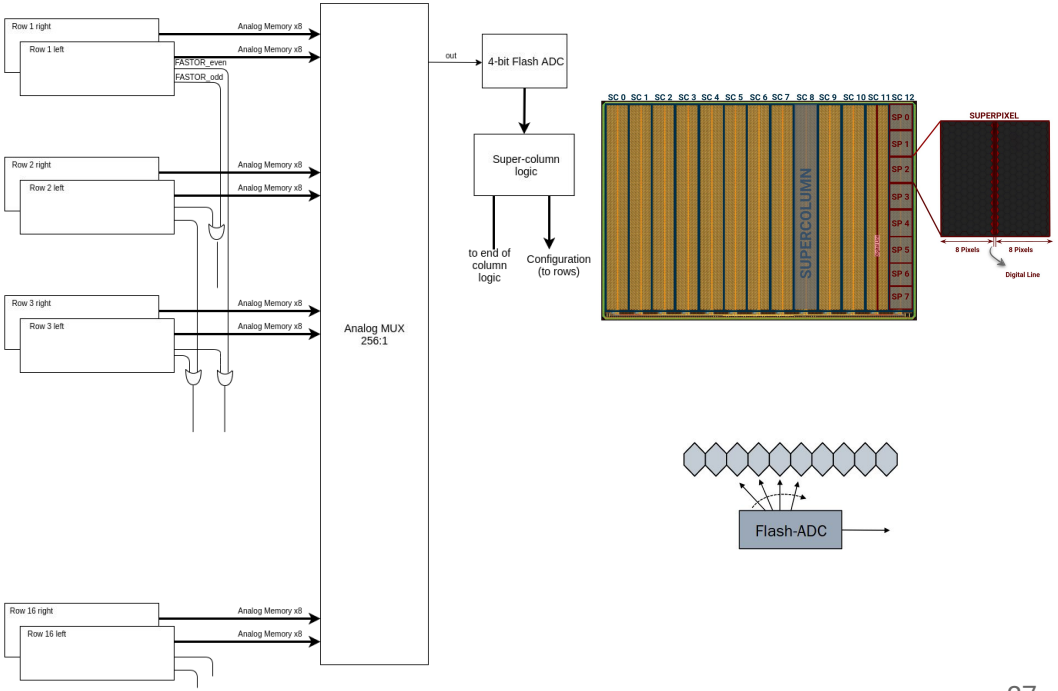




Preamplifier designed to produce a signal proportional to the log of input charge

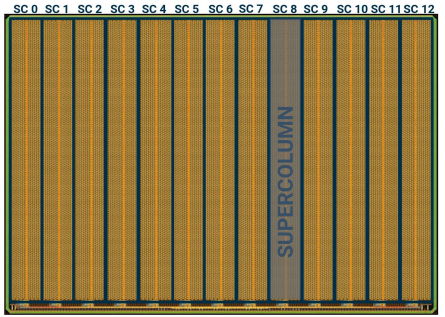
Monolithic ASIC architecture: Super-pixel

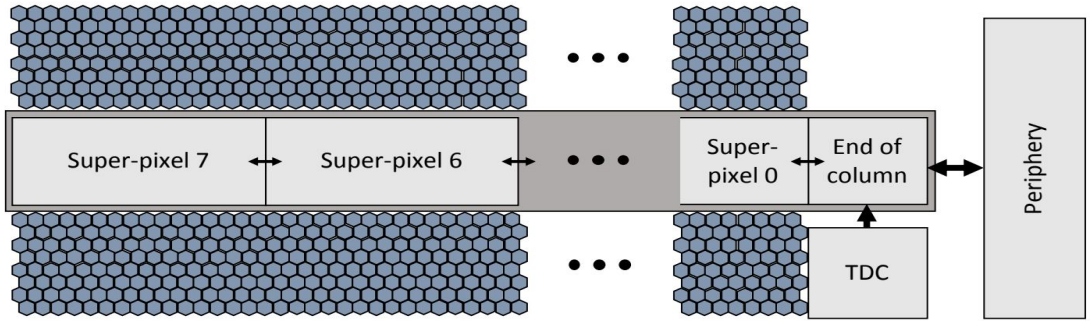
- Data is stored on the capacitor in each pixel and **converted on the fly** with a flash ADC. 256-to-1 MUX
- The capacitor is charged with a constant current during the TOT
- The same ADC will poll all the pixels in a superpixel and convert them as needed



Monolithic ASIC architecture: Super-columns

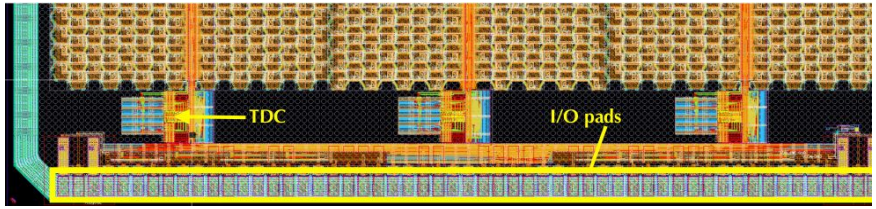
- All the logic is in the supercolumn!
  - Super-column logic: it **masks the pixels, generates the test-pulses,** drives the analog **MUX**, handles **readout** and **communication with periphery**
- Unusual aspect ratio digital line: **1.4 cm by 40 µm**

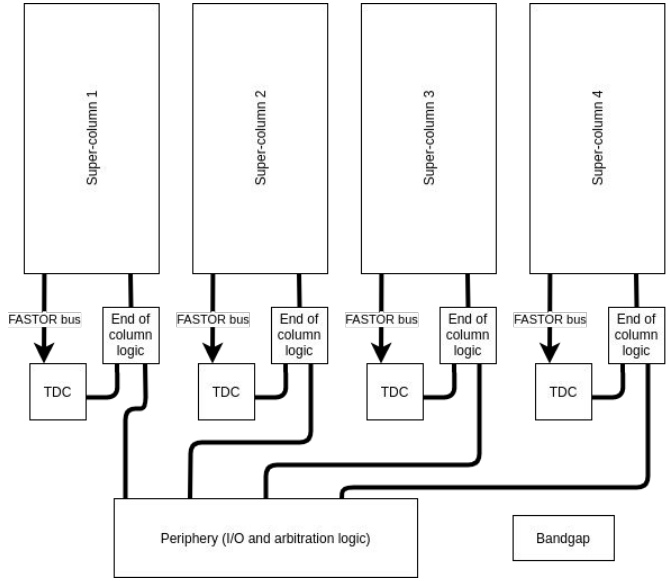




Monolithic ASIC architecture: Periphery and I/O

- The periphery interrogates the super-columns from left to right, and handles the chip I/O
- Two clock domains: 50 MHz (programming phase) and 200 MHz (readout phase)
- **Super-column level frame-based** solution for readout logic in the periphery
- Data are not stored in the chip, but they are sent out on the fly at 200 Mbit/s

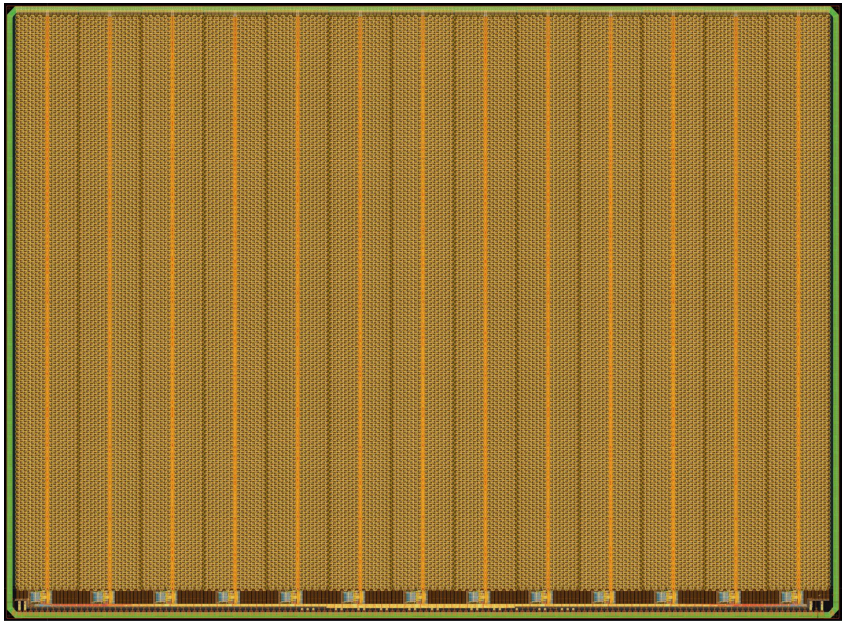




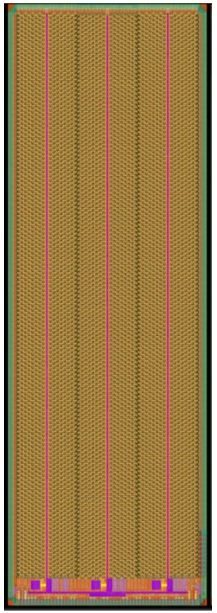
Tests on the pre-production & production ASICs

Production ASIC Vs Pre-production prototype

Production

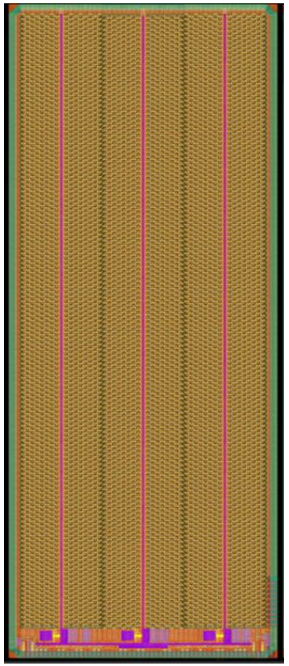


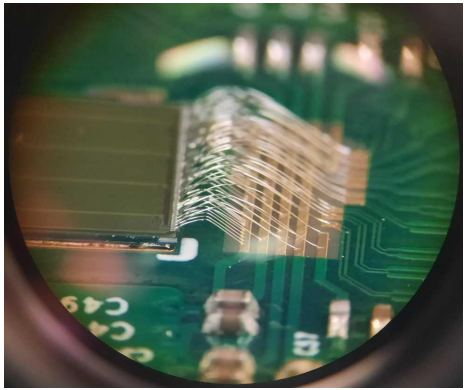
Pre-production

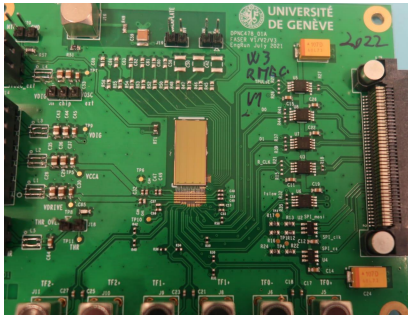


Pre-production prototype & Test on board

- Large area, fully functional prototype
- 128 x 48 pixels, 3 supercolumns
- The circuits work
- The issues were identified and corrected



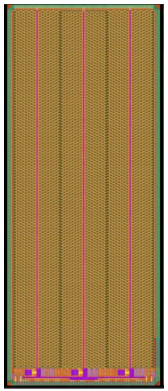




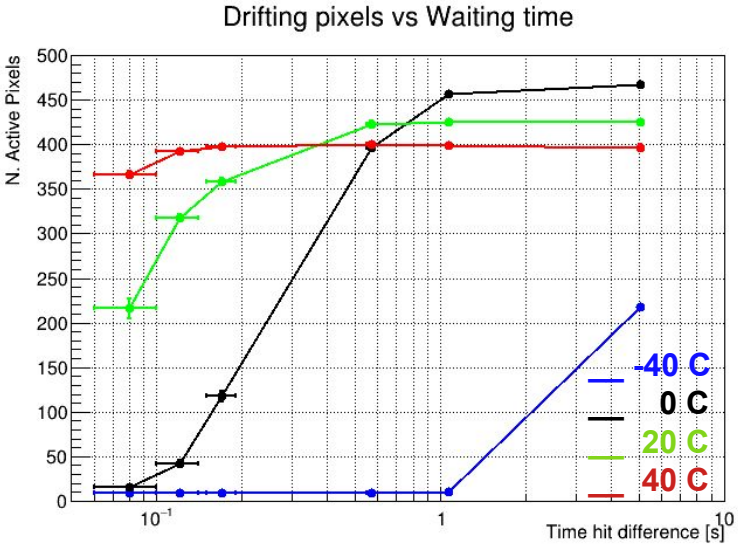
Pre-production ASIC: Memory Drift

Problems Detected

- Memory drift
- Synch digital blocks
- Unable to operate at 200 MHz
- Long calibration methods



Laboratory Measurement

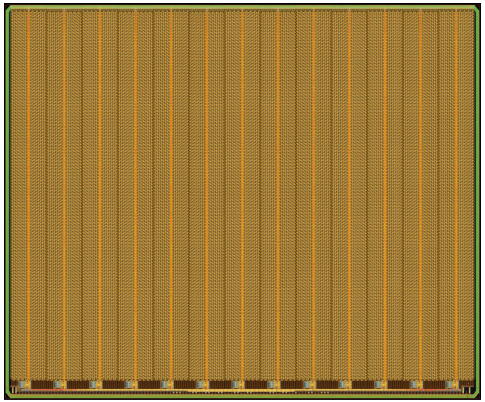


The pedestal is time dependent and it disappears at low temperature, suggesting the presence of a current leakage.

Production ASIC : Solved

Problems Solved

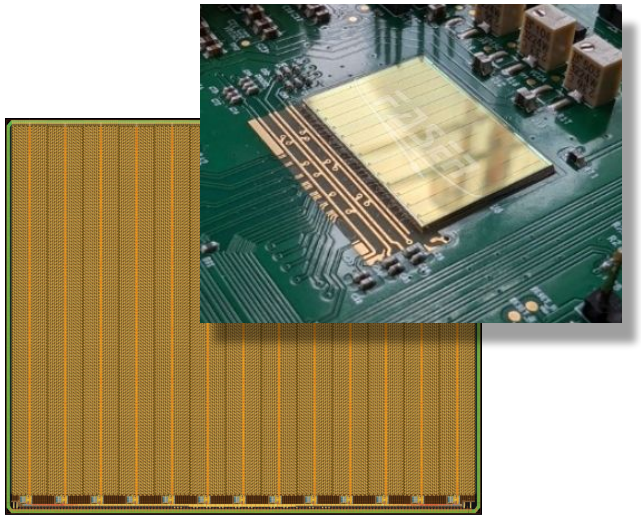
- No memory drift
- Synch digital blocks
- Able to operate at 200 MHz
- Fast calibration methods



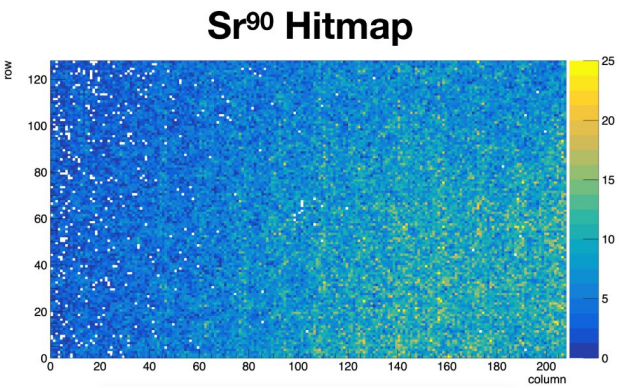
Production ASIC : Solved

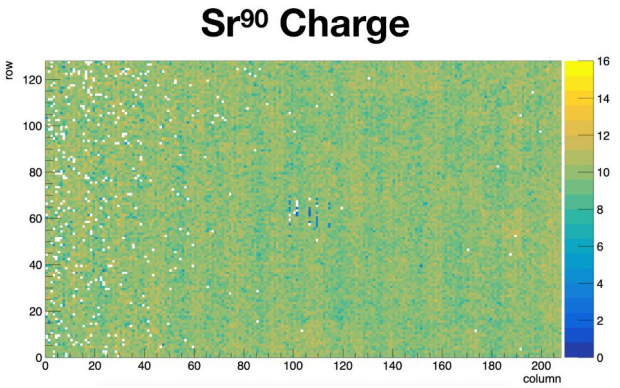
Problems Solved

- No memory drift
- Synch digital blocks
- Able to operate at 200 MHz
- Fast calibration methods



Laboratory Measurement



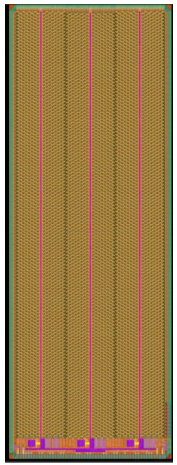


Source characterization for the final ASIC

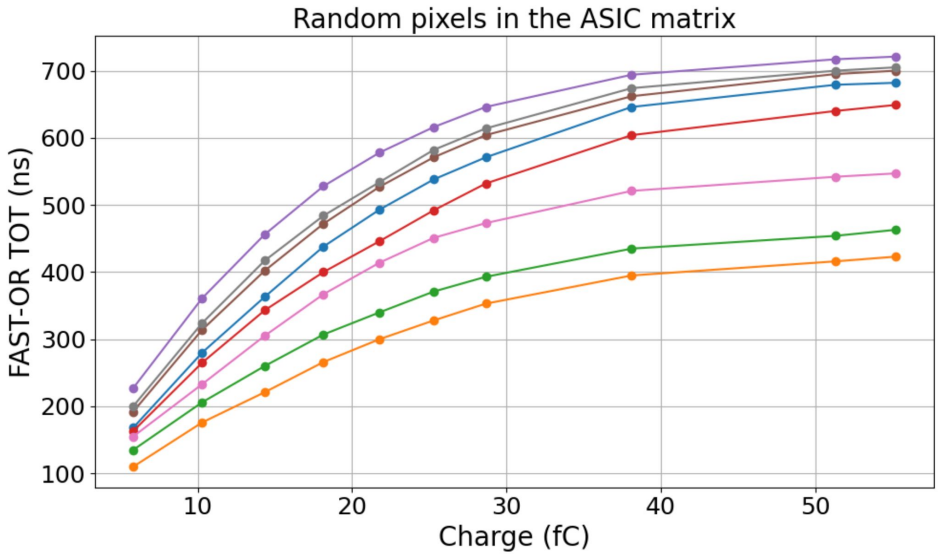
Pre-production ASIC: Mismatch

Problems Detected

- Memory drift: **SOLVED**
- Synch digital blocks: **SOLVED**
- Unable to operate at 200 MHz: **SOLVED**
- Long calibration methods: **SOLVED**
- Mismatch



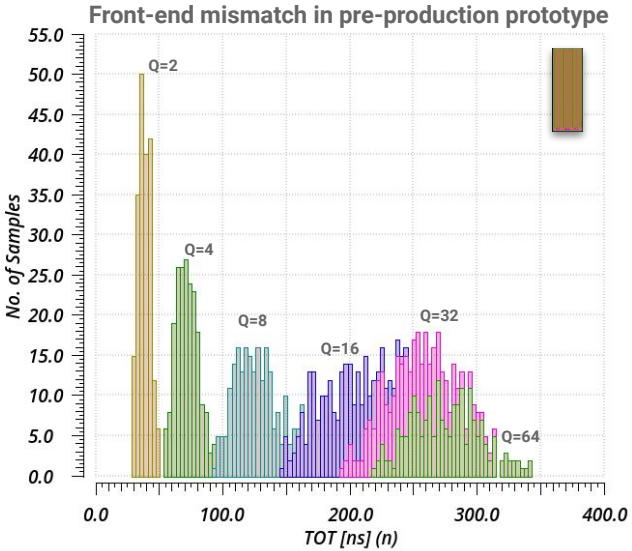
Laboratory Measurement

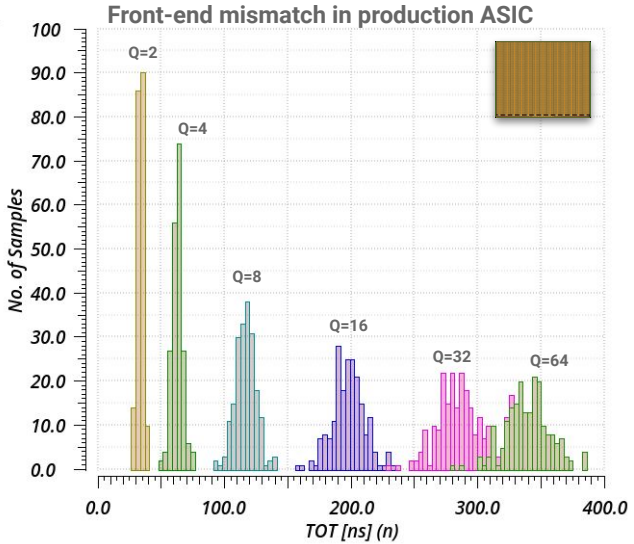


Big variation of TOT in the same injected charge value

Simulation: TOT mismatch

Cadence Spectre Simulation





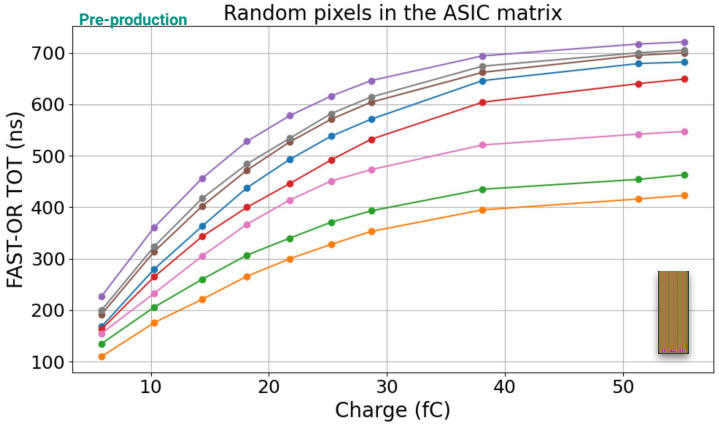
Some mismatch observed from amplifier response: increase the size of preamplifier transistors

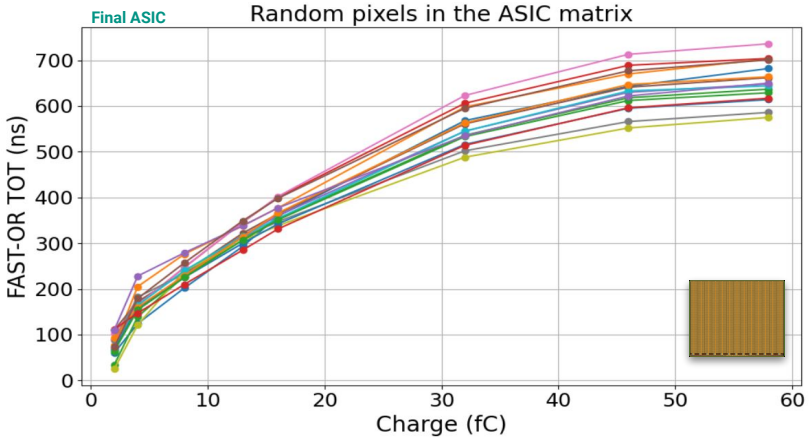
Production ASIC-Mismatch: Solved

Problems Solved

- No memory drift
- Synch digital blocks
- Able to operate at 200 MHz
- Fast calibration methods
- More uniform pixel to pixel response

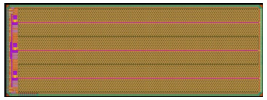
Laboratory Measurement





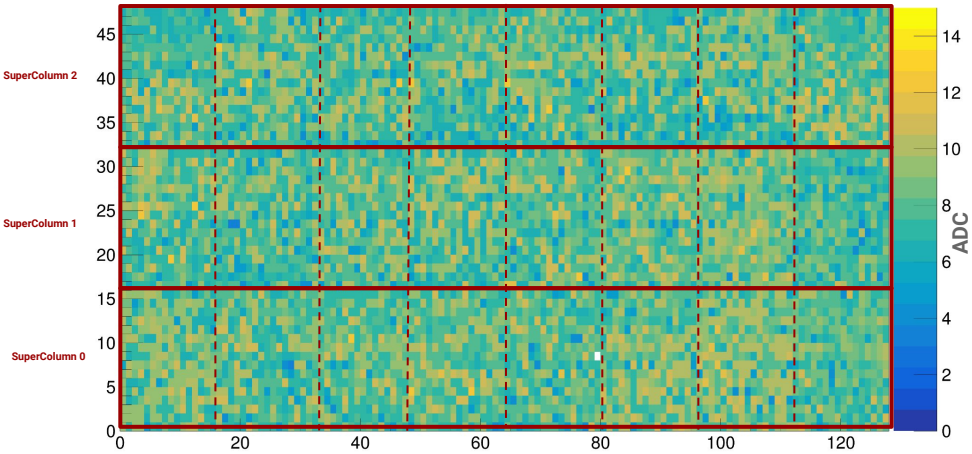
Much smaller variation on the TOT values for the final ASIC

Charge calibration

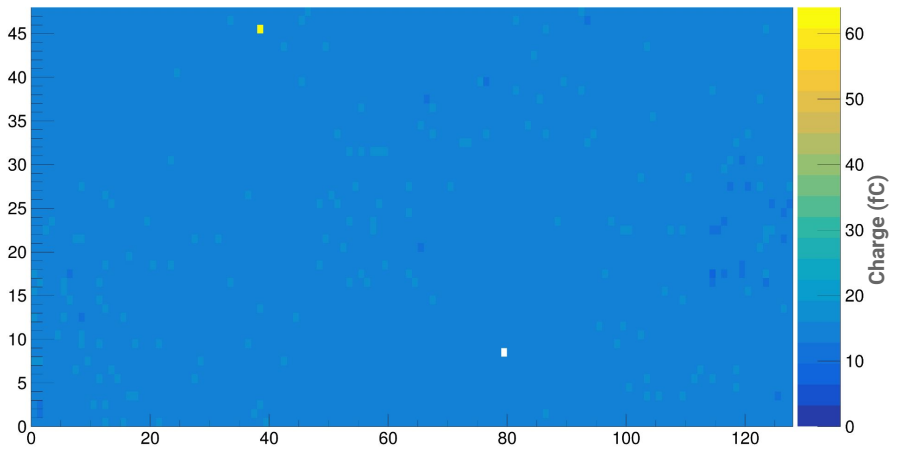


Laboratory Measurement

Before Calibration



After Calibration



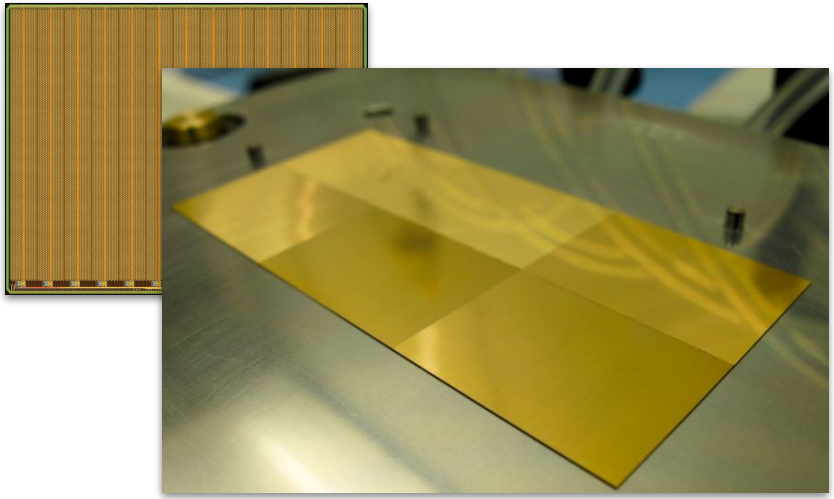
Injection of 14 fC, in the whole ASIC matrix

Conclusions

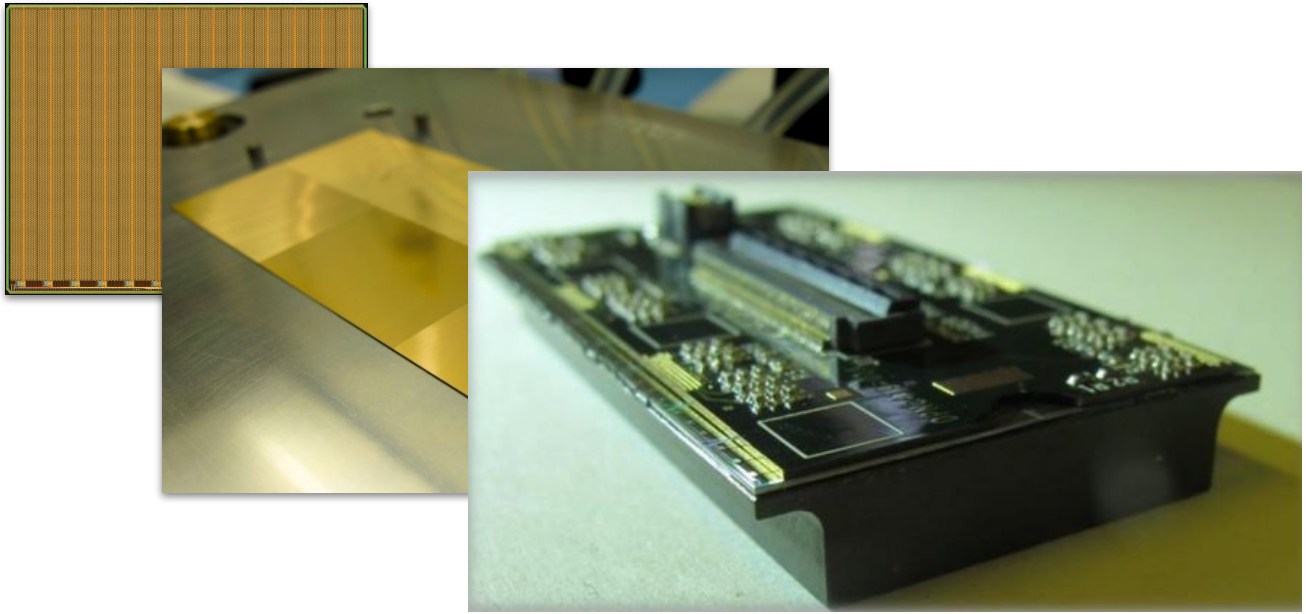
Conclusions

- A **new preshower detector** is being developed for the **FASER experiment** at the LHC
  - Enabling discrimination of ultra-collimated multi-TeV diphoton events from LLP decays
  - Chosen technology: 130nm SiGe BiCMOS MAPS designed and developed at UniGe
  - Installation in 2024, data taking during LHC Run 3 and High-Luminosity LHC
- **Preproduction chips delivered in June 2022**
  - Everything is working fine with lab characterization
  - Minor bugs have been identified and they are corrected
  - First assembled modules currently ongoing
- **Final chip just delivered & meets the expectations!**
  - More ongoing tests

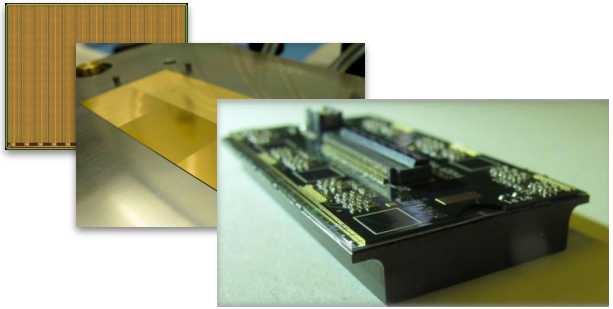
Next steps

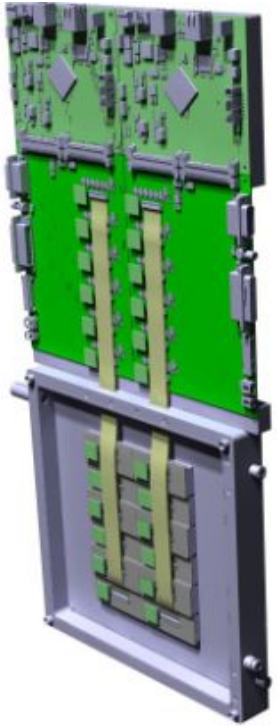


Next steps

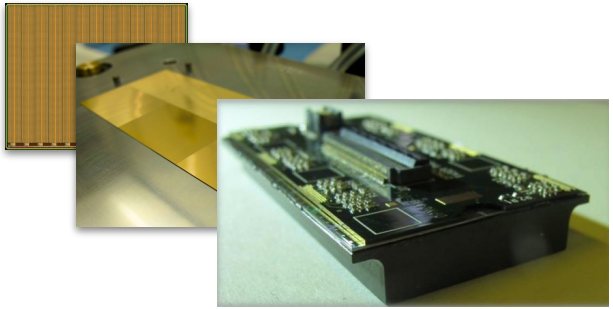


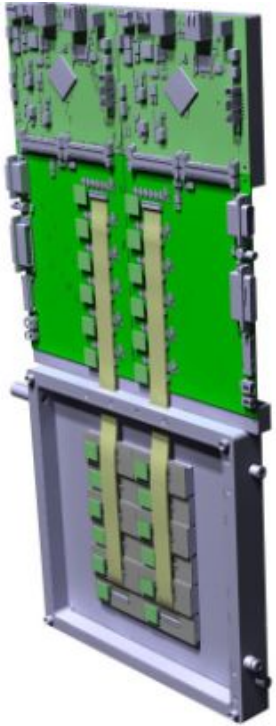
Next steps

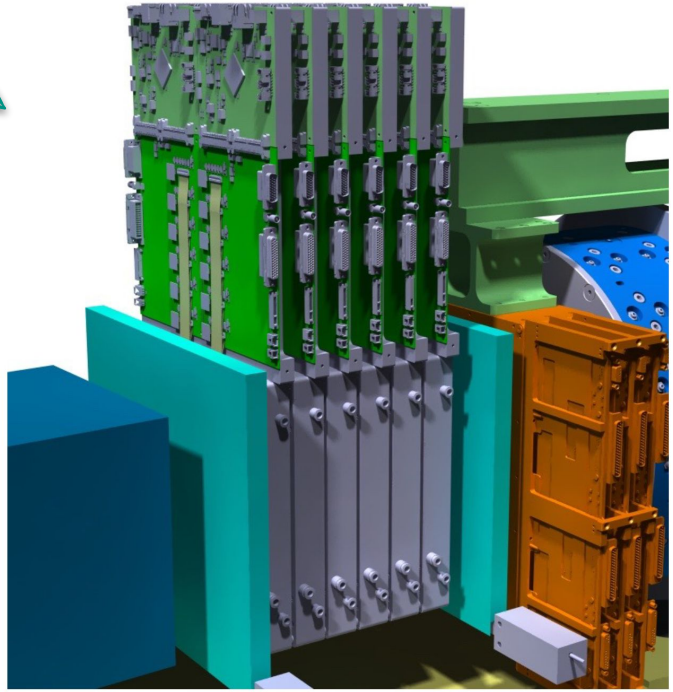




Next steps







The people…

FASER COLLABORATION

99 collaborators, 27 institutions, 11 countries

FASER Collaboration Members

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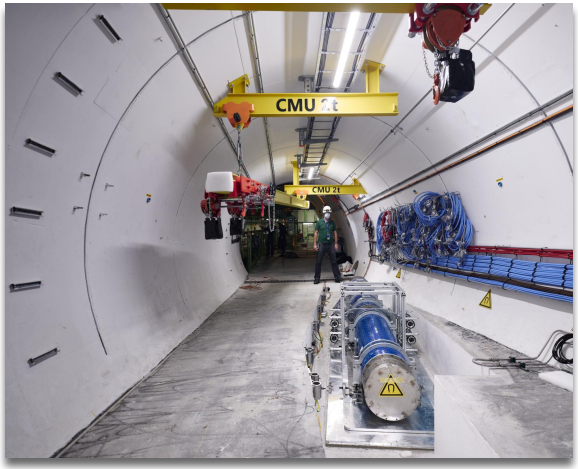
99 members from 27 institutions and 11 countries

The development and construction of the W-Si pre-shower of the FASER experiment was funded by the **Swiss National Science Foundation (SNSF)** under the **FLARE grant 20FL21-201474** at the University of Geneva. Additional financial contributions from **KEK**, **Kyushu University**, **Mainz University**, **Tsinghua University** and the **Heising-Simons Foundation** are also acknowledged.

Thank you for your attention…!

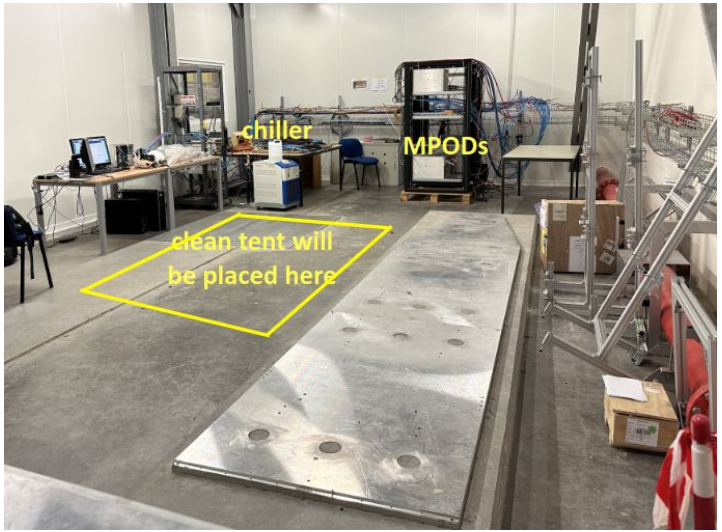


FASER installation in TI12 tunnel

Backup Slides

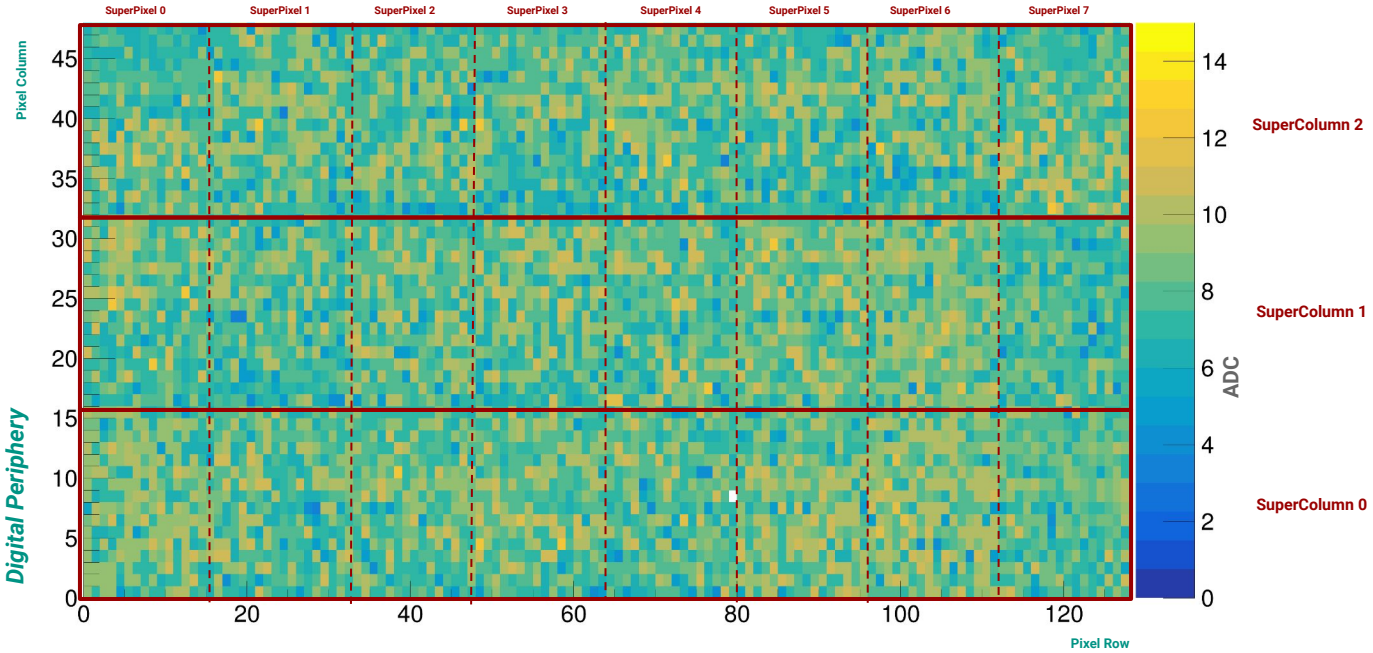
Preparations ongoing for detector commissioning and installation

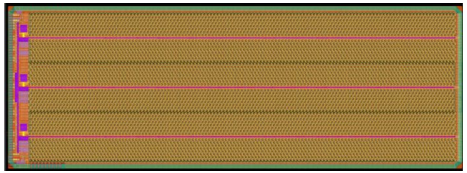
- Test planes one by one as they are brought to EHN1, and then assembled prewhower
- Tests with realistic services, DCS, TDAQ software; preparations in EHN1 have started



Pre-production ASIC, injection of 14.3 fC

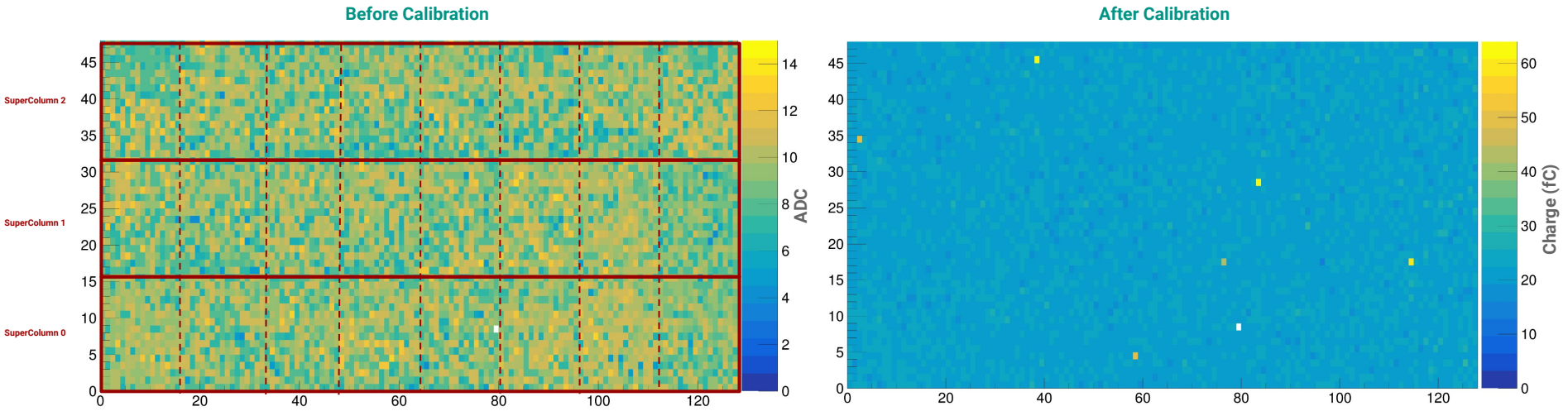
Laboratory Measurement





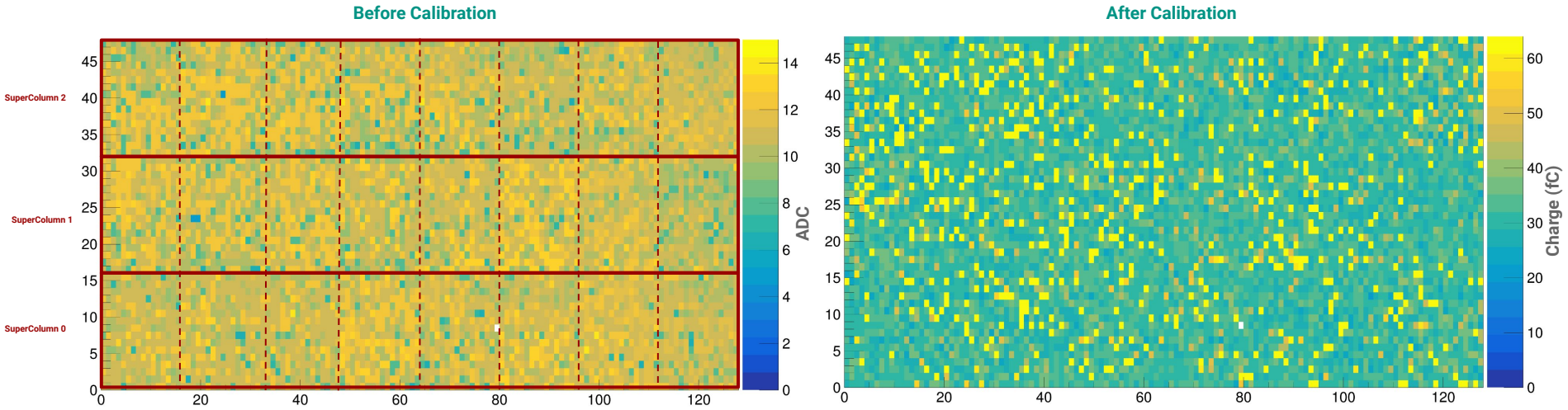
Injection of 21.78 fC, in the whole ASIC matrix

Laboratory Measurement



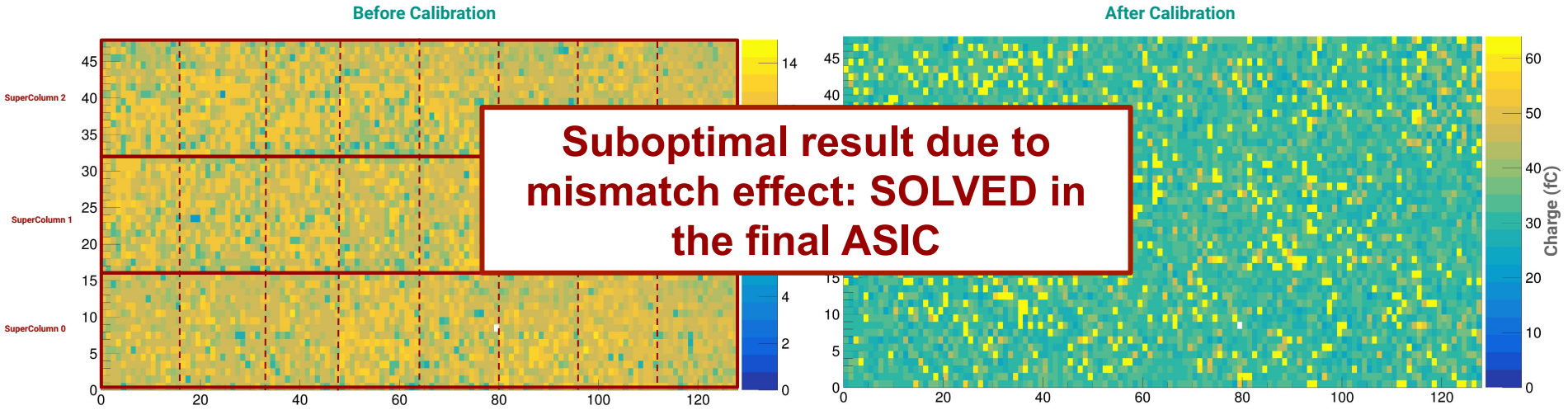
Injection of 31.95 fC, in the whole ASIC matrix

Laboratory Measurement



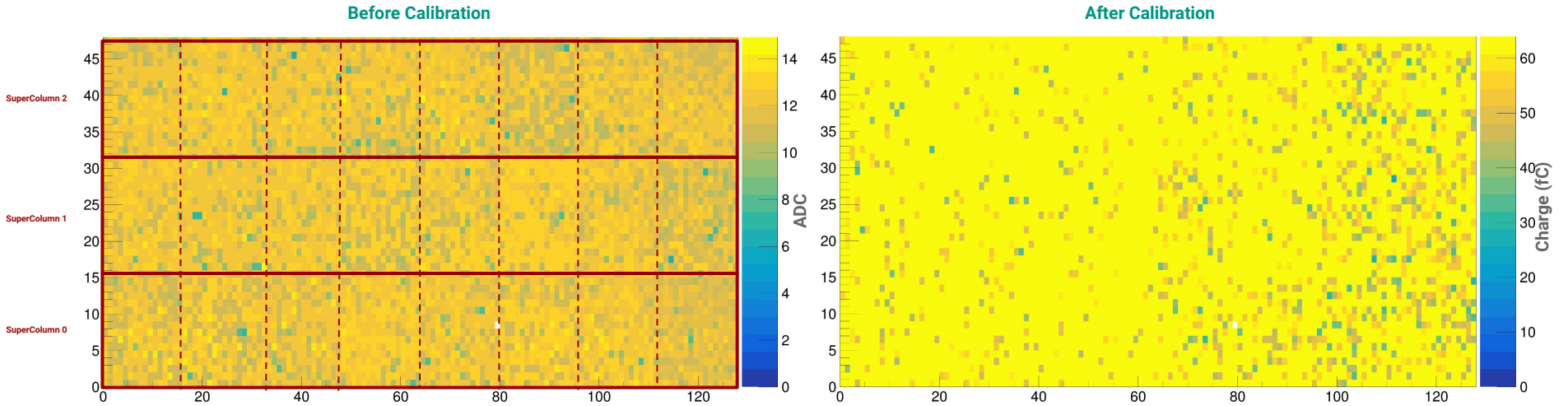
Injection of 31.95 fC, in the whole ASIC matrix

Laboratory Measurement



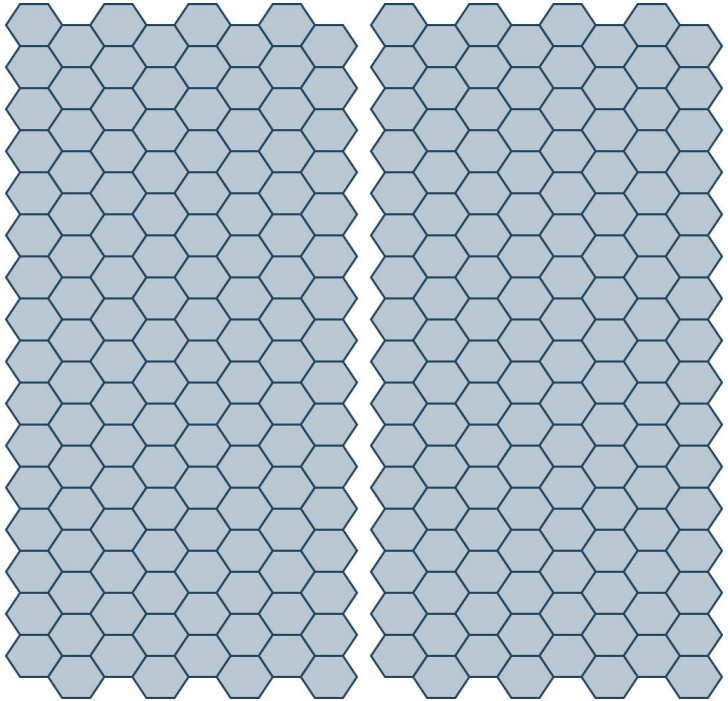
Injection of 54.25 fC, in the whole ASIC matrix

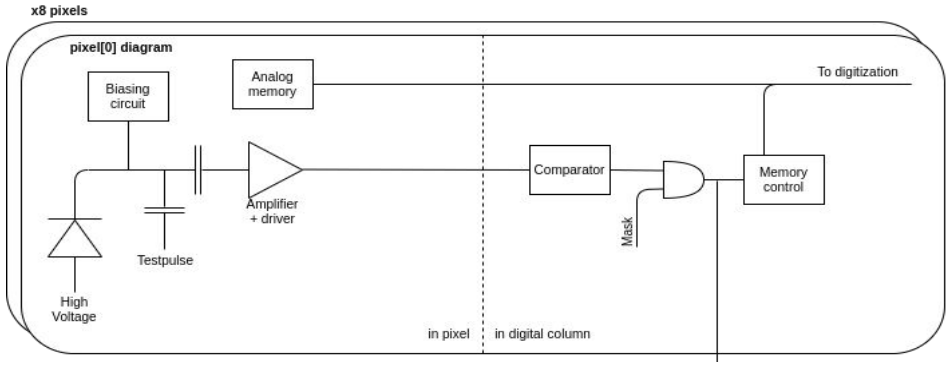
Laboratory Measurement



General Charge Calibration Method

Part of the pixel matrix





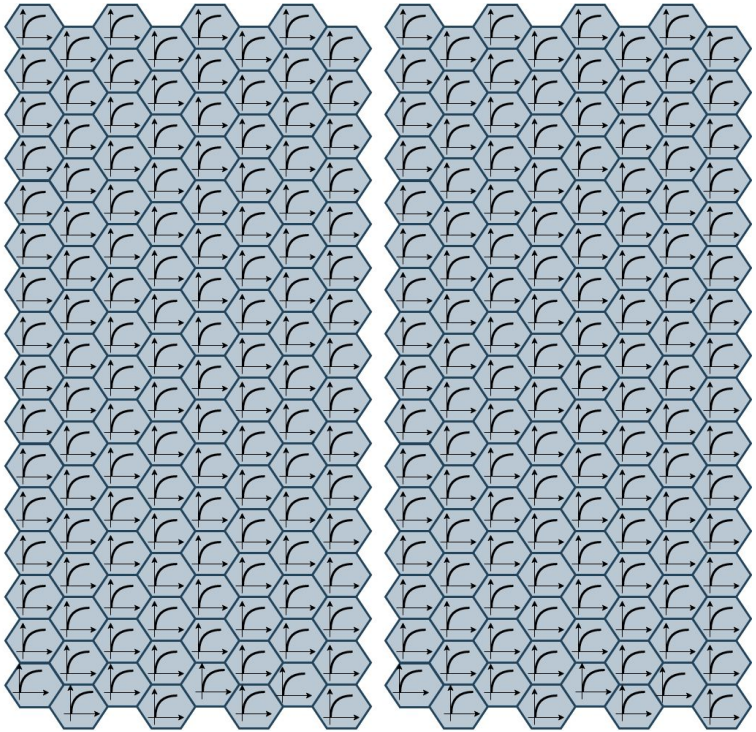
Analog signal ⇒ We receive digitized data from the chip

Goal of the charge calibration:

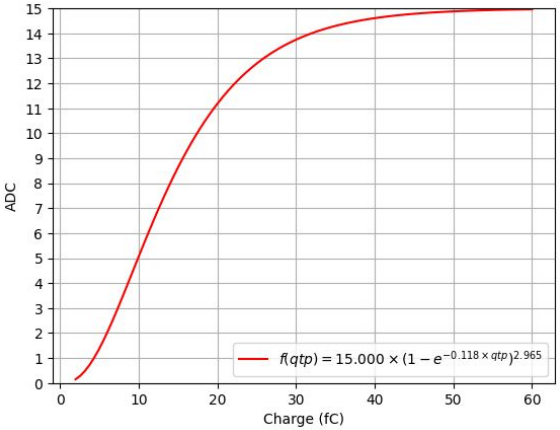
From the digitized data information, reconstruct the real fC charge information that the particle deposited in each pixel

General Charge Calibration Method

Part of the pixel matrix in a perfect world



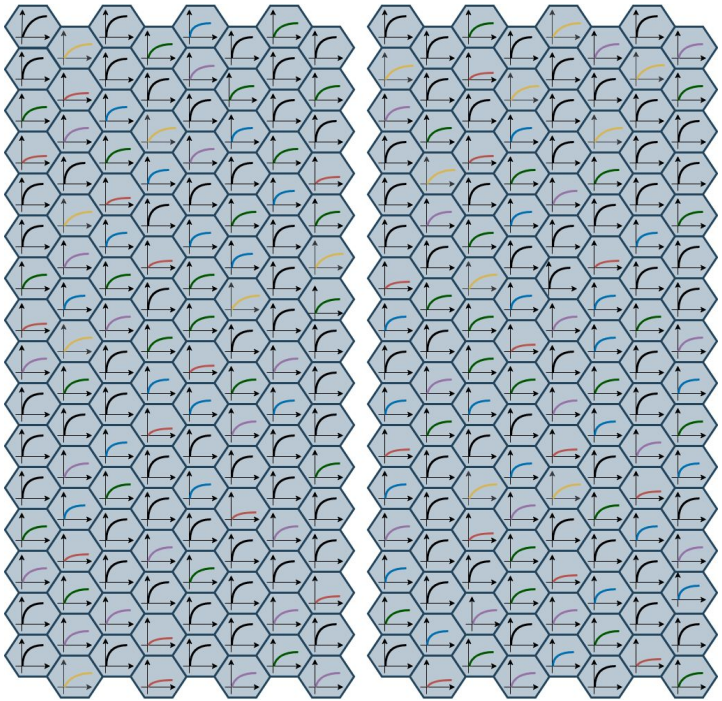
Example plot of our logarithmic response



- Each pixel has the same response and the same saturation point, taking the advantage of all the ADC bin range.

General Charge Calibration Method

Part of the pixel matrix in the real world now

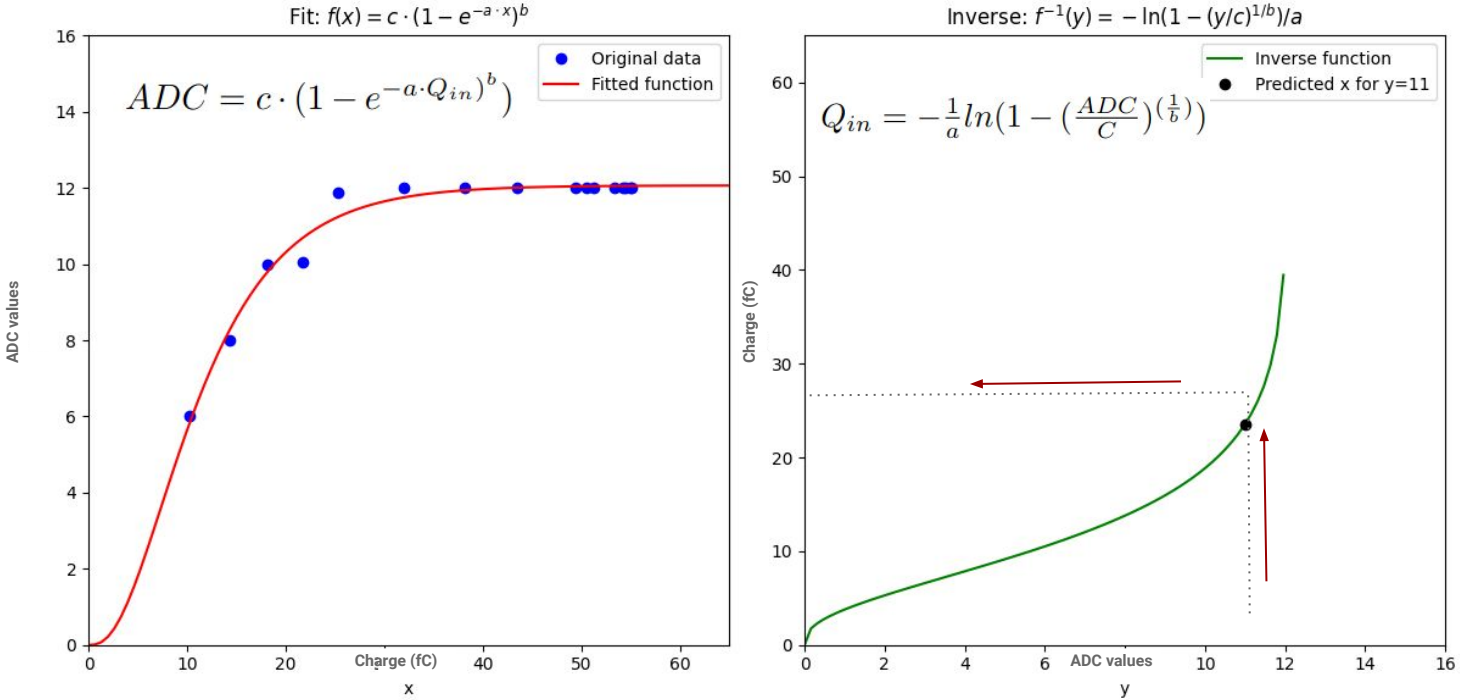


- This means:
  - Saturation too early
  - Different saturation point
  - Each pixel saturates in different bin
  - Different size of the bins
- Big error in high charges

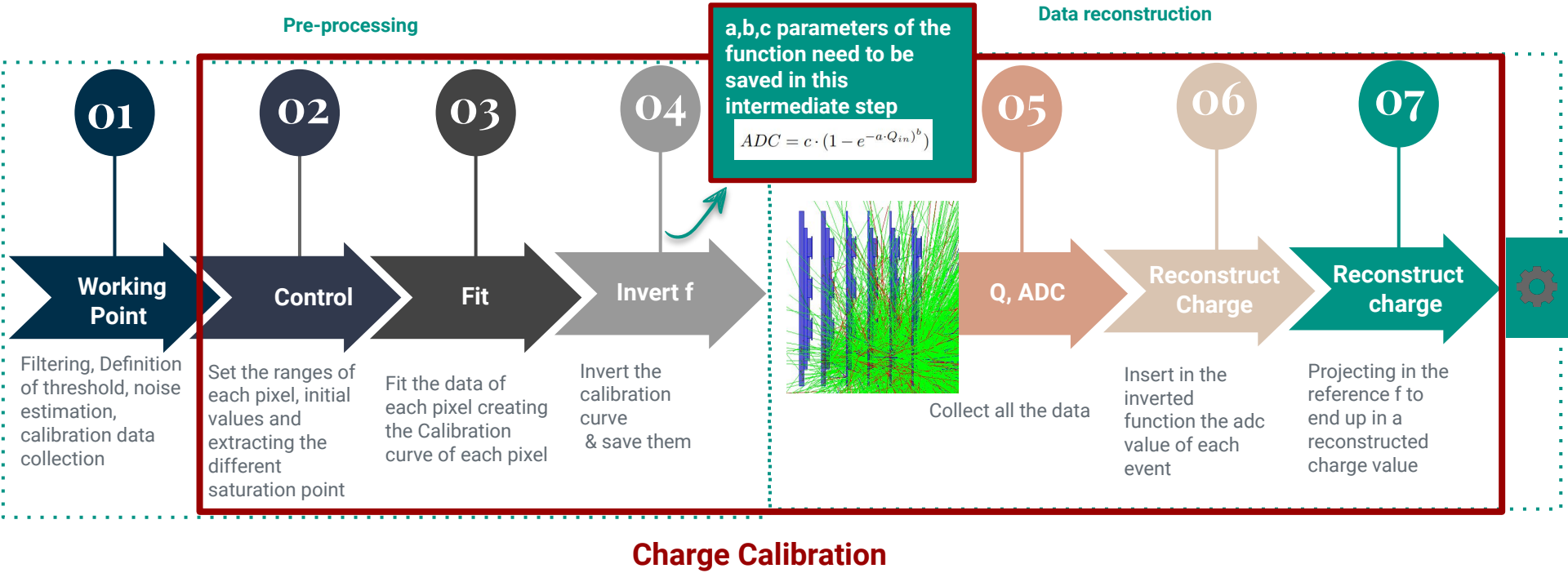
Goal of the charge calibration:

From the digitized data information, reconstruct the real fC charge information that the particle deposited in each pixel, considering the response of each pixel

One pixel's calibration curve



General Calibration Method



Charge Calibration

The Detector Effects Code

Link to the modules: https://gitlab.cern.ch/rkotitsa/allpix-squared/-/tree/calibration_genie_updated?ref_type=heads

01 Q,V

Import and fit real data from chip measurements!

⇩

Sets of (Q,V) pairs

$$y = a + b(1 - e^{c(x-d)})$$

⇩

f_i

02 "PixelCharge"

PixelCharge

⇩

Q_s, (x, y)

03 Conversion

Apply random f_i to Q_s.

$f_i(Q_s) = V_s$

04 Add Noise

Add gaussian noise

$V_s \Rightarrow V_{sn}$

05 Discretization

16 equal bins in the range of V

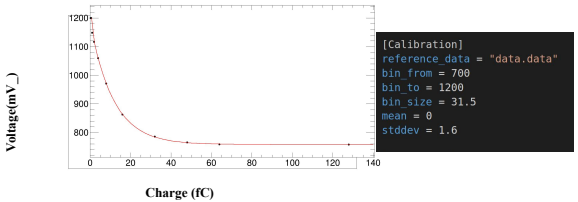
$V_{sn} \Rightarrow V_f$

06 Inversion

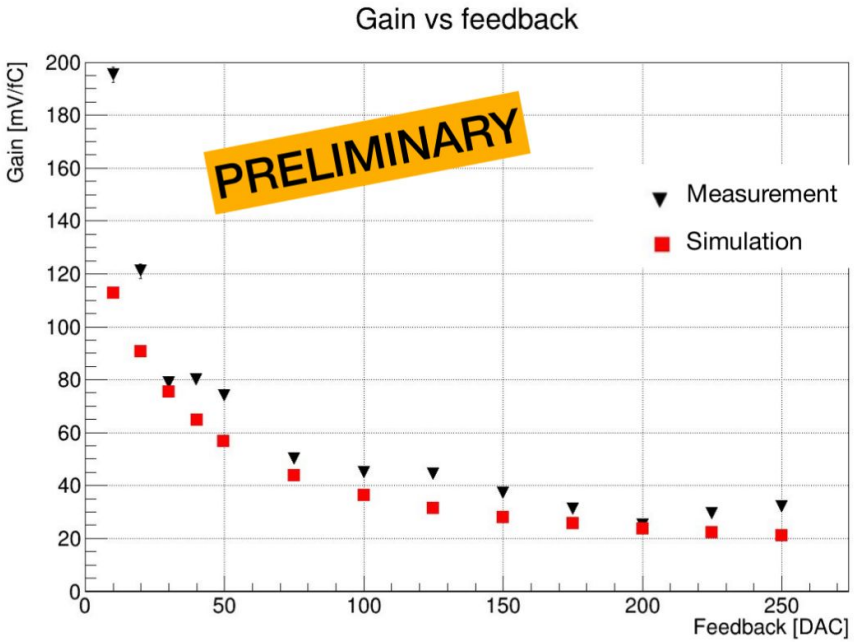
$f^{-1}{}_1(V_f) = Q_{meas}$

07 Qmeas

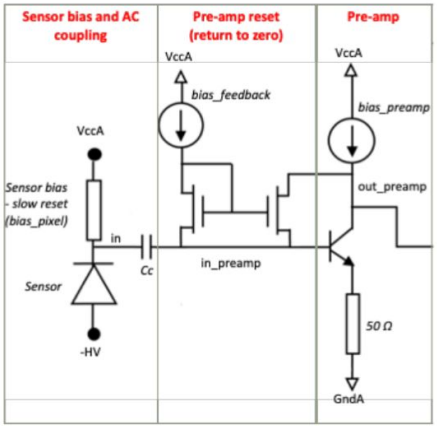
Q_{means_s}, (x, y)



Gain Vs Feedback



Test pulse with fixed charge

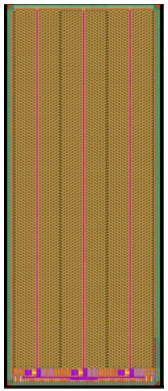


Feedback changes baseline and gain

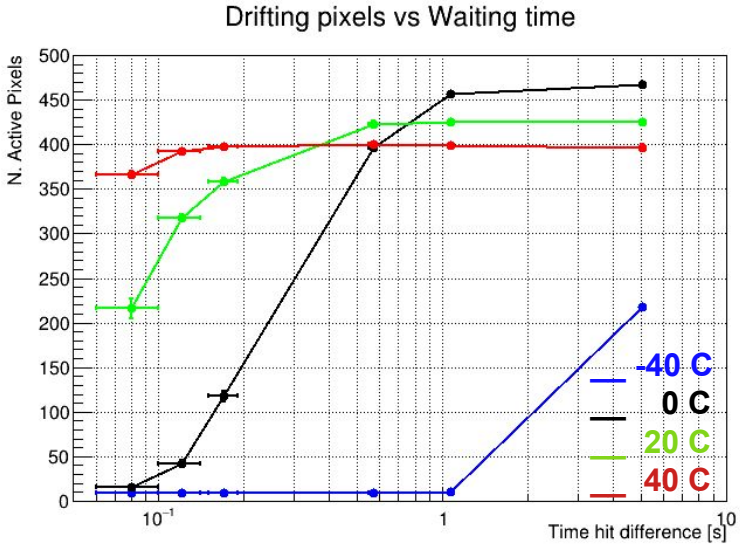
Pre-production ASIC: Memory Drift

Problems Detected

- Memory drift
- Synch digital blocks
- Unable to operate at 200 MHz
- Long calibration methods

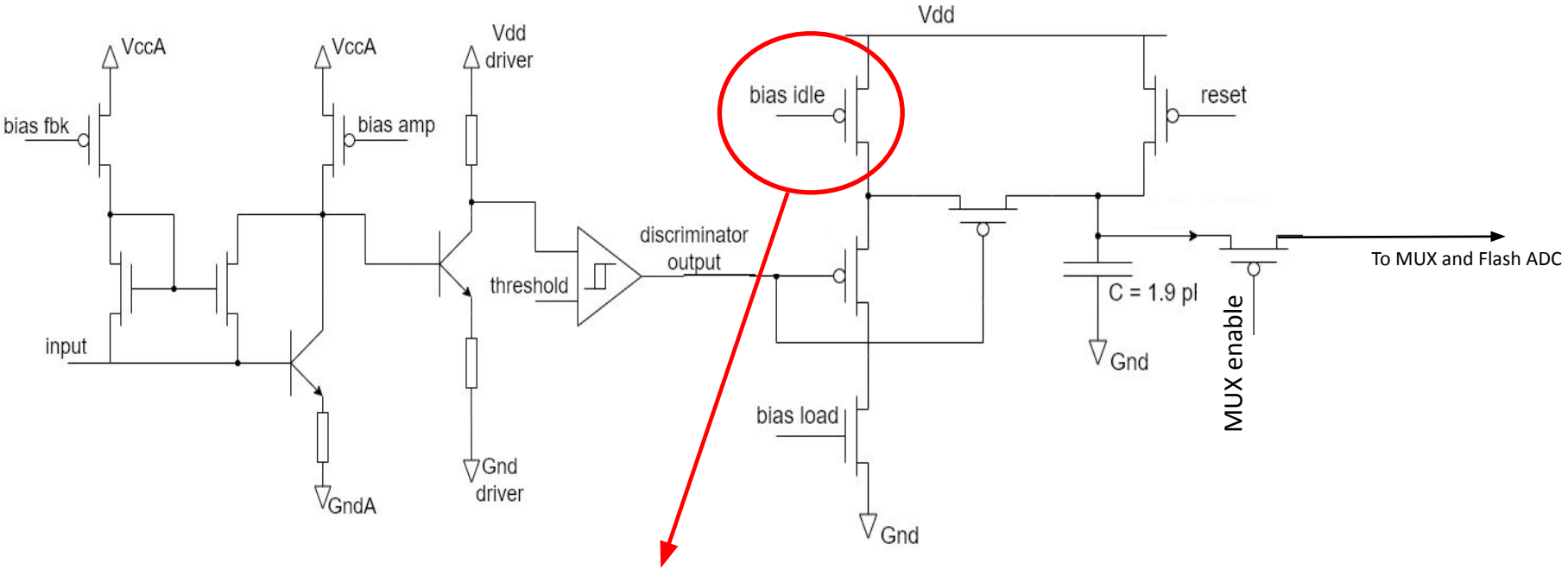


Laboratory Measurement

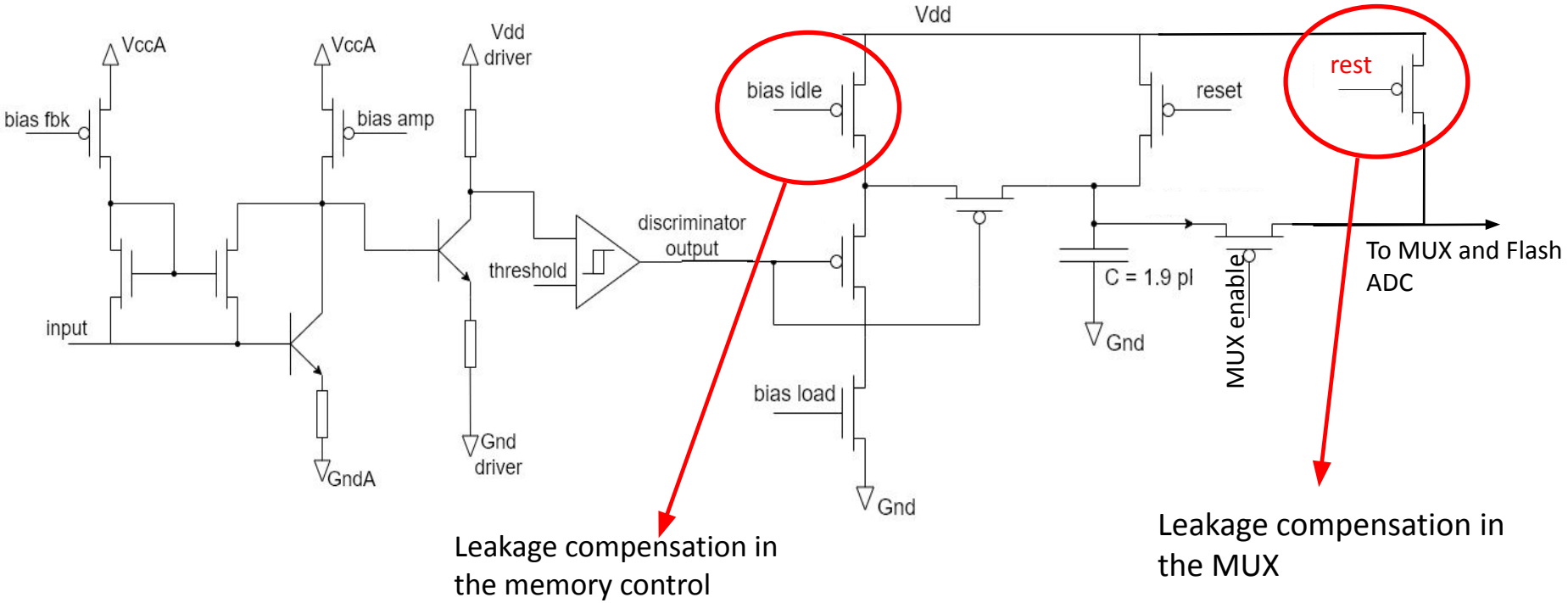


The pedestal is time dependent and it disappears at low temperature, suggesting the presence of a current leakage.

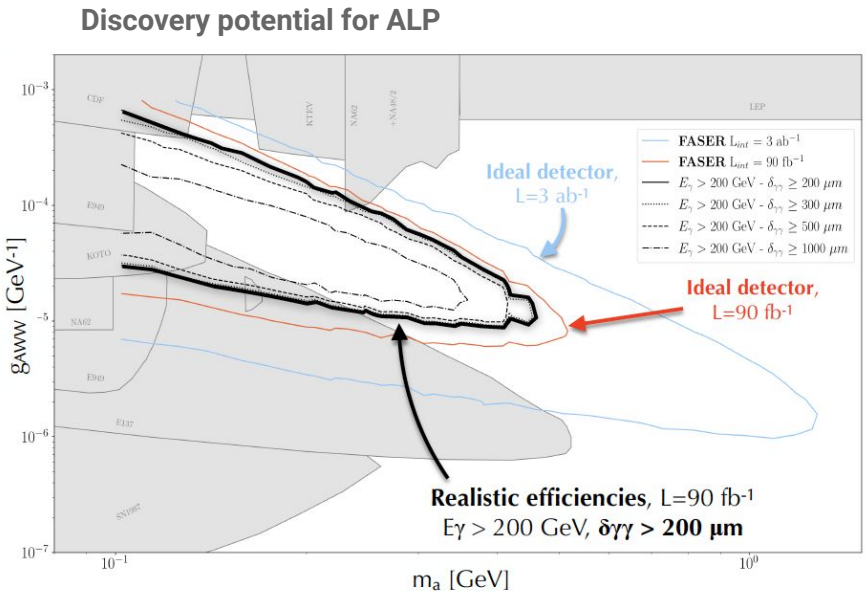
Memory leakage – test from pre-production ASIC



Memory leakage – test from pre-production ASIC

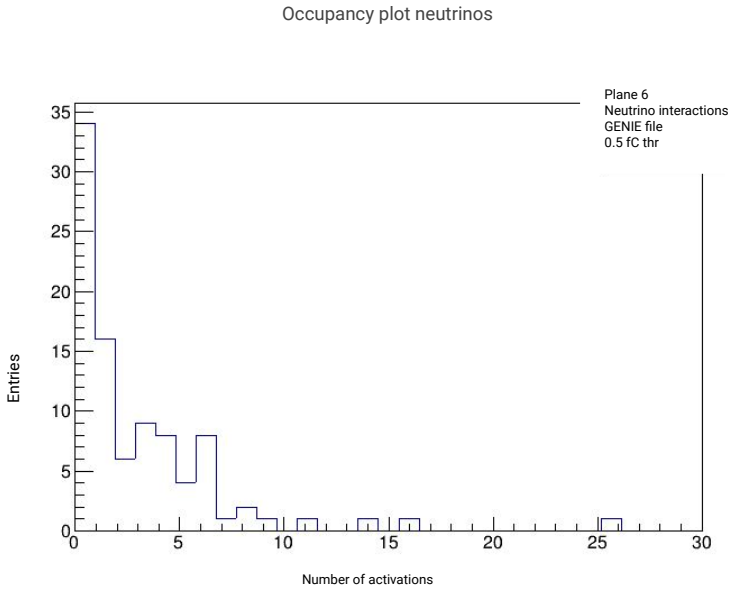


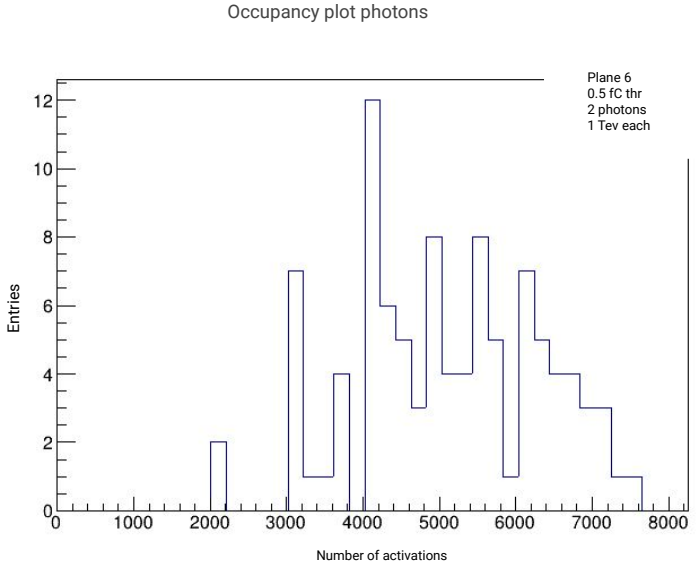
Motivations for the new preshower detector



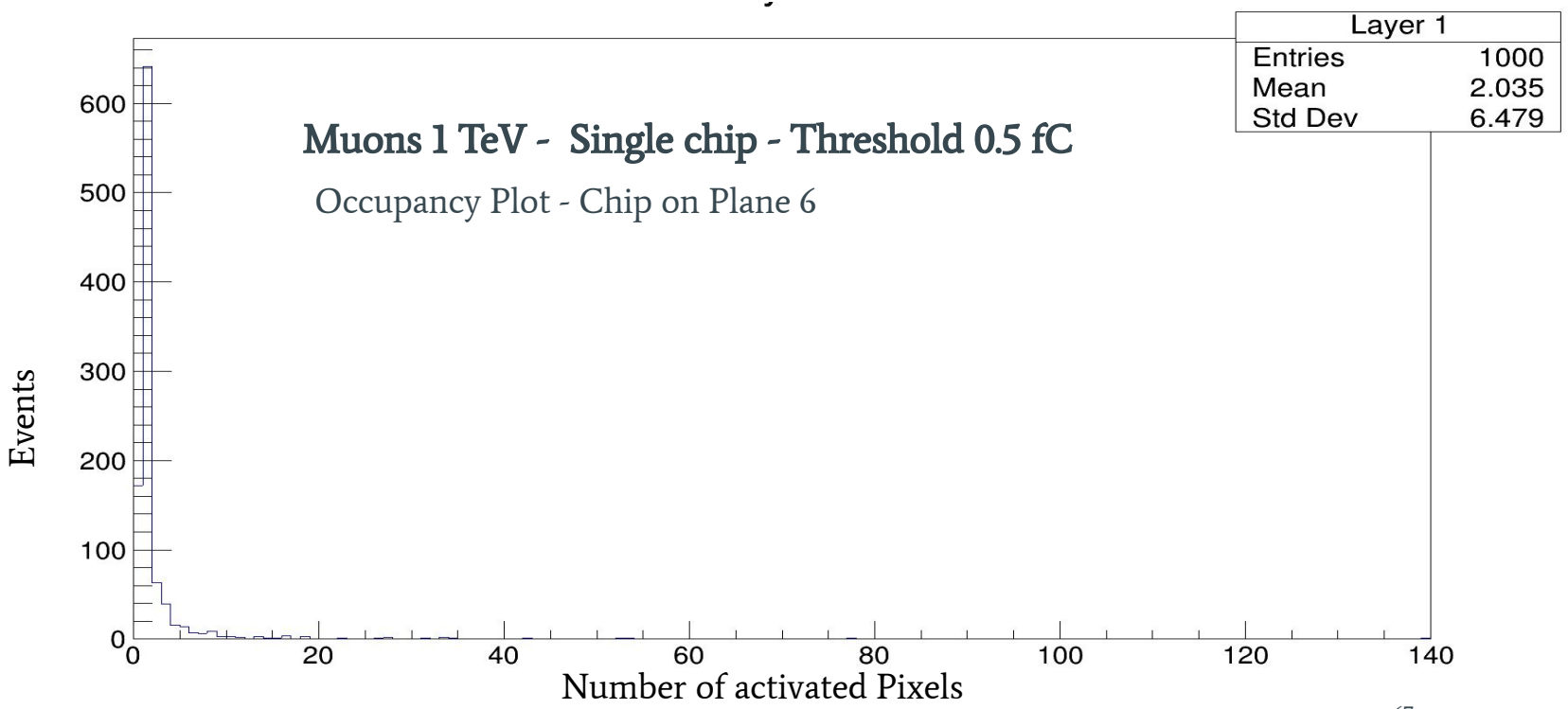
Detector requirement: Discriminate photons with 200 μm separation to exploit the full potential of the experiment.

Simulation results





Simulation results



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