

Development of a common pixel readout electronics for pixel detector

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Abstract: Pixel detector is one of the most advanced radiation detectors. Due to its advantages, pixel detectors have been applied in multiple international physics experiment equipment and have shown excellent performance. This paper presents the Common Pixel Readout electronics (CPR) for pixel detectors. CPR is based on Xilinx Kintex 7 series FPGA. It has four optical fiber interfaces with a total bandwidth of 50 Gbps, 2 GB DDR3 and Universal Serial Bus Gen 3.0 (USB3.0). Using optical to electrical converter module, it can support up to 10 Gigabit Ethernet, which means it can effectively store short-term test data and transmit data to the upper computer. In pixel detector testing, CPR has a 16-channel 14-bit, 65 MSPS ADC, two 8-channel 16-bit DACs and 44 GPIOs for chip control. In laboratory tests, the error rate of the optical fiber is as low as $1.7E-15$, and the R-Square values of DAC voltage output and ADC acquisition data are both greater than 0.9999. This paper will discuss the design and performance of CPR.

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