TCAD Simulation of Stitching for Passive CMOS Strip Detectors

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Most of the tracking detectors for high energy particle experiments are covered by silicon detectors since they are radiation hard, they can give very small spatial resolution and they can take advantage of the silicon electronics foundries' developments and production lines.

Big area strip detectors are very useful to cover large areas for tracking purposes. The majority of particle physics experiments use conventional silicon strip detectors fabricated in foundries that do not use stitching, relying on a very small number of foundries worldwide that can provide large area detectors. For this production we fabricated strip detectors in a CMOS foundry, based on CMOS imaging technology, using two $1\,\mathrm{cm}^2$ reticles stitched three and five times. The passive CMOS strip detectors were produced by LFoundry with 150 nm technology, 150 µm thick 3-5 $\mathrm{k}\Omega\,\mathrm{cm}$ wafer and back-metalized at IZM Berlin. With this project we want to investigate if the stitching of two reticles impacts the performance of the passive strips, since the strip implant might be separated or in a slightly different configuration that could increase the electric field. Figure 1 shows an image of a passive CMOS strip detector with a stitching line next to the pads.

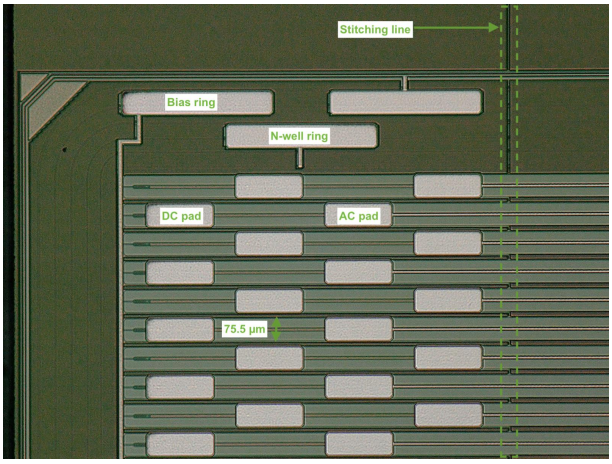

Figure 1: Image of the passive CMOS strip pad with the stitching line.

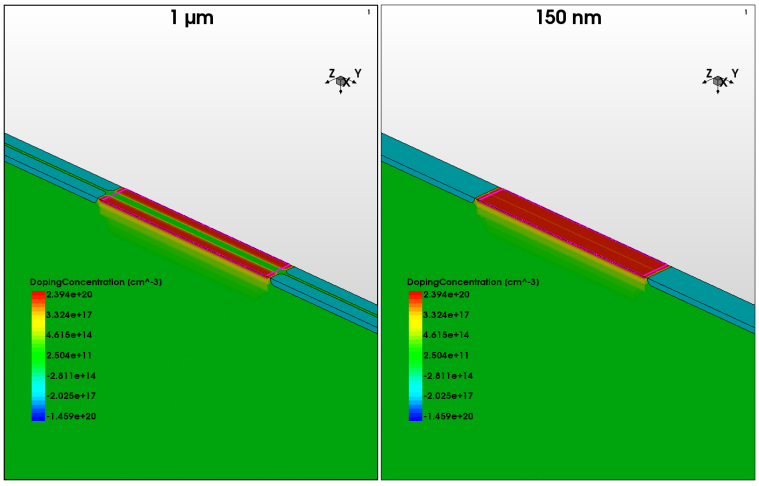

Figure 2: Doping profile simulation of the two stitching distances, left 1 µm and right 150 µm.

To know the precise impact of stitching we used the Synopsys Sentaurus Technology Computer-Aided Design (TCAD) software for simulating how stitching might affect the performance of the strip detector. Different stitching effects can be taken into account since we do not know the exact alignment of the two consecutive reticles for stitching, but for this simulation we considered the implant being separated between the two reticles. We simulated a non realistic 1 µm stitching distance and 150 nm that corresponds to the foundry technology resolution. For doing that, we simulated a single 3D strip segment with a 2 µm long structure to take into account the stitching distances as shown in Figure 2. The full strip simulation is not considered for computational constrains. Figure 3 shows the simulation of the electric field at 100 V (when the detector is fully depleted) for the two stitching distances. The simulation shows that the electric field for 1 µm stitching distance has a non depleted region on the surface in the inter-stitching region, therefore the strip loose efficiency along the 1 µm stitching distance. This distance is not appreciated for 150 nm stitching, having negligible impact on the performance of the strip.

For this presentation we will show an overview of the excellent results of passive CMOS strip detectors in testbeams and lab setups, measurements of the sensors unirradiated and irradiated as well as an in-depth TCAD simulation of the stitching impact, and future plans for the next CMOS submission for this project.

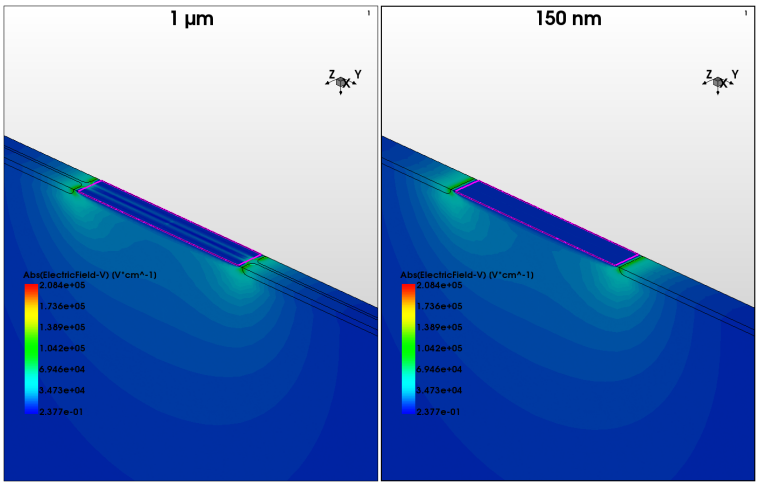

Figure 3: Electric field simulation at 100 V of the two stitching distances, left 1 µm and right 150 µm.