A High Accuracy CMOS Peak Detection and Holder ASIC for Neutron Detectors

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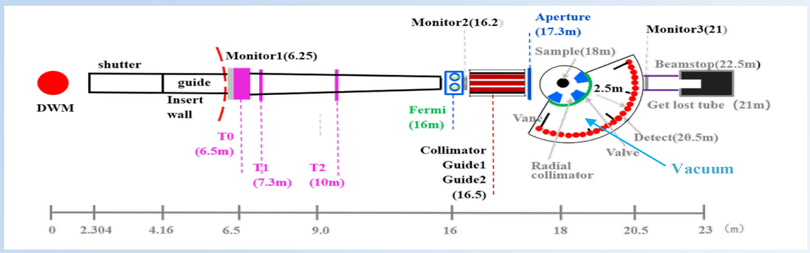
INTRODUCTION

China Spallation Neutron Source is the first spallation neutron source in China. The first phase of the project has been completed and three instruments are open to users. During the cooperative instrument phase, eight instruments were jointly constructed with other research institutions. The second phase of the project will officially start in 2024, and will involve the construction of seven new neutron instruments and multiple test beamlines. At the same time, the target power will be increased from 160 kW to 500 kW.

Neutrons are ideal probe for exploring material dynamics, with neutron scattering pivotal in defense, industry, and research. High-performance neutron sources like CSNS drive demand for improved spectrometers, necessitating a vacuum to reduce neutron-air collisions for precise measurements. The traditional readout electronics, reliant on discrete components and commercial chips, fall short due to high power usage, large size, and limited event rates. These drawbacks impede next-gen neutron spectrometers' demands for performance and operational conditions.

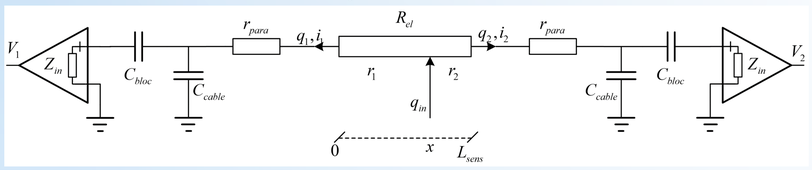
Building upon the HEROC chip (a readout chip developed by the Institute of High Energy Physics, Chinese Academy of Sciences for Helium-3 tube neutron detectors), this chip optimizes front-end circuit parameters and achieves peak detection and hold functions. The ASIC further reduces the power consumption of the entire electronics system, introducing a fundamental research direction for electronics designed for vacuum-operated 3He neutron detectors.



the Illustration of Inelastic Scattering Spectrometer in CSNS

MODELING OF ^{3}He PSD

Position-sensitive ^{3}He detector utilize charge division methods to calculate the incident neutron position, making the precision of charge measurement directly impact the detector system's position resolution. Simultaneously, the charge equilibrium effect within the ^{3}He detector causes unequal charges at both ends to migrate towards the anode wire, equalizing the charge distribution and thus affecting the accuracy of charge measurement. Through software modeling of the ^{3}He detector's intrinsic characteristics and theoretical analysis of front-end circuit parameters, a circuit-level solution for the aforementioned issues is presented. This solution involves considering factors such as the input impedance and open-loop gain of core operational amplifiers, as well as shaping circuit-level aspects like signal width and structure during the design phase. By doing so, the overall position resolution of the entire system can be enhanced.



the Equivalent Circuit Model for ^{3}He Tube Detector with Second-Order Effects

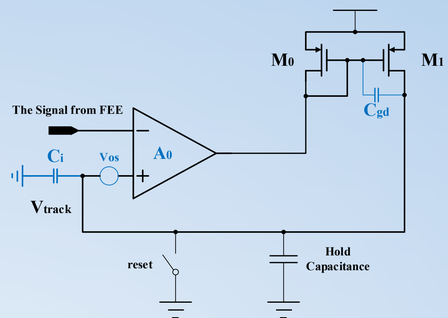
PDHASIC

The HEROC chip accomplishes the conversion and amplification of readout signals from 3He tube neutron detectors. Building upon this, the ASIC implements peak detection and hold function. The 8-channel ASIC is designed using the Global Foundry 0.18 μm IC process， has a 40fC to 1pC input signal range. The chip area is 2368 μm * 2413 μm and includes front-end circuits, peak hold modules, trigger circuits and DAC modules.

the Schematic of One Channel of PDHASIC

The PDH module is supplied with a single voltage of 1.8V with a total power consumption of 350 μW with a layout area of 361 μm $\times$ 68 μm. The peak hold module adopts the structure as shown in the figure below, and utilizes the classic circuit structure mentioned in the literature by Gianluigi De Geronimo. The voltage to be held is converted to current through a current mirror, and an on-chip 7 pF capacitor is used as the hold capacitor to achieve peak hold function. Additionally, a switch controlled by a discriminator module is added to the loop for voltage discharge function. The holding time of the peak hold module can be controlled by the discrimination signal generated by the discriminator.

PDHASIC & SIM. RESULTS



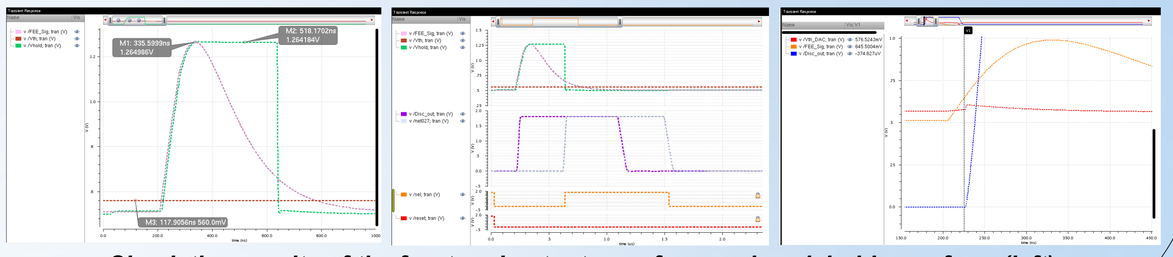
the Schematic and the Parasitic Parameters of the PDH Module

Parameters Table for the PDH Module

Specification	Simulation Results
Power dissipation of the module	350 μW
Pulse amplitude range	tens mV to 1V
Relative error peaking time = 200ns	40mV to 90mV < 1% 90mV to 800mV ≤ 0.22% 800mV to 1V < 0.62%

In order to achieve a better accuracy, the following aspects were considered in the design: 1. the size of the current mirror and the selection of the hold capacitor value; 2. the design value of the open-loop gain of the core amplifier; 3. the input tube size of the core op-amp; 4. additional errors brought by the external buffer in the feedback loop. In this version, a more complex multi-phase read/write control circuit structure was not used. This can be considered in future revisions to further improve the accuracy of peak hold.

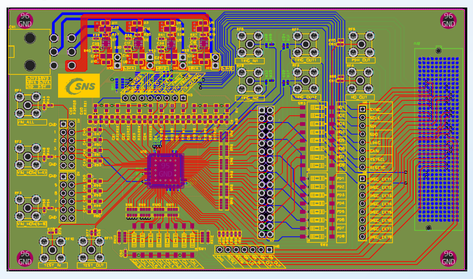
In the DAC design, attention was focused on the impact of kickback noise on threshold comparison. In the simulation results, it was observed that the threshold generated by the DAC would undergo a certain change when the discriminator output begins to flip. However, this change occurs after the discriminator has started to flip, so it is considered that the impact on the discriminator output can be ignored.



Simulation results of the front-end output waveform and peak hold waveform (left); discriminator output signal and its delayed signal, with the hold capacitor reset controlled by the sel signal (middle); simulation results of DAC kickback noise (right)

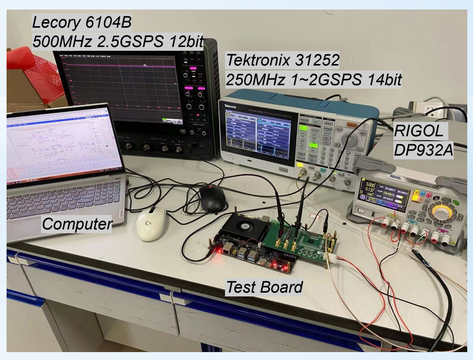
MEASUREMENT SETUP

The chip has successfully completed tape-out, and the die has been diced. The chip is wire-bonded to the front-end circuit board, which supplies power, injects calibration signals, and connects to the FPGA development board via an FMC connector. The FPGA, which is an XCZU9EG-2FFVB1156E MPSoC, is used to control the ASIC. The test setup has been fully set up, and we have completed preliminary power-on and basic tests. The chip's power consumption and DC bias are consistent with the design simulation results. Detailed testing will proceed step by step, and we expect to publish the related test results in the conference proceedings.

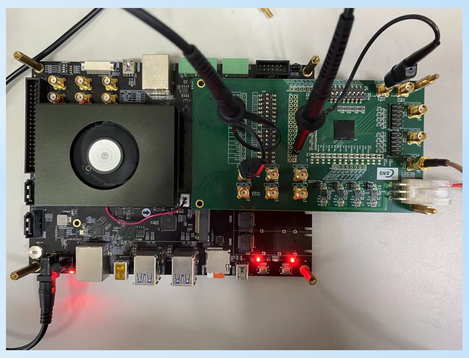


the PDHASIC Front-end Test PCB Layout

the Photograph of the PDHASIC Die



the Photograph of the Test Set-up



the FPGA Development Board and the Front-end Test Board

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