Performance of the Analog Pixel Test Structure in 65 nm TPSCo CMOS imaging technology for the ALICE ITS3

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Abstract

Thanks to the reduced production expenses and the undemanding manufacturing process, Monolithic Active Pixel Sensors (MAPS) represent appealing candidates for radiation imaging applications and for the design of high-performance silicon vertex and tracking detectors of high-energy physics experiments. In the context of future detector upgrades for the HL-LHC at CERN, the R&D initiative on monolithic sensors of the CERN Experimental Physics Department, together with the ALICE ITS3 (Inner Tracking System) upgrade project, developed the MLR1 (Multi Layer per Reticle) submission to validate the Tower Partner Semiconductor Co. 65 nm technology. Among the three different test structures belonging to the MLR1 submission, the Analog Pixel Test Structure (APTS) allows a direct analogue readout of the pixels. The APTS chip measures 1.5×1.5 mm^2 and it comprises a 6×6 pixel matrix with pitch ranging from 10 to 25 μm. Two different versions of the output buffer were designed: a source-follower (APTS-SF) and an operational amplifier (APTS-OA), the latter addressed to measure the time resolution. In-beam measurements proved that the analogue structures show a detection efficiency above 99% for all the investigated pixel pitches at thresholds as high as 150 e^-. The performance remains unchanged after a Non-Ionizing Energy Loss irradiation level of 10^{14} 1 MeV neutron equivalent cm^{-2}, above the ALICE ITS3 requirements. Moreover, the analogue test structure equipped with fast individual operational amplifier-based buffering shows a time resolution as low as 63 ps, well below the one reached with the 180 nm CMOS process, paving the way for other applications in addition to the high energy physics.