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SPHIRD: readout controller and communication protocol –design and implementation

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SPHIRD ASIC is dedicated to high count rate single photon counting operation at the European Synchrotron Radiation Facility with Extremely Brilliant Source. The prototype IC has a matrix of 64×32 pixels with 50µm pitch. Pixel front-end electronics employs novel pile-up compensation techniques [1], while pixel logic uses relocation algorithms to increase spatial resolution [2]. This paper focuses on readout controller, responsible for matrix readout and implementing a dedicated communication protocol.

Communication with imaging sensors is asymmetric in its nature. Configuration, calibration and control data has to be sent to the sensor. These transfers are typically not time-critical or are composed of relatively short commands, hence a single, source-synchronous link is sufficient. However, in the other direction, it is desired to transfer image data as fast as possible, thus a high-speed, multigigabit serializer is a preferred option.

Having that in mind, the developed controller is divided into two parts: control path and readout path. Control path is responsible for loading configuration data to the pixel matrix and controlling chip operation. This path is bidirectional - it allows also to read image data at lower speed. Readout path on the other hand is unidirectional and designed for high data throughput. It uses an on-chip 4-lane serializer together with PCS (Physical Coding Sublayer), capable of line rates of 4Gbps per lane. Additionally, it has a configurable FSM (Finite State Machine), which allows for pixel matrix readout with different readout modes, pixel data lengths etc.

The controller has been successfully launched and tested. At the conference, we will present the main goals and requirements for the controller and the communication protocol, the partitioning of functionality between the integrated circuit and the reading system, and describe the implementation details.

1. P. Grybos et al., "SPHIRD–Single Photon Counting Pixel Readout ASIC With Pulse Pile-Up Compensation Methods," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 9, pp. 3248-3252, Sept. 2023, doi: 10.1109/TCSII.2023.3267859
2. P. Otfinowski et al., "Increasing the Position Resolution in Single Photon Counting Pixel Readout IC by Real-Time Interpixel Communications," in IEEE Transactions on Circuits and Systems II: Express Briefs, doi: 10.1109/TCSII.2024.3372884.

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