R&D of a Generic Readout Platform Based on the Modern SoC Architecture for CSNS

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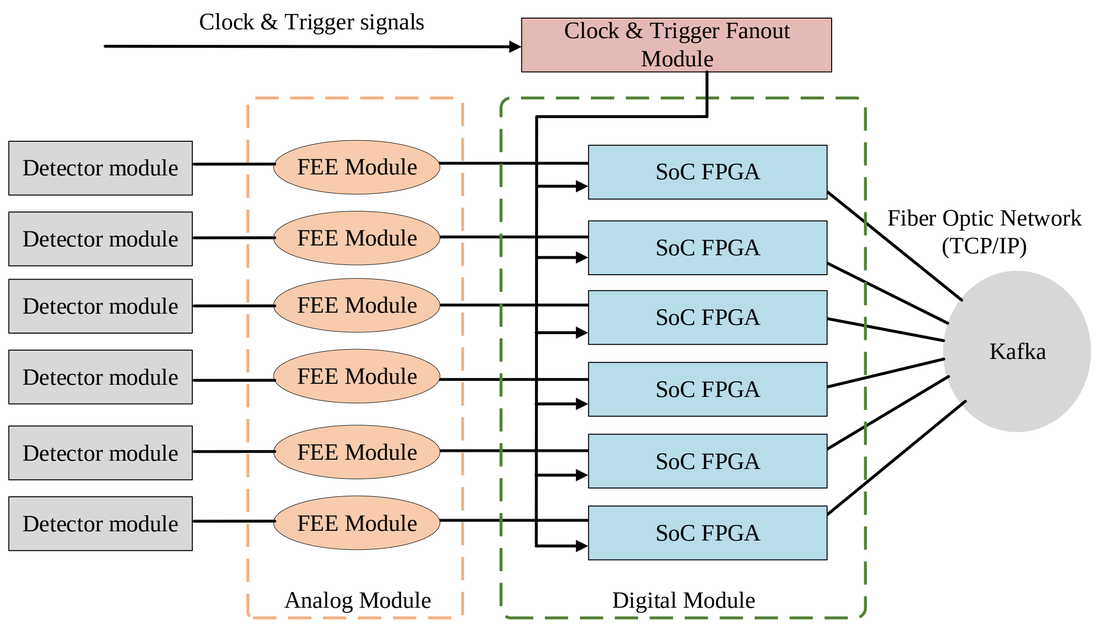
Introduction

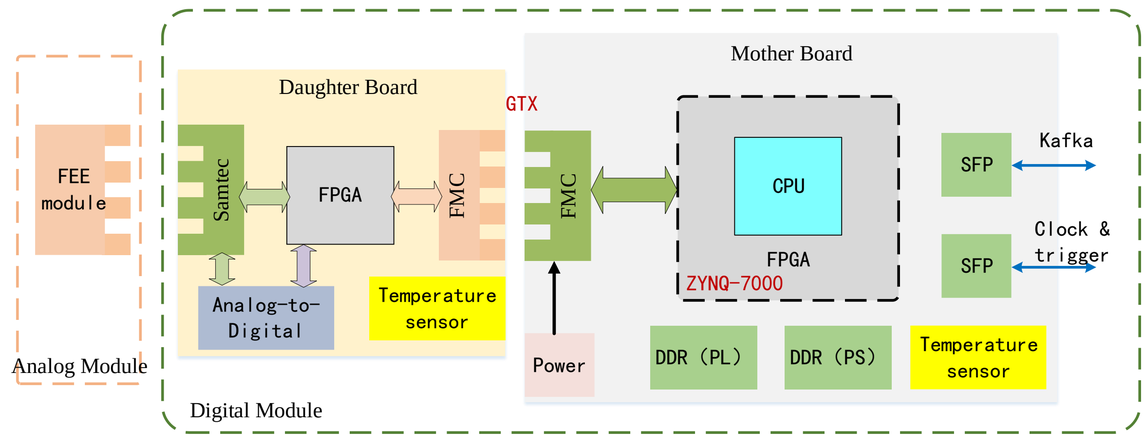
To address complexities arising from the various readout electronics for different neutron detection or imaging system, a general readout electronics platform is introduced in the paper, which can greatly reduce the difficulty of designing and maintaining readout electronics for Chinese Spallation Neutron Source (CSNS). The fundament thought of the general readout electronic platform is achieved through the cooperation of analog and digital modules. The analog module is used to condition the input signal in order to improve the signal-to-noise ratio. The digital module is a system-on-chip (SoC) solution, which can facilitates the following functionalities: analog-to-digital conversion, digital signal processing, communication and providing embedded Linux system for software development. The introduction of SoC architecture make the general readout electronics platform become a more modern system, which can flexibly achieve the data analysis, physical information extraction and access to data stream-processing platform, such as Apache-Kafka. As well as provide a brand new perspective on the process of developing next-generation neutron spectrometers software and hardware readout system.

IMPLEMENTATION

➢ Structure of Readout electronics:



In order to alleviate the pressures of designing the readout electronics in the construction stage of neutron spectrometer at Chinese Spallation Neutron Source (CSNS), a general readout platform will be used, which is implemented by a distributed architecture in accordance with the modular detector system. The distributed architecture of general readout electronics platform can provide a flexible deployment and convenient management for the experiments, as shown in figure 1. Every detector module matches a readout electronics module which is composed of an analog module and a digital module. The global clock signals and trigger signals are received by clock & trigger fanout module, which can fan them out to the entire readout system to achieve data alignment and data selection. The scientific data, command data and status data communicate with Apache-Kafka over gigabit optical network implemented with SoC FPGA technique.

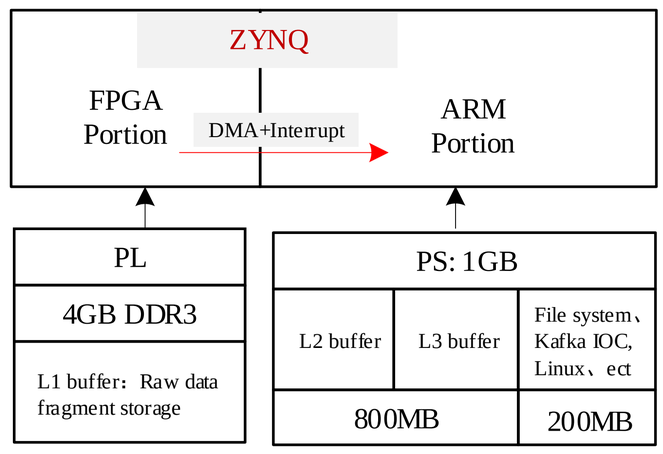


The digital module is composed of daughter board and mother board, as shown in figure 2. To meet various requirements of different detector systems, analog module and daughter board can be specifically designed. The mother board will be designed as a general module which can adapt to different detector system. In this way, the generality of readout electronics is not only reflected in the readout architecture, but also in that important modules can be share.

The daughter board is responsible for both configurating/controlling the analog module and converting the analog signal to digital signal. The mother board is implemented with SoC FPGA technique which can inherited the advantages of FPGA and provide ARM for software development. The introduction of ARM gives an implementable way to interact with Apache-Kafka, as well as allows readout electronics to calculating data flexibly and controlling the entire readout system intelligently. The communication between daughter board and mother board through FPGA Mezzanine Card (FMC) and implemented with the gigabit transceiver.

The data flow of readout electronics, especially the mother board, is shown in figure 3. Firstly, storing the raw data fragment in L1 buffer. Secondly, reconstructing physical event in L2 cache and L3 cache. Finally, sending the scientific data to Apache-Kafka. In order to ensure the space of L2/L3 buffer is enough for running data analysis software, as well as reducing the computational pressure of ARM.

L1 buffer is put on PL side of SoC FPGA which can offer 4GB storage space, large enough to solve the difficulty of ARM portion. Data transmission between PS and PL of SoC FPGA is realized by DMA + Interrupt.



Conclusions

In this work, we present a readout electronics design that is implemented based on SoC architecture . and this readout electronic have been successfully applied in ERNI and EMD spectrometers, and will be promoted for use in other spectrometers in the future.

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