Contribution ID: **92** Type: **Poster**

Design and Validation of the DAQ hardware for MAPS based telescope readout

Wednesday 3 July 2024 14:09 (1 minute)

MIC series MAPS ASIC are being designed at CCNU for a few physics experiments. A flexible chip readout and DAQ system is under the development, to support the chip evaluation and the readout of telescope with multiple modules. The system includes a front-end kit CARO and a back-end PCIe based system PiDAQ. CARO is based on the AMD Kria K26 SOM, while PiDAQ is based on the AMD Versal Prime series FPGA VM1402. The main features of PiDAQ board contains: PCIe Gen4×8 bus support throughput up to 14.76 GB/s; two DDR4 on-board memory to support data buffering with the bandwidth faster than 37.7 GB/s; two QSFP28 cages to support up to 8 bidirectional links, with a throughput up to 25 GB/s. PiDAQ is able to interface up to eight CARO modules in future telescope. This poster introduces the design details and preliminary validation of the PiDAQ hardware, firmware, and software.

Primary author: LIANG, Qiming (Central China Normal University)

Co-authors: CHEN, Kai (Central China Normal University); XIAO, Le (Central China Normal University CCNU (CN)); YIN, Weigang (IHEP, CAS); LANG, lei (Central China Normal Unversity)

Presenter: YIN, Weigang (IHEP, CAS)

Session Classification: Poster Session