Characterization of silicon Monolithic Stitched Sensors for ALICE ITS3 in view of LHC Run 4

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ALICE Inner Tracking System for LHC Run 4

- A new Inner Tracking System **ITS3** will replace the innermost layers of the ALICE ITS2 during LHC Long Shutdown 3 (2026-2028)
- **Reducing material budget down to 0.086 % X_0 per layer**, more homogeneous distribution of material over the azimuth as for ITS2

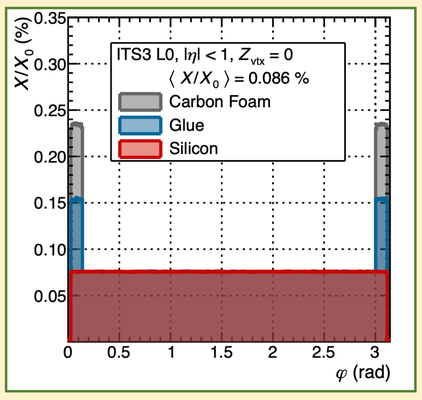

Fig. 1: Material budget of ITS3 Layer 0 [1]

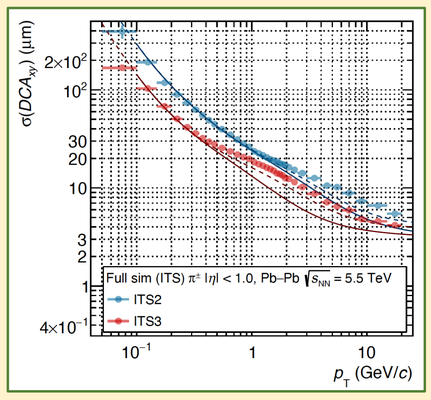

Fig. 2: Simulated ITS2/ITS3 ponting resolution [1]

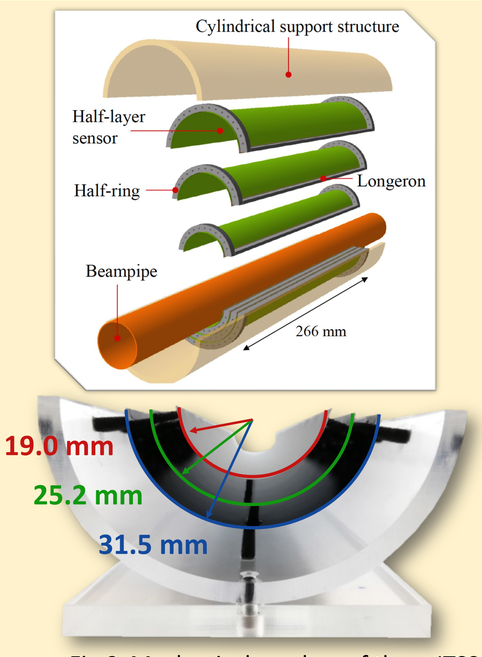

Fig 3: Mechanical mockup of three ITS3 half-layers [1,2]

- Significant **improvement of tracking resolution**, especially for low transverse momenta (*Fig. 1*)
- 3 **truly cylindrical, wafer-sized, self-supporting** half-layers
- Each half-layer consists of **ultra-thin** (≤ 50 μm), **large-area** (10 cm × 26 cm), flexible MAPS (*Fig. 3*)

Beampipe inner/outer radius (mm)	16.0/16.5		
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	19.0	25.2	31.5
Length (sensitive area) (mm)	260	260	260
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm^2)	305	407	507
Pixel sensors dimensions (mm^2)	266 × 58.7	266 × 78.3	266 × 97.8
Number of pixel sensors / layer		2	
Material budget (%X_0 / layer)		0.07	
Silicon thickness (μm / layer)		≤50	
Pixel size (μm^2)		$O(20 \times 22.5)$	
Power density (mW/cm^2)		40	
NIEL (1 MeV n_{eq} cm^{-2})		10^{13}	
TID (kGray)		10	

[a] The pseudorapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point ($z = 0$).

Fig. 4: ITS3 general parameters and requirements [1]

Submissions towards a truly-cylindrical, wafer-sized, nearly massless detector

Multi-Layer Reticle 1
Successfully validated the use of the **TPSCo. 65 nm CMOS technology** for HEP

Engineering Run 1
First submission **of large-scales stitched MAPS** prototypes: MOSS, MOST

Engineering Run 2
Full size & functionality prototype for the final ITS3 sensor**:** MOSAIX

Engineering Run 3
Final Sensor to be used in ITS3

Pixel Test Structures of the Engineering Run 1 (ER1)

MOnolithic Stitched Sensor (MOSS)

Sensor layout:
- Chip size: **14 mm x 259 mm**
- **6.7 million pixels** organised in **10 Repeated Sensor Units** (RSUs)
- Each RSU hosts 8 pixel matrices (regions)
  - 4 x 256 x 256 pixels with 22.5 μm pitch
  - 4 x 320 x 320 pixels with 18.5 μm pitch
  - Matrices include different front-end implementations

Scope:
- **define the layout and stitching parameters** for the subsequent full, wafer-scale MAPS
- First **yield and uniformity studies** of the stitched sensor production
- **Characterisation** of the pixel-matrix front-end

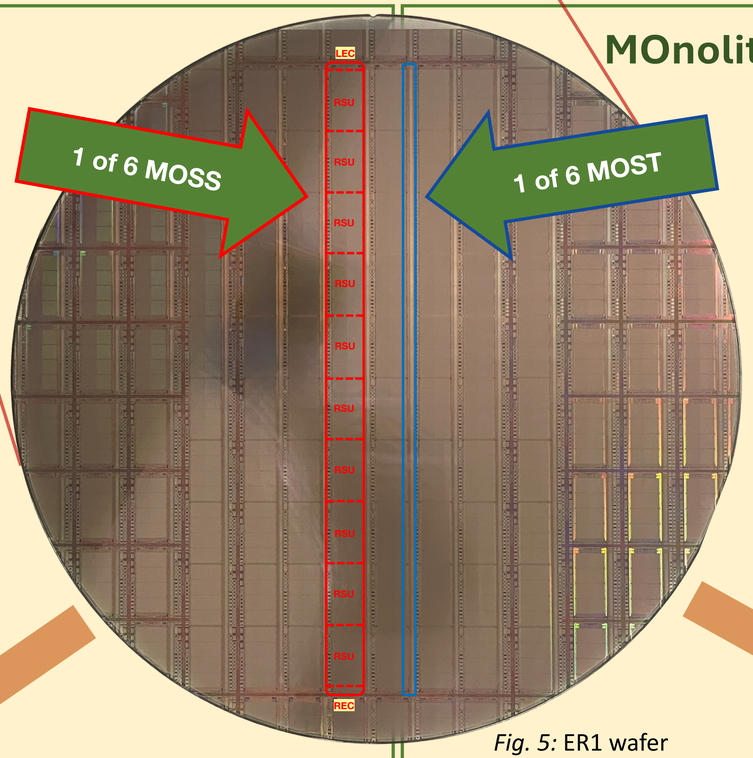

Fig. 5: ER1 wafer

MOnolithic Stitched Sensor with Timing (MOST)

Sensor layout:
- Chip size: **2.5 mm x 259 mm**
- **0.9 million pixels** with **18 μm pitch**

Scope:
- Testing production with **high integration density in pixel** and testing of detaching subsets of pixels with power switches to handle possible shorts
- Testing transmission quality of high-speed data over full length of the ITS3

Results:
- Verified high-speed data transmission of **1 Gbit/s over the full length of the ITS3**

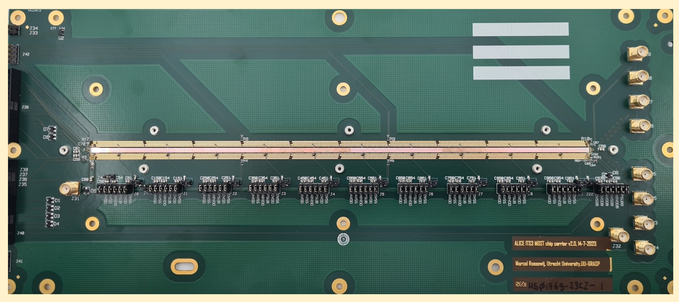

Fig 7: MOST bonded on a carrier card

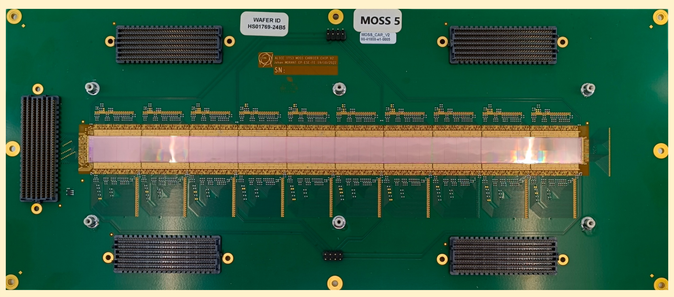

Fig. 6: MOSS bonded on a carrier card [1]

First yield assessment results:
- Wafer-to-wafer variation, but significant numbers of wafers show yield compatible with ITS3 requirements
- Only observed failure mode is shorts in top metals → will be resolved for ER2

First Characterisation results:
- MOSS can be operated with above **99% efficiency** while maintaining **<10^{-6} pixel^{-1} event^{-1} fake-hit rate** (ITS3 requirement)
- First assessment of the spatial resolution shows < 6 μm resolution (dedicated study to be carried-out)

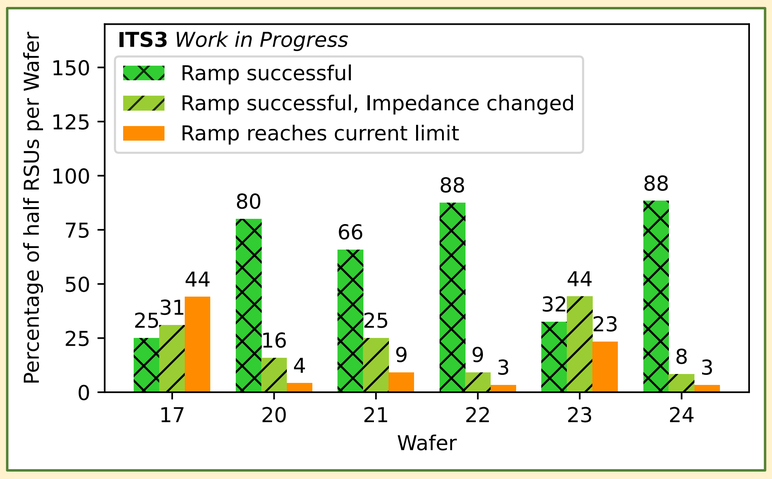

Fig 8: Yield assessment of the MOSS power ramping

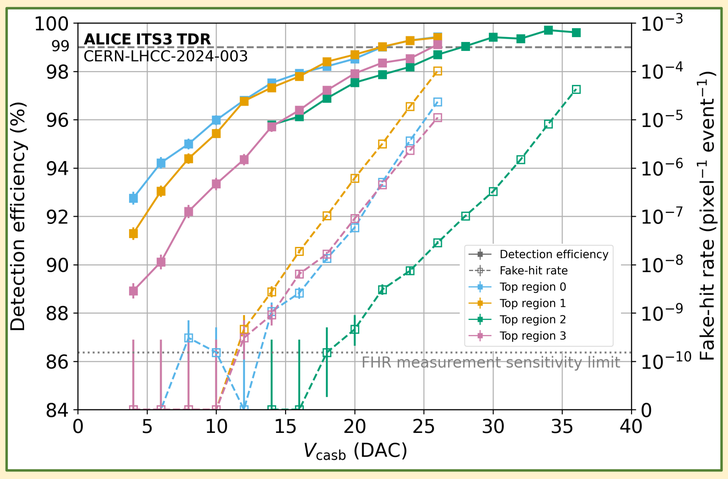

Fig 9: In-beam performance of a non-irradiated MOSS [1]

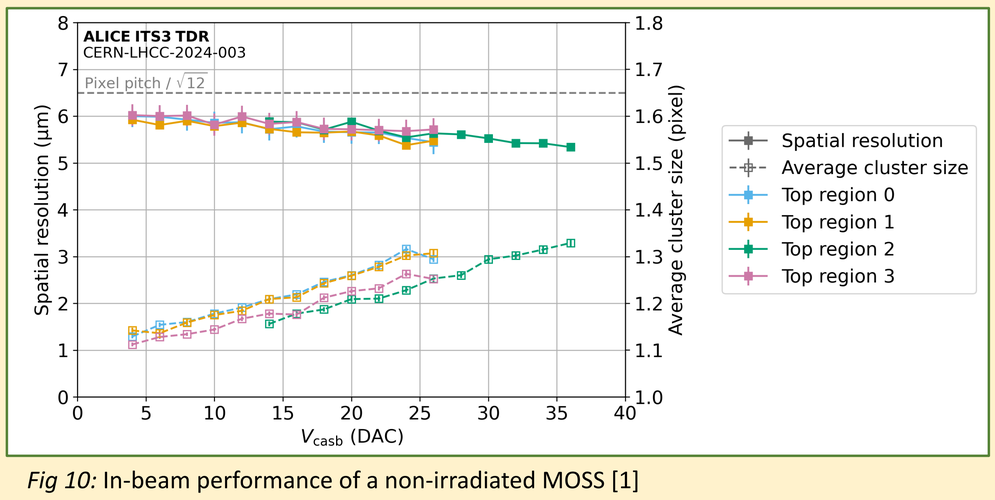

Fig 10: In-beam performance of a non-irradiated MOSS [1]

References

[1] Technical Design Report of the ITS3 – A bent wafer-scale monolithic pixel detector, ALICE Collaboration, December 11, 2023, Journal of Physics G: Nuclear and Particle Physics, (8):087002, jul.
[2] Letter of Intent for an ALICE ITS Upgrade in LS3, ALICE Collaboration, September 8, 2019

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Conclusion and Outlook

- Technical Design Report of ITS3 **approved by CERN LHC Comitee (LHCC)** and the CERN Research board (RB)
- **ER1 sensors are working** and are currently characterised:
  - Yield prediction for ER2 complies with ITS3 requirements (based on ER1 experience)
  - MOSS operable with >99% efficiency maintaining <10^{-6} pixel^{-1} event^{-1} fake-hit rate
- ER2 design is currently finalised
- **ITS3 will be installed during the Long Shutdown 3** (2026 – 2028)