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Preparing ATLAS for the High-Luminosity LHC: System Testing and Performance Evaluation of the ITk Strip Detector

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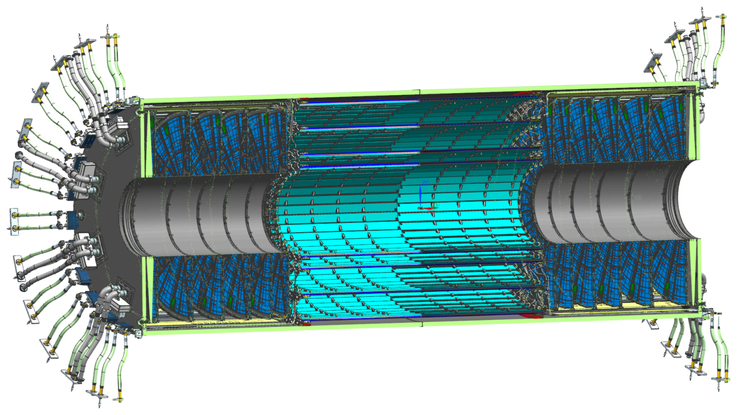
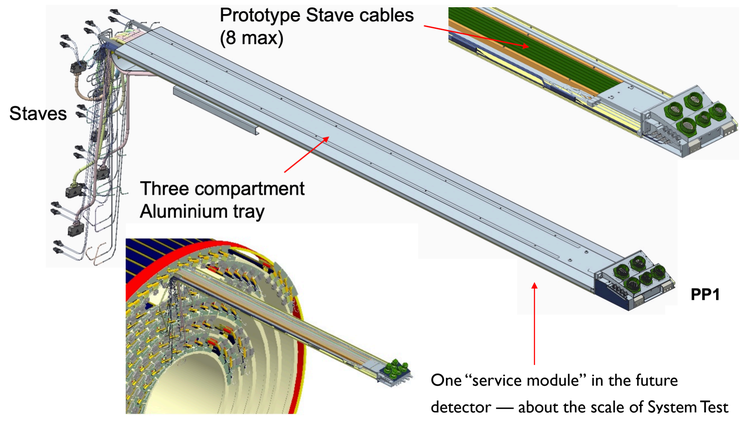
Abstract

The new ATLAS Inner Tracker (ITk) will replace the current tracking system in ATLAS to cope with the challenging conditions during the high-luminosity phase of the Large Hadron Collider. ITk is an all-silicon detector consisting of a pixel inner tracker and a silicon microstrip outer tracker. This contribution focuses on the results of the large-scale system testing of the ITk strip detector, which is the testbed for verifying the design and evaluating the performance of detector components prior to production. This setup is also being used to develop detector control and data acquisition systems required for the eventual operation of the ITk Strip detector.

Two setups at CERN and at DESY (Hamburg/ Germany) target the design verification of the central barrel section around the interaction point and the end-cap section covering the forward region. In both setups, silicon sensors mounted on support structures are connected to electrical, optical and cooling services as realistic as possible as in the latter detector integration. As such it is possible to validate the detector design, verify the detector DAQ and perform tests with the services, e.g. concerning the dual-phase CO_2 cooling. This contribution gives an overview of the developed system tests for the ITk strip detector, summarises the current status of the two sites, and shows a selection of performance measurements.

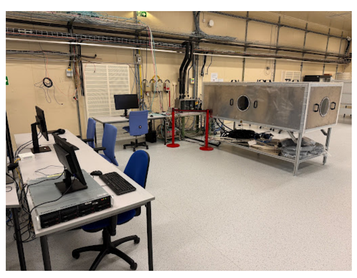


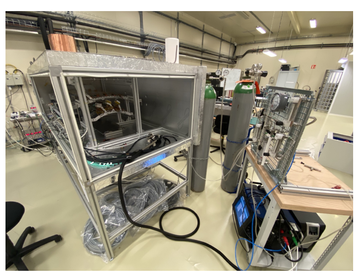


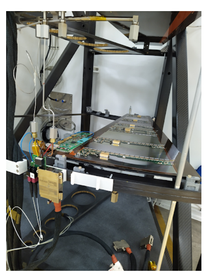
Overview

ITk is a part of the upcoming Phase-II upgrade of ATLAS detector. It is designed to meet the extreme challenges of data-taking in High Luminosity Large Hadron Collider (HL-LHC): hard radiation, high rate and large volume of read-out data.

- The ITk Strips project is about to begin the production of the detector components and start the integration of the detector in the second half of 2025.
- The System Tests are prototype implementations of the smallest independent unit of the ITk Strips detector components in the Barrel (CERN) and the Endcaps (DESY). Their feedback is crucial for the production and development of all detector components : hardware, electronics, software.
- To enable development and long-term maintenance of the readout system, ATLAS employs a system based on commercial off-the-shelf components: AMD/Xilinx-based Frontend Link Exchange (FELIX) firmware, RDMA infiniband network based on Nvidia/Mellanox products, and Intel Xeon CPUs.



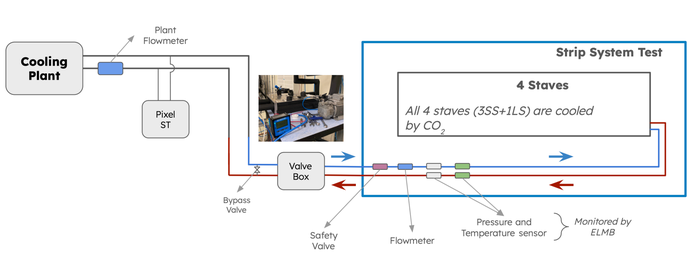


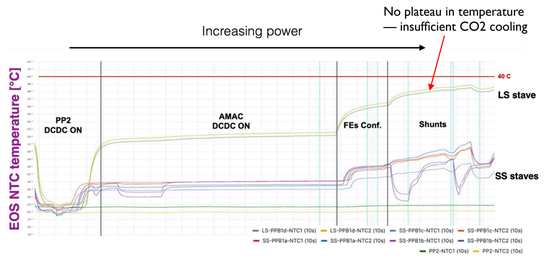


ITk Strips system tests

The system test is composed of all components of the detector, providing a “final dress rehearsal” for their commissioning and reviews:

- CO_2 dual-phase cooling (-25°C), with titanium capillaries and custom welding process
- Testing the power chain: ISEG PSU, Patch Panel 2 (PP2) with custom monitoring & control ASICs (AMAC). And Electro-magnetic compliance (EMC) tests.
- Safety: custom hardware interlock for the environment control: Local Interlock Safety SYstem (LISSY), with CAN-based environment monitoring (ELMB2 board).
- On-detector components: the safety and control (AMAC chips), and data-taking electronics (HCC & ABC Star)

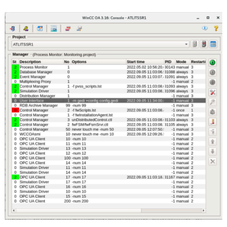


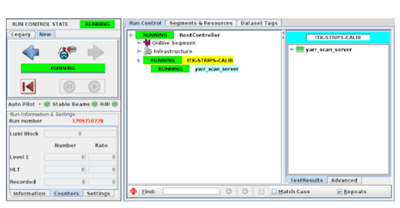


Large scale software operations

The operations in the system test and future detector are supported by large scale orchestration software:

- Detector Control System (DCS) — safety of the detector operation; based on industry standards OPC-UA and WinCC SCADA system, with additional CERN-specific frameworks. Plus InfluxDB & Grafana monitoring.
- Data Acquisition (DAQ) — ITk-specific software Yet Another Rapid Readout (YARR) within ATLAS-specific TDAQ framework that provides services and orchestration of DAQ processes.
- A custom object relational database ConfigDB on top of OpenAPI for large system configuration.

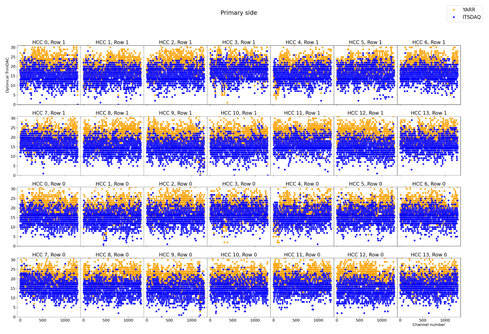




Detector calibration and diagnostic data

The ITk Strips chips that collect the physics data (HCC and ABCs “hybrid” frontends) require careful calibration and diagnostic monitoring..

- ITk Strips employ ITSDAQ package of firmware+software in the production and development of the frontends.
- The ITSDAQ operations are ported to Yet Another Rapid Readout (YARR) project, which is used to handle the Strips chips with FELIX readout system at large scale. The same software is used in ITk Pixels production.
- The system test serves as test bench to commission and further develop the software operations.



Data-taking in HL LHC

High Luminosity LHC (HL-LHC) will produce events at about 1MHz trigger rate. ITk Strips physics data stream consists of many tiny packets:

- A packet from 1 Frontend = about 48 Bytes in physics data taking, and about 1200 Bytes in calibrations
- About 14 Frontends per 1 optical link with 10 Gbps bandwidth (the GBT protocol)
- 24 optical links per 1 FELIX card; and ITk Strips needs about 70 such cards

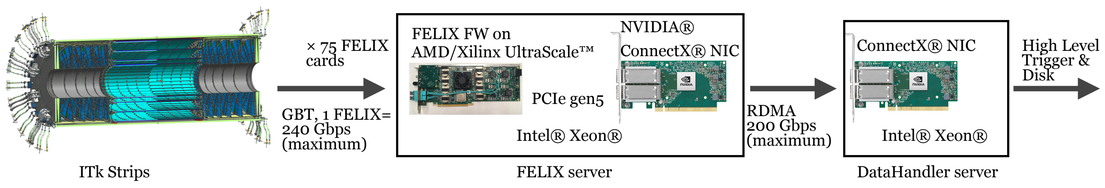
I.e. 1 FELIX card transmits a packet of 48 Bytes at about 336 MHz rate. Assuming 4GHz CPU clock, the DataHandler has about 12 CPU clock cycles to process it.

The system must also have a performance margin up to 2MHz trigger rates.

FELIX-based readout system

The FELIX system transfers functionality from hardware to software & commercial off the shelf components, for eade of development and maintenance:

- Detector data is sent over Gigabit Transceiver protocol (GBT) to Xilinx-based (Kintex Ultrascale) board with custom firmware: frontend link exchange (FELIX).
- FELIX card transfers the data to the host system via DMA (Wupper open source IP).
- The host CPU finds the data packets in the received blocks of memory, and pushes them to subscribed clients over Nvidia/Mellanox (ConnectX-5) 200Gbps infiniband RDMA network.
- The RDMA data is passed with a custom message protocol handled by a custom client library, netio-next and FelixClient respectively, built on top of industry standard libfabric.
- An enterprise-grade CPU server (Intel Xeon) runs detector specific software to interpret and act on the data.



CPU performance at high rate

To sustain the multi-MHz data rate:

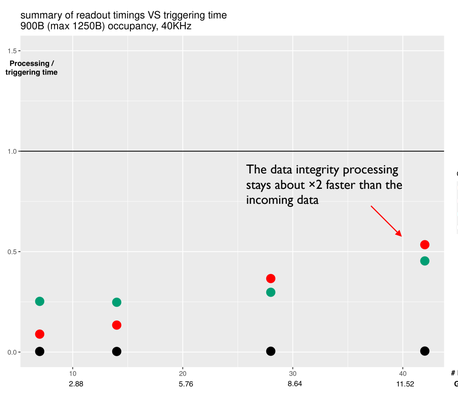
- Utilise the parallelism in RDMA hardware: Mellanox network cards can maintain multiple RDMA connections..
- CPU cache-friendly algorithms and data-structures for multi-threaded processing.
- Hide latencies by buffering the data.

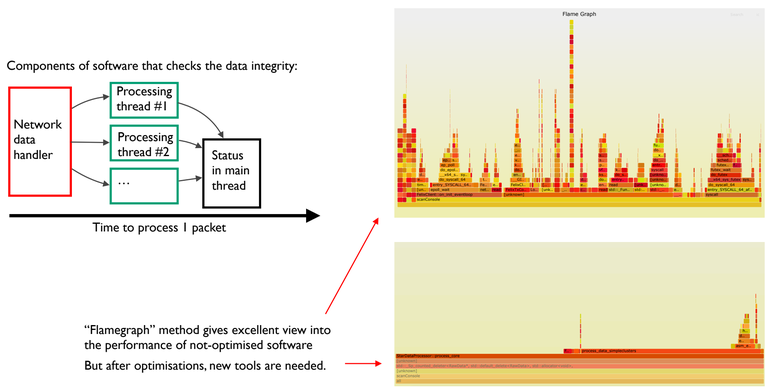
Algorithms & data structures: an array of single producer single consumer queues based on open source ring buffer SPSCQueue or a modified version of Boost memory pool that is used in ATLAS.

Comprehensive measurements are vitally important for performance evaluation:

- Measurements on the system test setup are compared to software emulated benchmarks with gradually increasing complexity.
- Standard tools: Linux perf, AMD uProf & Intel VTune.
- The hardware clock counter TSC in x86 processors for fine time measurements.

The most telling metric is simple time measurement of how long it takes for different software components to process a packet VS the rate of the packets stream.





Outlook

Integration of the detector is expected to start in the 2025. The development of the integrated operations will expand to meet the milestones during the integration and further in the final detector.

The system test serves as a test bench to verify the quality and explore the performance of the system.

The system test work is additionally supported by firmware and software emulators of the detector components.

More information:

ITk Strips Technical Design Report
https://cds.cern.ch/record/2257755?ln=en

Design, development, characterisation and operation of ATLAS ITk strip staves
https://ora.ox.ac.uk/objects/uuid:16ea0c42-8bae-482d-bfbc-e1d898124461

ATLAS DAQ software (SWROD)
https://gitlab.cern.ch/atlas-tdaq-software/swrod

FELIX project
https://atlas-project-felix.web.cern.ch/atlas-project-felix/

YARR project
https://gitlab.cern.ch/YARR

SPSCQueue package
https://github.com/rigtorp/SPSCQueue