Design of a Time to Digital Converter for LGAD detector at HIAF complex

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The High-Intensity Heavy-ion Accelerator Facility (HIAF) is a leading platform for heavy ion scientific research in China with advanced beam current indicators. Several physics experiments such as the Electron-ion collider in China (EicC), the China Hyper-Nuclear Spectrometer (CHNS), the High energy FRagment Separator (HFRS) are being under construction at HIAF. To measure the position, energy deposition, and arrival time of particle hit in these experiments, Low-Gain Avalanche Detectors (LGAD) have become the detector of choice due to an excellent performance. The readout circuit of LGAD requires time-to-digital converters (TDC) to convert the time measurement results into digital signals. Thus, the performance of TDC is crucial for the readout circuit. Since smaller pixel area is conducive to improving positional resolution and spatial resolution, a TDC using a calibration module instead of DLLs is proposed to achieve lower power consumption and area.

The proposed TDC is a 3-stage architecture, the first stage uses a high-speed counter TDC, achieving a large dynamic range; the second stage is a delay-line TDC, which balances between the dynamic range and resolution; the last stage is a vernier delay-line TDC, achieving a high resolution. The 3-stage architecture achieves both large dynamic range and high resolution. In addition, a calibration module is used to measure the relationship between two adjacent stages of resolution, thus, the resolution of the TDC could be confirmed under the influence of PVT variation. Compared with the TDCs using DLLs, the proposed TDC reduces the power consumption and area.

The resolution of TDC is about 5.13 ps, and the dynamic range is 25.2 ns. The INL and DNL are both less than 0.3 LSB. Including two TDCs which measure the TOA and TOT respectively, the layout area is 931*447 μm^2.