Design of a Time to Digital Converter for LGAD detector at HIAF complex

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Introduction

The High-Intensity Heavy-ion Accelerator Facility (HIAF) is a leading platform for heavy ion scientific research in China with advanced beam current indicators. To measure the position, energy deposition, and arrival time of particle hit in these experiments, Low-Gain Avalanche Detectors (LGAD) have become the detector of choice due to an excellent performance. The readout circuit of LGAD requires time-to-digital converters (TDC) to convert the time measurement results into digital signals. Thus, the performance of TDC is crucial for the readout circuit. Since smaller pixel area is conducive to improving positional resolution and spatial resolution, a TDC using calibration modules instead of DLLs is proposed to achieve lower power consumption and area.

Overall architecture

The Proposed TDC shown in Figure 1 is a 3-stage architecture, the first stage uses a high-speed counter TDC, achieving a large dynamic range; the second stage is a delay-line TDC, which balances between the dynamic range and resolution; the last stage is a vernier delay-line TDC, achieving a high resolution. The 3-stage architecture achieves both large dynamic range and high resolution. In addition, calibration modules are used to measure the resolution relationship between two adjacent stages, thus, the resolution of the TDC could be confirmed under the influence of PVT variation. Compared with the TDCs using DLLs, the proposed TDC reduces the power consumption and area.

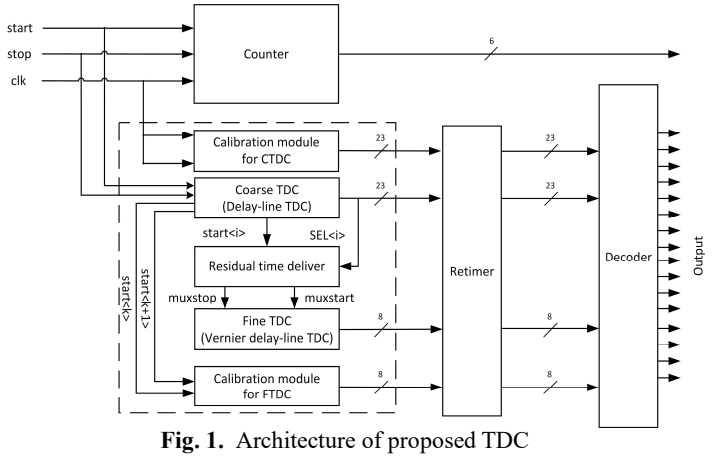

Fig. 1. Architecture of proposed TDC

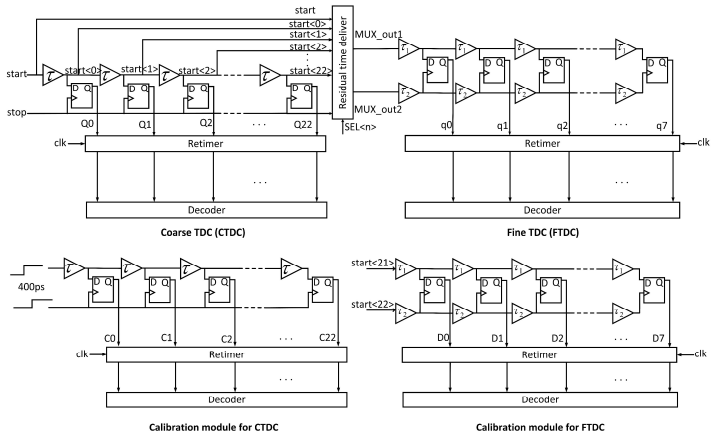

Fig. 2. Architecture of the second and the third stage

Calibration method

As shown in Figure 2, calibration modules are used to measure the resolution relationship between two adjacent stages. The architecture of calibration modules are identical to the CTDC and the FTDC.

The input signals of the calibration module for CTDC are two step signals generated by the system clock, with a time interval of one clock cycle. While, the input signals of the calibration module for FTDC are generated by the CTDC, with a time interval of 1τ (the resolution of the CTDC). Thus, the resolutions of the CTDC and the FTDC can be calculated from the output results of the calibration module and the time interval of the input signals.

Performances

The TDC is designed in a 55 nm process. **Shown in Figure 3**, including two TDCs which measure the TOA and TOT respectively, the **layout area** of the TDC is **931×447 μm²**. With a **2.5 GHz** system clock, **the resolution of TDC is about 5.13 ps**, and **the dynamic range is 25.2 ns**. The INL and DNL are both less than 0.3 LSB.

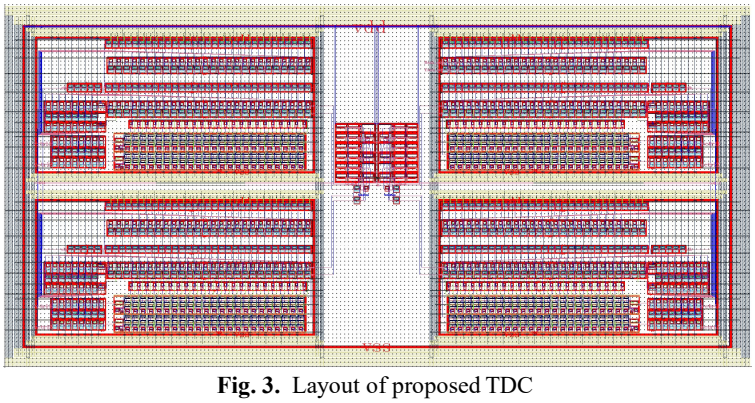

Fig. 3. Layout of proposed TDC

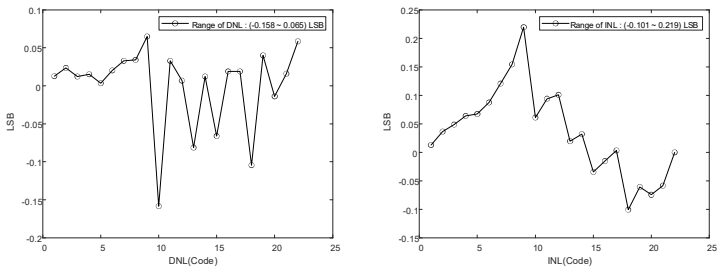

Fig. 4. INL and DNL of proposed TDC

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