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Development of a Clock and Data Recovery (CDR) ASIC for heavy-ion physics experiments

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The Heavy Ion Research Facility in Lanzhou (HIRFL) and the High Intensity heavy-ion Accelerator Facility (HIAF) are essential platforms for heavy-ion scientific research in Asia. Some experimental facilities are currently under construction at HIRFL and HIAF, such as the CSR External-target Experiment (CEE), the High energy FRagment Separator (HFRS), the China Hyper-Nuclei Spectrometer (CHNS), and the Electron-ion collider in China (EICC). These projects aim to enhance advanced experimental conditions for research in heavy ion physics and related interdisciplinary fields. In the context of large-scale scientific experimental facilities, as the collision energy increases rapidly, detector resolution improves, and trigger-less readout is implemented, higher demands have been proposed on the radiation resistance and transmission speed of the signal transmission links.

The advent of high-speed serial data transmission technology has significantly enhanced the transmission speed of links. A clock and data recovery (CDR) circuit can extract the clock information from high-speed serial data, and recover the clock to sample optimally at the center of a unit interval (UI), improving the quality of data transmission in physical experiments. Thus, a quarter-rate radiation-resistant CDR has been designed for large-scale physical experiments. The proposed CDR is based on a phase interpolation structure, consisting of a phase interpolator, eight high-speed samplers, two 4:120 Deserializers, a Bang-Bang phase detector, and a digital loop filter. The two-level structure phase-interpolator effectively enhances the precision of the interpolation clock. The customized three-level structure in the Deserializer guarantees the timing margin between the data and the clock. The pipeline-structure digital loop filter increases the data throughput rate of digital circuits. Furthermore, various strategies are considered to reduce the impact of radiation on the chip, such as triple-mode redundancy technology, modular design method, and reasonably modifying the layout of critical nodes.

The proposed CDR is designed in a 55 nm process and the input data rate is 20 Gbps. Ultimately, the bit error rate (BER) of the CDR is lower than 10e-12 and the power is less than 180 mW with a supply voltage of 1.2V.

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