Conceptual Design of TUPI (Timepix-based Ultra-fast Photon Imaging) Detector's Front-End Electronics

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TUPI (Timepix-based Ultra-fast Photon Imaging) is the new family of direct conversion and vacuum-compatible hybrid detectors under design at SIRIUS, the Brazilian 4th generation light source. Based on the Timepix4 [1] ASIC, it targets different kinds of experiments, such as tomography and spectrometry, and will be used in multiple bioimaging beamlines of ORION, Brazil's first Biosafety Level 4 (BSL4) Laboratory project, covering a wide energy range (5 to 45 keV) by using different sensors materials (Si, GaAs and CdTe). Designed in a modular approach to ensure scalability for constructing larger active areas in a compact form, each TUPI module will be composed by a set of 3x1 ASICs to provide approximately a 74 x 28 mm² sensitive area (1344 x 512 pixels of 55 µm pitch), streaming up to 44 thousand frames per second through up to 48 x 10.24 Gbps optical links directly connected to a Data Acquisition (DAQ) system.

Hardware Architecture

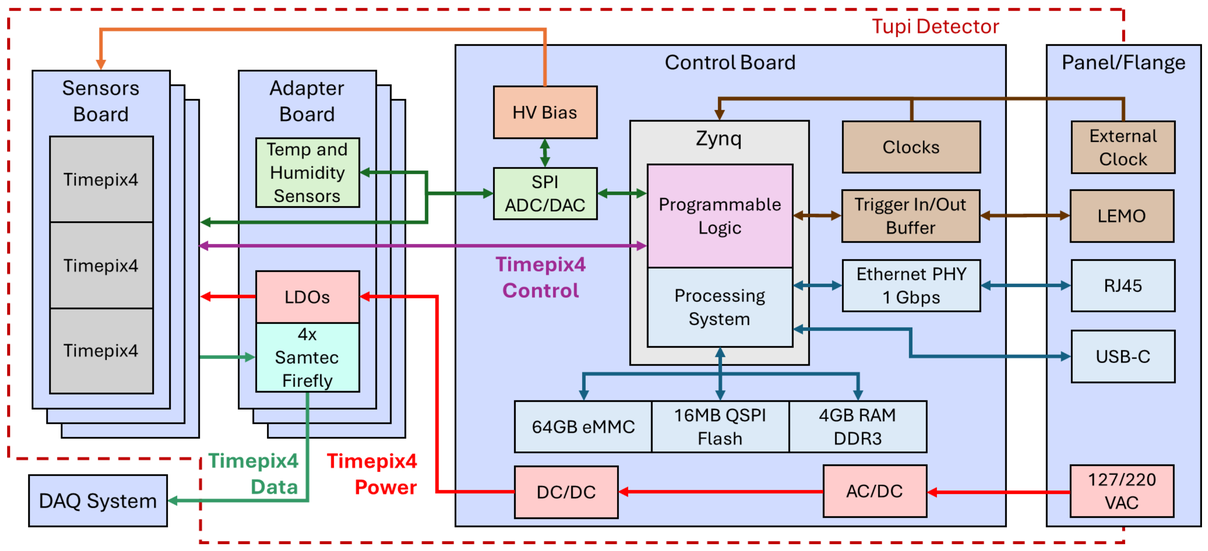


Figure 1 – TUPI`s Hardware Architecture

Sensors Board

The Sensors Board design supports varied sensors materials and hybridization modes: Slim edge or guard ring and single or multiple ASICs in monobloc. For TUPI modules, two types are planned with a fixed gap, as shown in Figure 2.

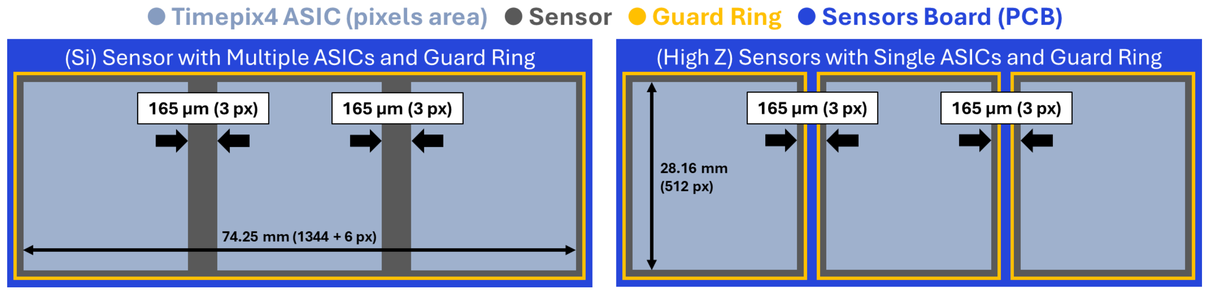


Figure 2 – Sensor's materials and hybridization types

The Timepix4 ASICs are available in two interconnection possibilities: Wire-bonding or TSV (Through Silicon Vias). Also, a high-voltage bias connection and thermal coupling are demanded from the board, as illustrated in Figure 3.

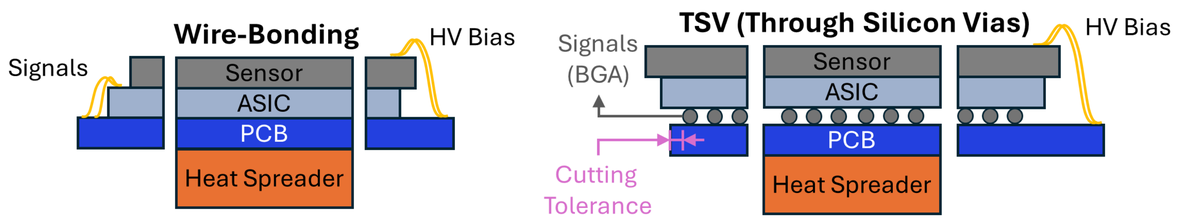


Figure 3 – Timepix4 electrical and thermal connections

For the wire-bonding PCB version, a Timepix4 footprint with pads had to be designed, while a BGA footprint was already available for the TSV. In both cases, the initial approach for applying bias voltage, limited to 2x modules side by side, is to connect at least one sensor and distribute it to the others, using a board edge aside by a gap of air or vacuum to meet the creepage for high-voltages (up to 1200 V) with shorten wire-bonds, as detailed in Figure 4.

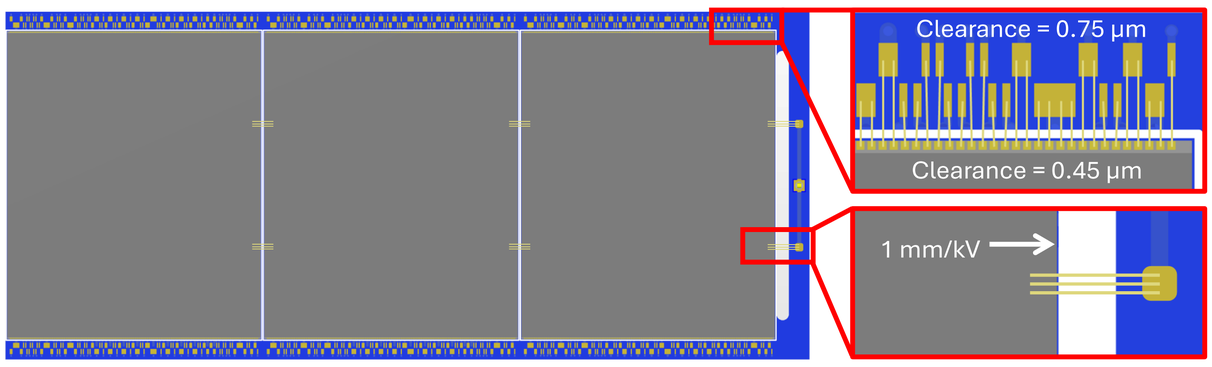
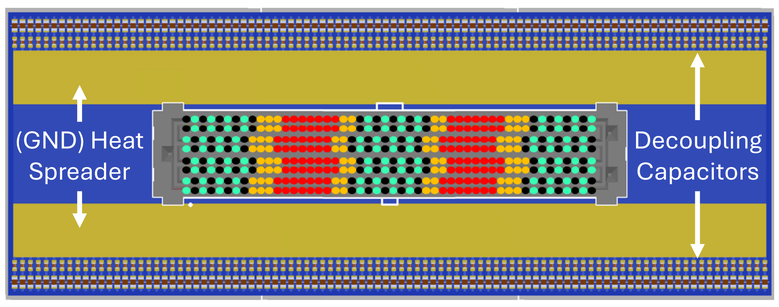


Figure 4 – Sensors Board edges design (Wire-Bonding PCB front view)

To interface all signals outside the Sensors Board, a single high-speed and high-density connector will be used: The Samtec 0.80 mm SEARAY. The distribution of its 400 pins is represented in Figure 5:



- **112 pins: GND (powering/shielding)**
- **112 pins: VDC**
- **96 pins: Data (48x high-speed links)**
- **80 pins: Control**

Figure 5 – SEAM8 pinout (TSV PCB back view)

This choice aims to save PCB area for heat spreader and sufficient decoupling capacitors, both crucial factors to ensure the ASICs proper functioning. Additionally, this configuration meets the maximum current requirement (18.5 A) for 3x Timepix4 ASICs, not exceeding the connector current carrying capacity (0.2 A/pin) [2].

Adapter Board

The Adapter Board was designed to split data, control and power in proper interfaces, as shown in Figure 6, converting all 48x 10.24 Gbps data links to optical fibers by using 4x Samtec Firefly's and providing stable DC voltages to the Timepix4 ASICs, keeping all LDO (Low Dropout) regulators as close as possible to improve voltage regulation and transient current capability.

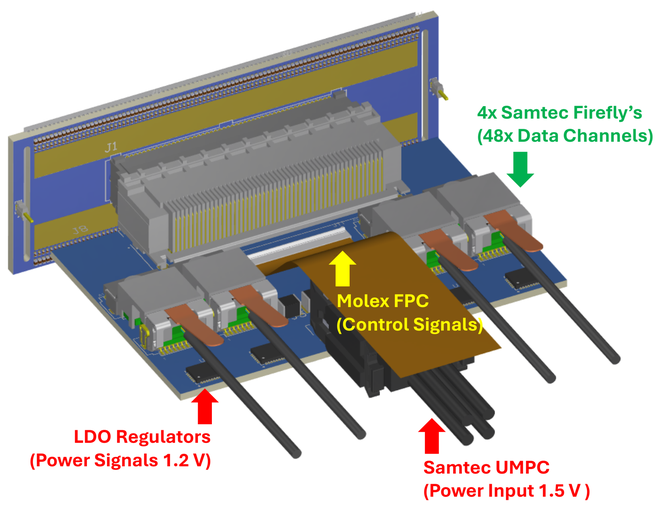


Figure 6 – Adapter Board

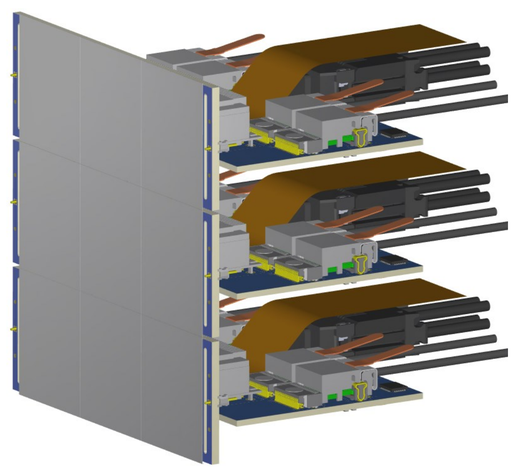


Figure 7 – Assembly of TSV TUPI modules

Furthermore, this PCB was designed to be completely covered behind the Sensors Board, allowing free arrangement of larger active areas and facilitating maintenance for each module, as shown in Figure 7. Moreover, this Adapter Board form factor enables the heat spreaders to reach the Sensors Board and cool down the Firefly's by a single water-cooled system.

Control Board

For the TUPI prototypes, it is planned to use the Avnet UltraZed-EG [3], shown in Figure 8, as the Control Board. It fulfills the number of I/Os and the main requirements detailed in Figure 1 to manage up to 3x TUPI modules. A custom Carrier Board will be designed to interconnect all UltraZed pins with Adapter Board interfaces and provide some missing elements (e. g. HV Bias source).

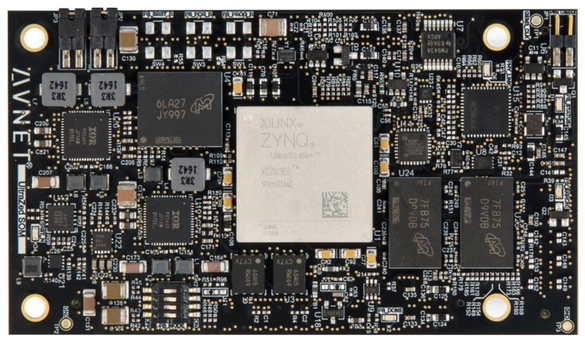


Figure 8 – AVNET UltraZed-EG. Author: AVNET [3]

Challenges and Future Developments

PCB materials (laminate and prepreg) definition:
- ❖ High thermal conductance;
- ❖ Low dielectric constant and loss tangent @ 10 GHz.

High-speed data links routing:
- ❖ Minimize mixed-signal effects (e. g. crosstalk and EMI);
- ❖ Minimize differential impedance mismatches to avoid reflections;
- ❖ Track length tuning to avoid skew and delay between channels.

Power Delivery System (PDS):
- ❖ Proper decoupling capacitors and power planes at PCB stack-up.

Proof of Concepts:
- ❖ Dummy board replacing ASICs by resistors for current and thermal tests;
- ❖ Board with high-speed data links loopback for signal integrity tests.

Acknowledgments

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References

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[2] Samtec, *Design Qualification Test Report 454284* (2015)
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