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Thin planar pixel detectors for highest radiation levels

L. Andricek, M. Beimförde, E. Fretwurst, C. Gössling, G. Kramberger,
G. Lindstroem, A. Macchiolo, M. Moll, H.-G. Moser, R. Nisius, R.H. Richter

» Proposal of a RD50 project

Institutes: CERN, Univ. Dortmund, Univ. Hamburg,

J. Stefan Inst. Ljubljana, MPI Munich

» Embedded within an ATLAS-Proposal for 3D integration

» Study of charge collection before and after radiation on pixelated readout nodes with different geometries and different sensor thicknesses – Check out the limits of planar detectors

» Status and plans

The Challenge

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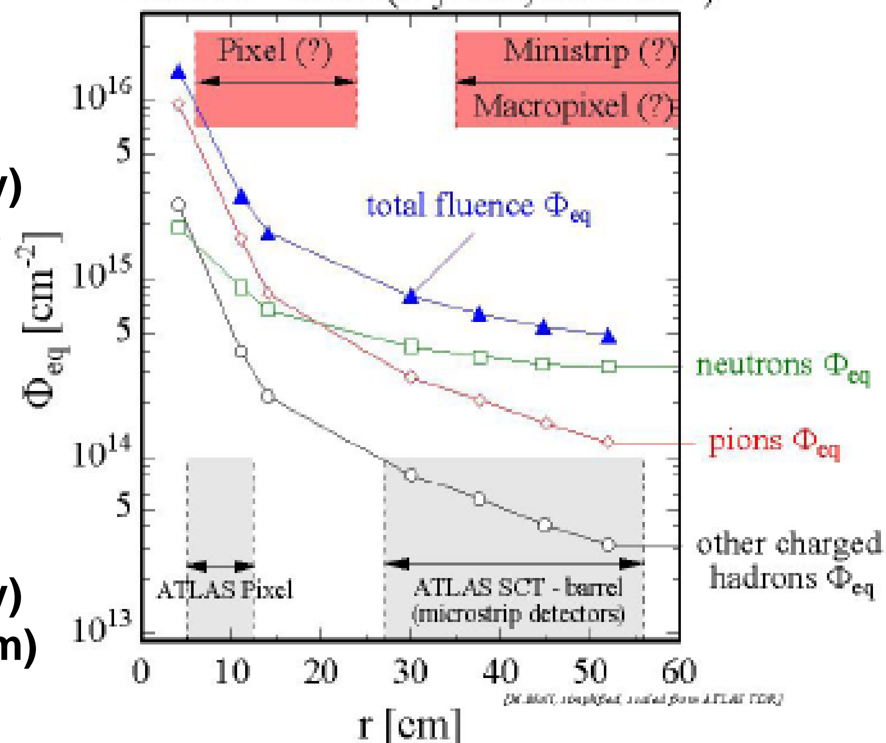
Expected conditions at LHC and sLHC

LHC:

- Start 2008
- L = 10^{34}cm^{-2}s^{-1}
- Integrated Luminosity: 500 fb^{-1} (10y)
- Fluence: 3x10^{15}cm^{-2} (1 MeV n, 4cm)
- Multiplicity: 0.5-1 k tracks/event

sLHC:

- Start 2016
- L = 10^{35}cm^{-2}s^{-1}
- Integrated Luminosity: 2500 fb^{-1} (5y)
- Fluence: 1.6x10^{16}cm^{-2} (1 MeV n, 4cm)
- Multiplicity: 5-10 k tracks/event



New detector concepts needed

The ATLAS Pixel Detector

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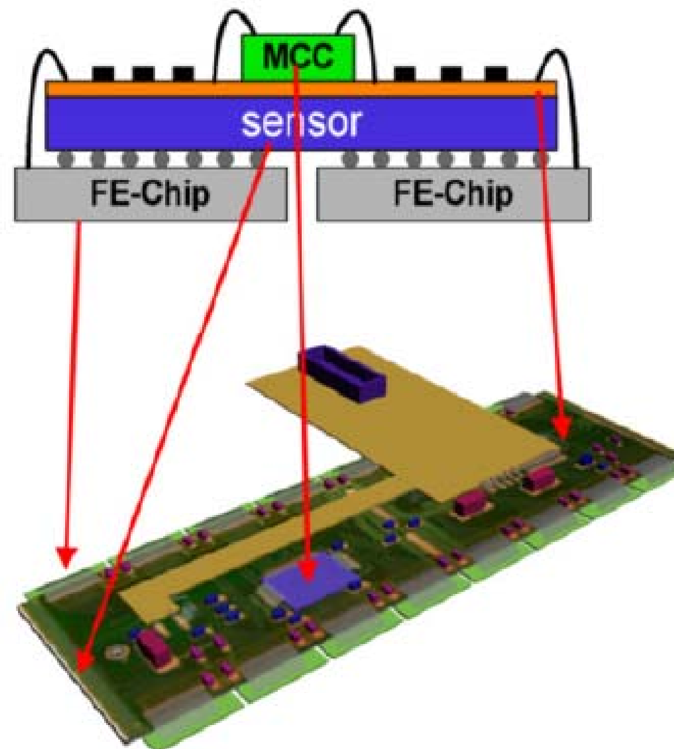
Present Layout:

-250 μm n-in-n pixel sensor
-50 x 400 μm^2 pixels
-0.25 μm rad hard ASIC
-raf hard till 10^{15} n/cm^2

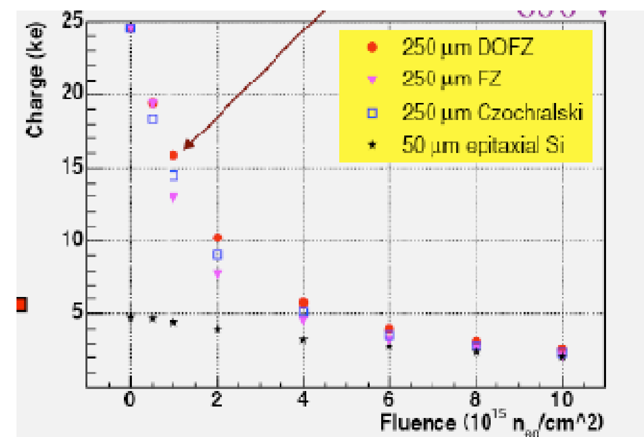
-Live fraction ~71%
-Cantilever for readout
-Sensor width 2x chip size: 16 mm
-Large material overhead



At SLHC:

-V_{dep} ~ 4200V
-Charge collection: ~15%
(at 10^{16} n/cm^2)
-High occupancy

Main cost driver: Bump bonding !



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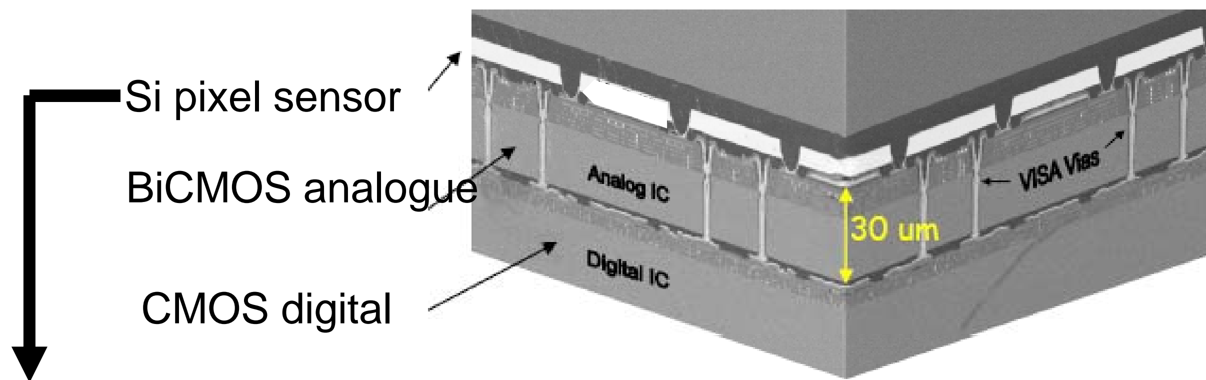
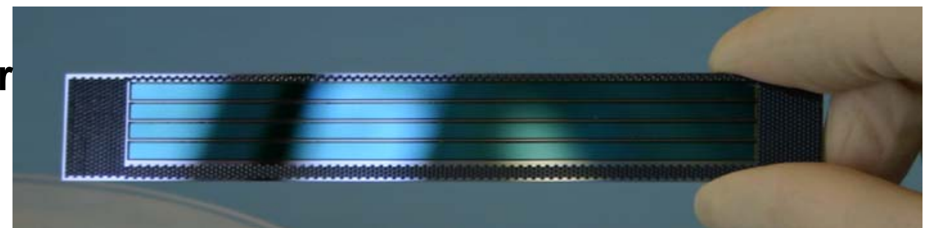
R&D for a novel pixel detector for SLHC

3D interconnection (sensor – electronics; electronics – electronics):

Alternative to bump bonding (fine pitch, potentially low cost?).
New possibilities for ASIC architecture (multilayer, size reduction).
Optimization of rad. hardness, speed, power.
Impact on module design (ultra thin ASICs, top contact, 4-side abuttable).



R&D on thin (O(50μm) FZ silicon detectors:
Based on well known pixel sensor technology.
Can be operated at 10^{16} n/cm^2 (V_{dep}, I_{leak}, CCE)?



Can lead to an advanced module design: rad hard with low material budget

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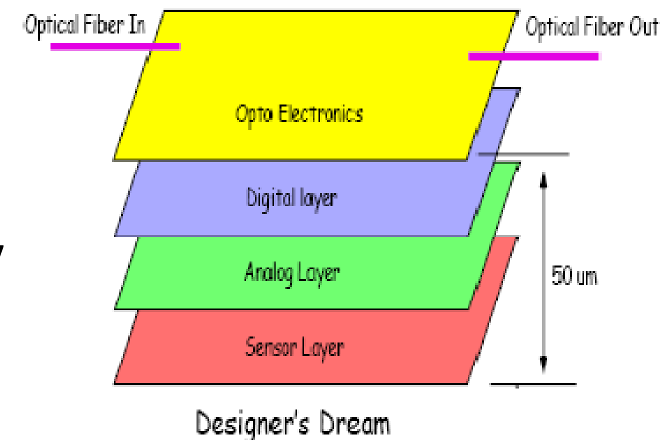
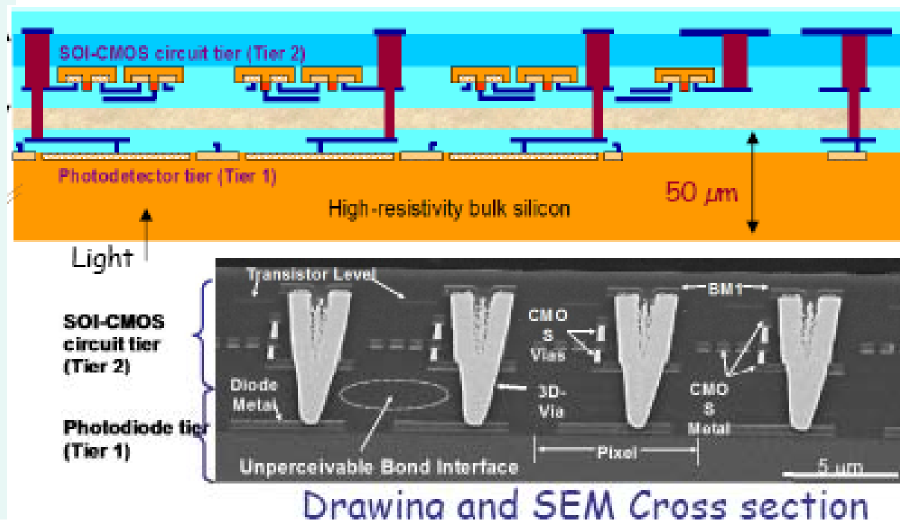
3D Interconnection

Two or more layers (="tiers") of thinned semiconductor devices interconnected to form a "monolithic" circuit.

- **Different layers can be made in different technology (BiCMOS, deep sub-µ CMOS, SiGe,…..).**
- **3D is driven by industry:**
  - **Reduces R,L and C.**
  - **Improves speed.**
  - **Reduces interconnect power, x-talk.**
  - **Reduces chip size.**
  - **Each layer can be optimized individually**





Drawing and SEM Cross section

For HEP: sensor layer: fully depleted Si
Example: 2-Tier CMOS Sensor, 1024 x 1024 pixel, pitch 8 µm by MIT-Lincoln Lab

IZM SLID Process

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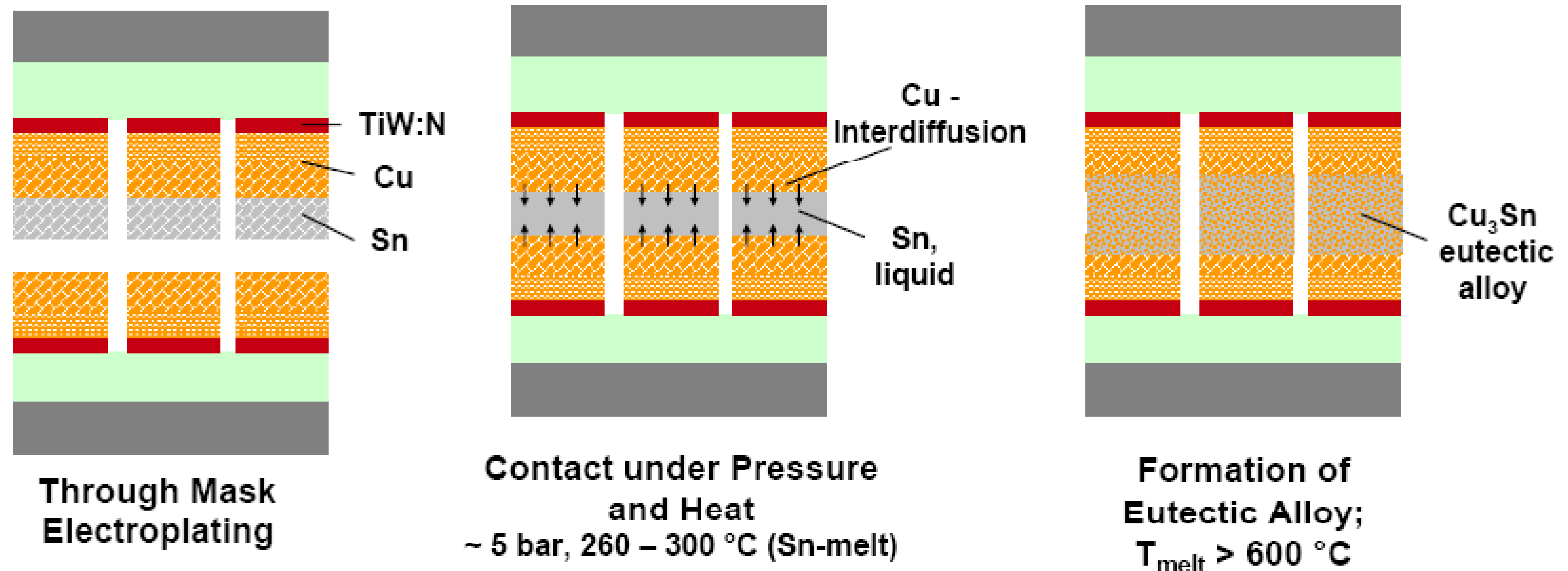
Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps "low cost" (IZM)).
- Small pitch possible (<< 20 µm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

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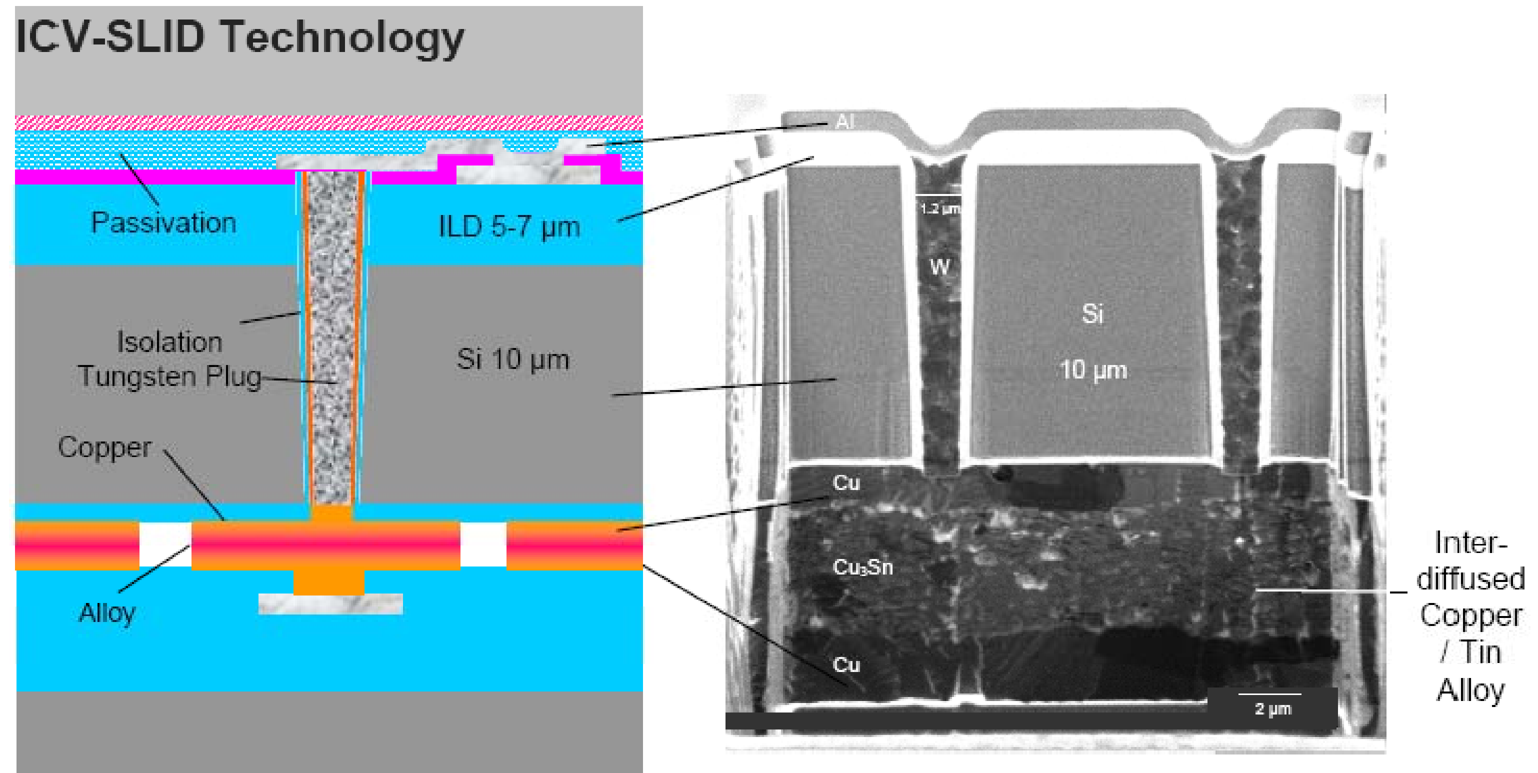
Through Silicon Vias



ICV = Inter Chip Vias

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- **Hole etching and chip thinning**
- **Via formation with W-plugs.**
- **Face to face or die up connections.**
- **2.5 Ohm/per via (including SLID).**
- **No significant impact on chip performance (MOS transistors).**

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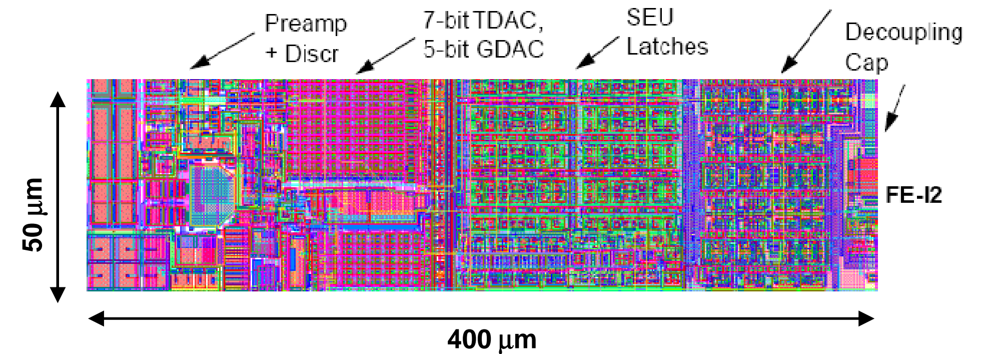
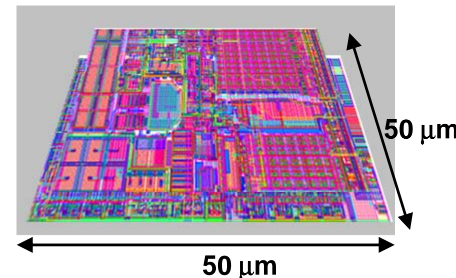
Advantages of 3D

Multilayer electronics:

Split analogue and digital part
Use different, individually optimized technologies:

-> gain in performance, power, speed, rad-hardness, complexity.
-> smaller area (reduce pixel size or more functionality).



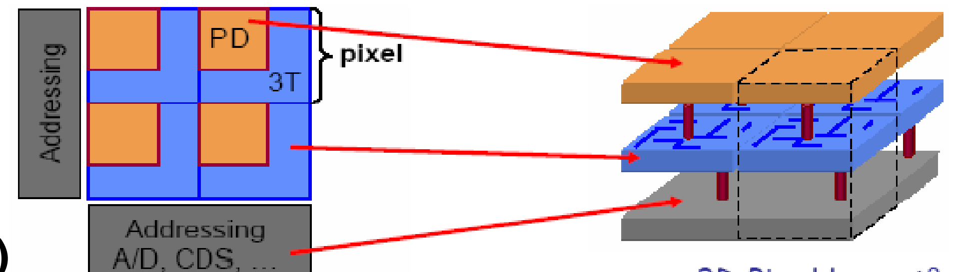


$50 \times 400\ \mu m^2$ (0.25 µm)
May shrink to ~ $50 \times 50\ \mu m^2$ (130 nm)

4-side abuttable devices:

-> no dead space.
-> simpler module layout.
-> larger modules.

(reduce complexity and material)



Conventional CMOS sensor (optical, similar: MAPS)

3D Pixel Layout[9]

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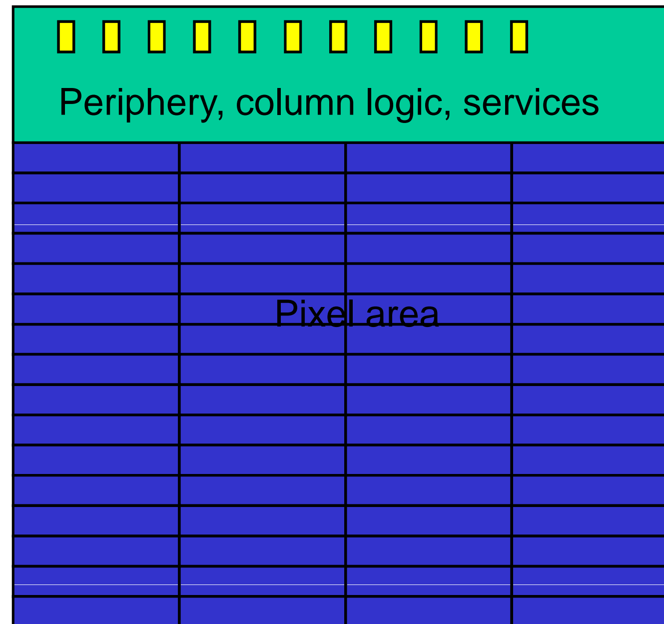
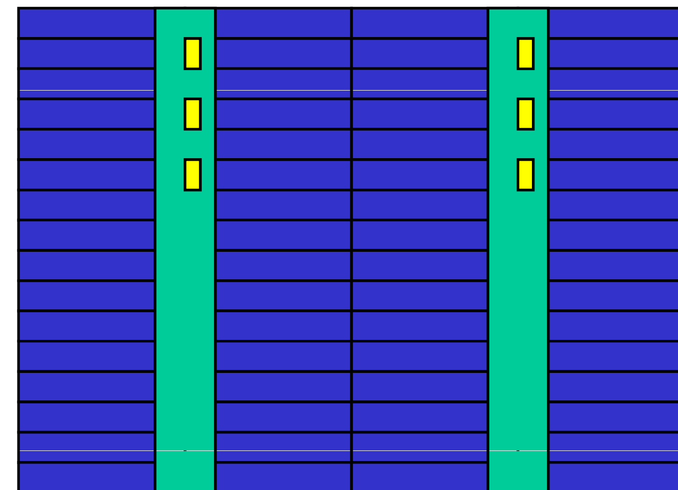
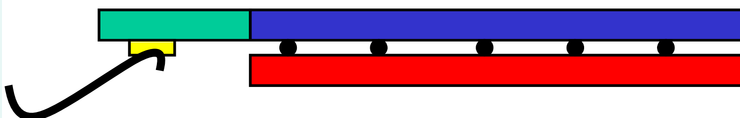
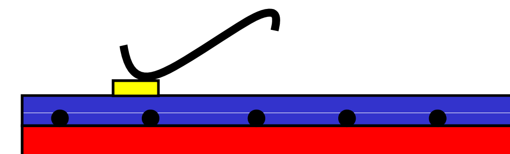
Advantages even for single layer

Conventional Layout | **3D Layout**









Make use of smaller feature size (gain space)
-> move periphery in between pixels (can keep double column logic)
-> backside contacts with vias possible
-> no cantilever needed, 4-side abuttable

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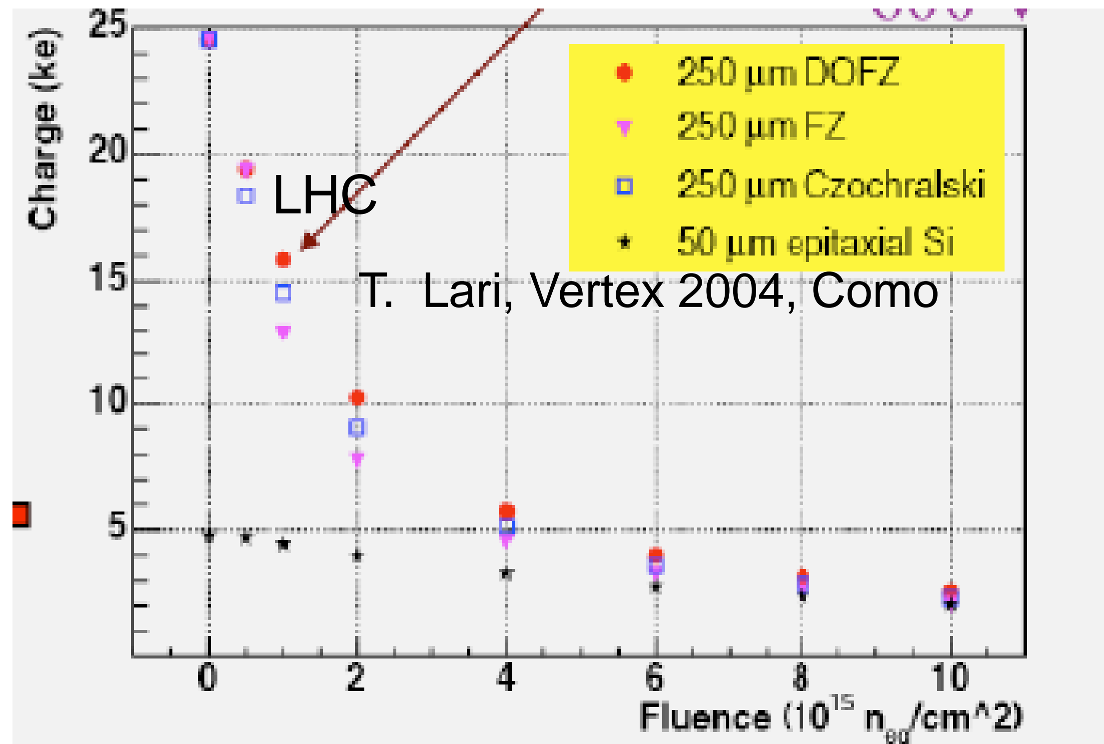
Motivation for Thin Detectors

After 10^{16} n/cm^2:

V_{dep} > 4000V (250 μm) -> operate partially depleted.
Large leakage currents.
Charge loss due to trapping (mean free path ~ 25 μm).
I_e > I_h (need n-in-n or n-in-p) to collect electrons.



No advantage of thick detectors ->thin detectors: low V_{dep}, I_{leak} (and X_0)
However: small signal size is a challenge for the readout electronics

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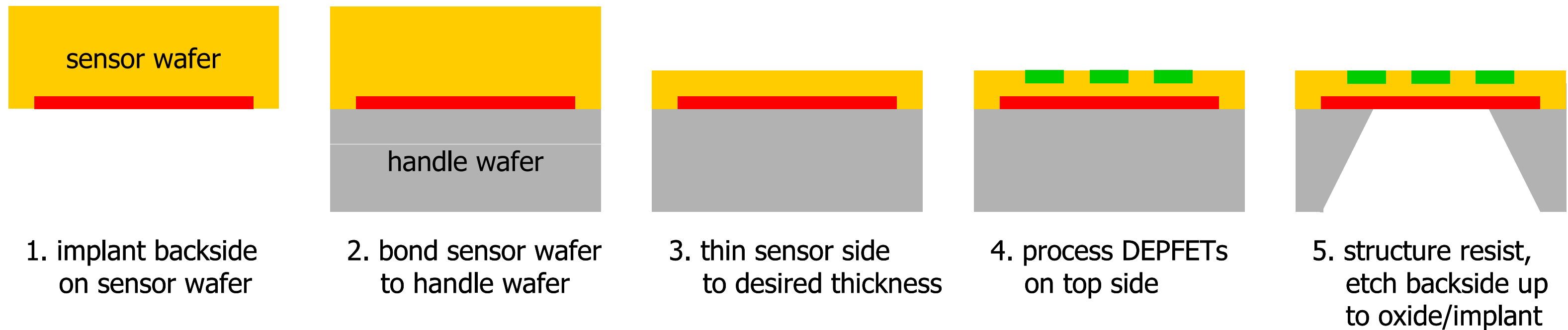
Thinning Technology

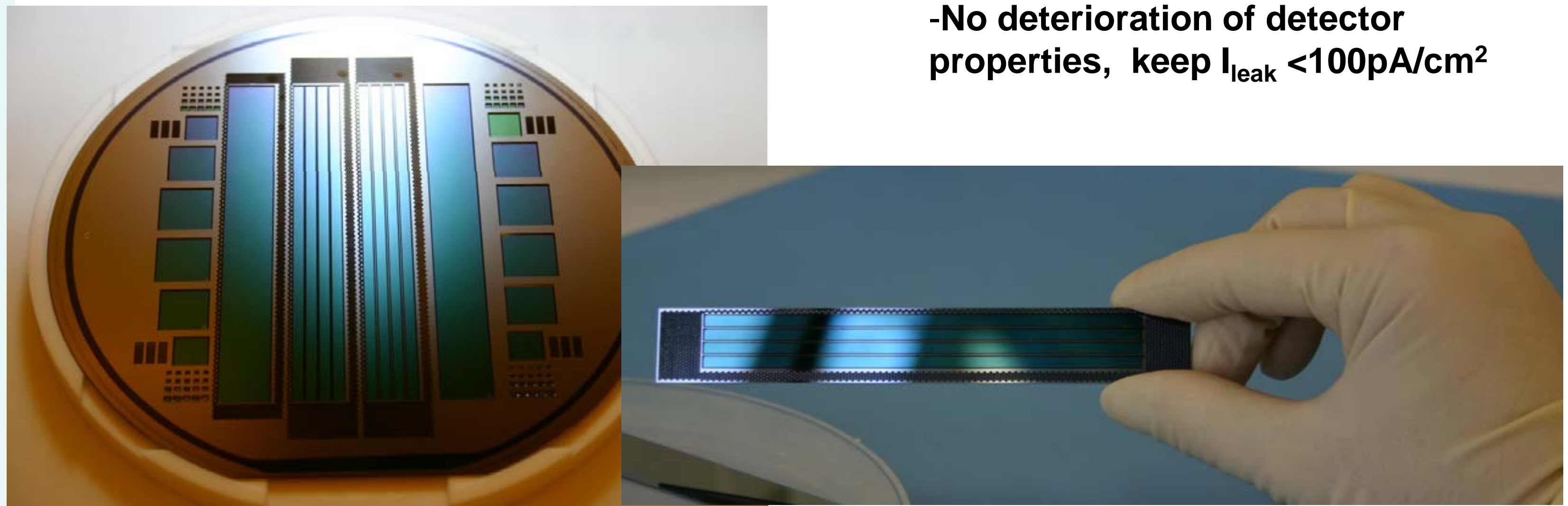


- **Sensor wafer: high resistivity d=150mm FZ wafer.**
- **Bonded on low resistivity "handle" wafer".**
- **(almost) any thickness possible**

Thin (50 µm) silicon successfully produced at MPI.

- MOS structures
- diodes

-No deterioration of detector properties, keep I_{leak} <100pA/cm^2



Measurements (V_{dep}, CCE)

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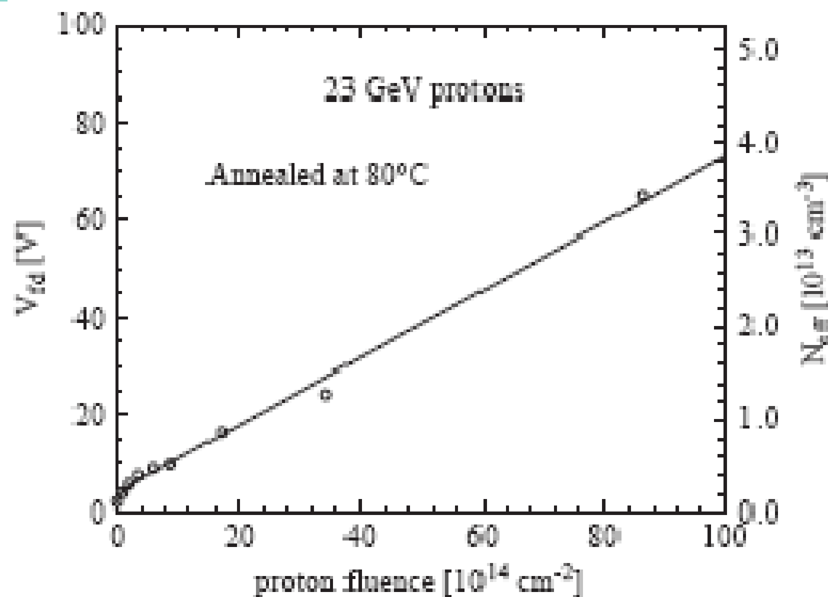

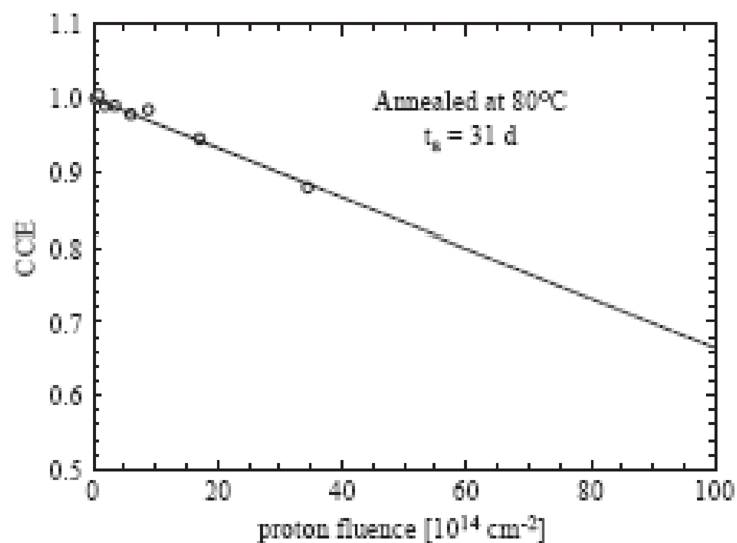

Fretwurst et al. NIM A 552 (2005): After short term annealing:

V_{dep} < 100V at 10^{16} 1/cm².

However, detectors need to be kept cold (reverse annealing!).

Leakage currents:
α(80°C, 8min) = 2.4 x 10^{-17} A/cm.

CCE ~ 66% @ 10^{16} p/cm² (extrapolated).

Similar to results from epi-material (G.Kramberger):

3200e (62% average), 2400e (60% most prob).

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Pre tests and Plans

Diode test wafers processed at HLL
-Preparation for SLID process IZM
-Diffusion barriers & Cu layers

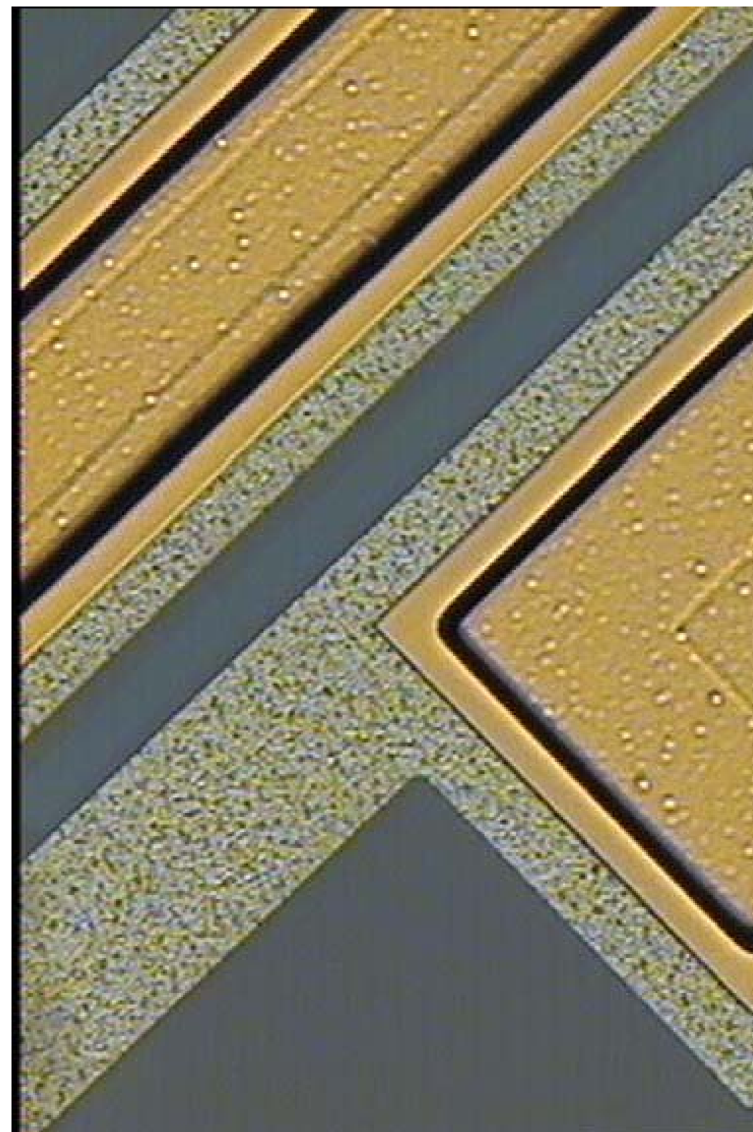
ok

RD50

Production of thin pixel detectors ATLAS footprint, single chip size: start, summer 2007
-includes test structures for irradiations (diodes, strips, small pixel arrays)

Connection of wafer & ATLAS pixel chip using SLID: 2008

Full demonstrator (thinning, SLID, ICV): 2009



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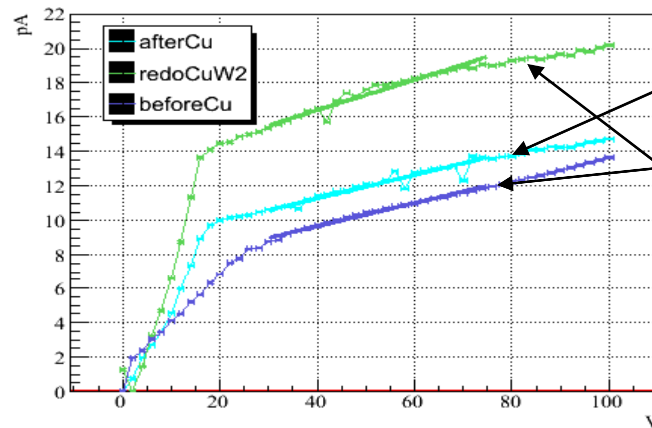
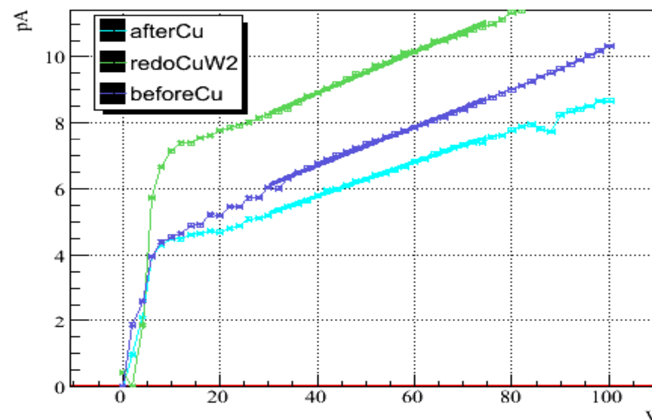
Pre tests on 50µm thin $10mm^2$ diodes

before and after Cu/Sn deposition and after rework





- thinned p on n diodes
  … Al + Passivation (HLL)
  IZM:
  Ti/W + Cu
  Removing of Ti/W + Cu
  Redeposition of Ti/W + Cu/Sn

wafer bonding works also with 150mm wafer

no Cu penetration into the sensor
Ti/W barrier system holds

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Modular approach

3D integration with SLID can be combined with any sensor concept

- N on P
- N on P (epi) Fz or MCz
- 3D sensor

Prototyping at HLL:
N on N technology, moderated pspray, no polyresistors
if 6“ p-doped material is available, some wafers P on N

3 thicknesses: 50µm, 100µm, 150µm

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Test program

Charge collection and sharing
vs readout node geometry, bias voltage, irradiation

4 readout chips

- ATLAS-pixel chip: 400x50µm², binary (ToT), SLID, rad hard, available

  Test structures: pixel (ATLAS geometry)

- SCT128, pitch adaptor, analogue, wire bonded after irradiation, available (Ljubljana)

  Test structures: mainly short strips (different geometries)

- Interon-Chip (Einar Nygard, Oslo), 10x10pixel, 200x50µm², analogue, SLID, rad hard, to be designed
- Medipix: 55x55µm², analogue, SLID, not rad hard, slow

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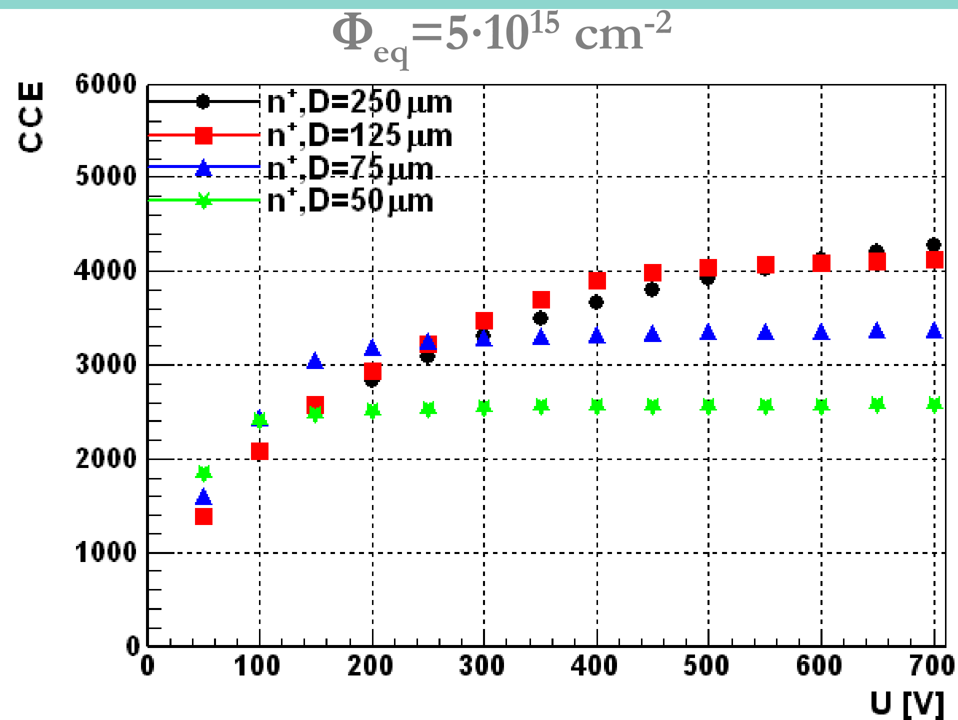
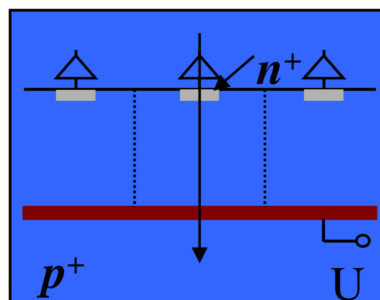
QV plots (Simulations) – different detector thicknesses G. Kramberger (Schloss Ringberg 2007)





- Similar Q-V characteristics up to full depletion!
- Thinner sensors are beneficial at lower voltages – the more voltage you can apply the more beneficial are thicker detectors

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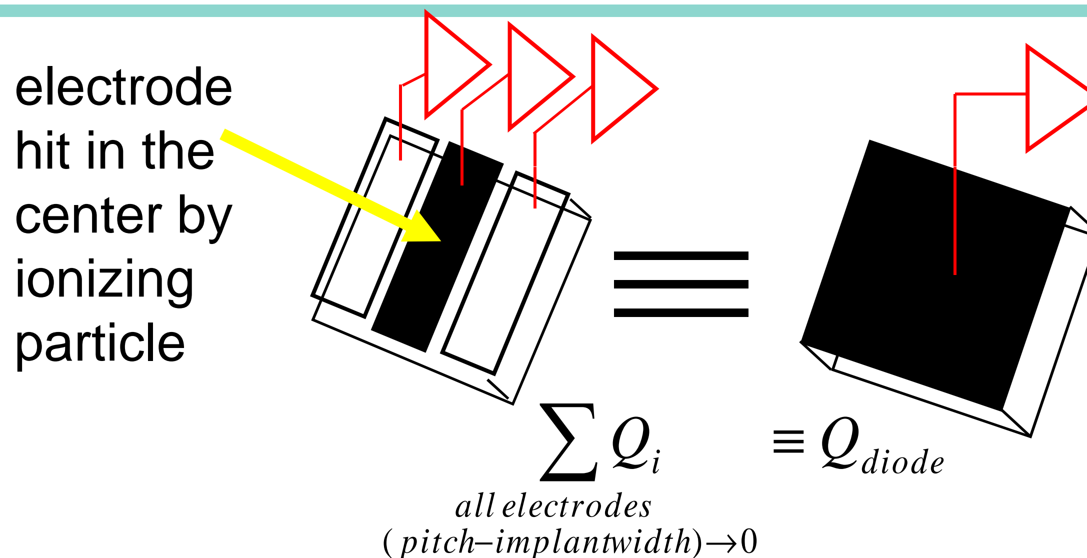
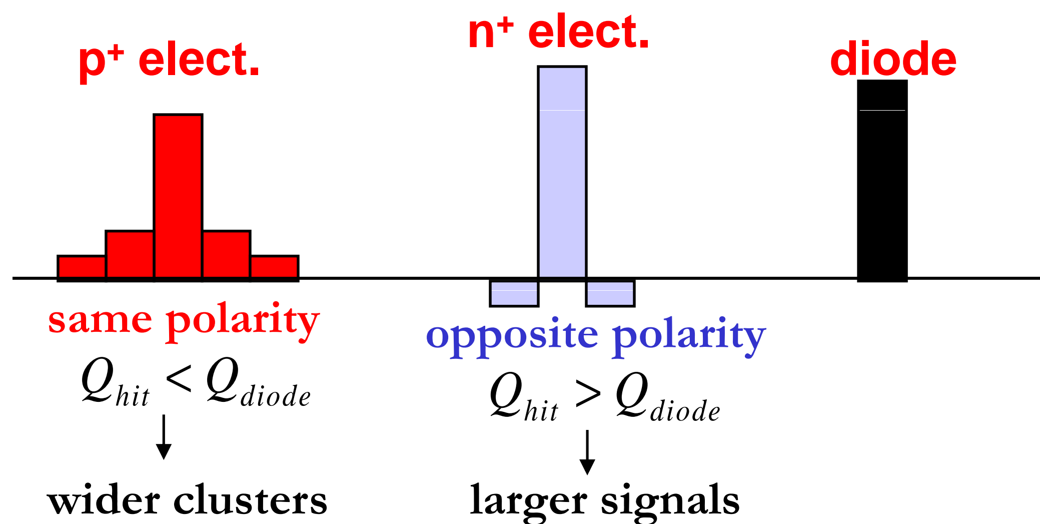
Trapping induced charge sharing (G. Kramberger)

electrode hit in the center by ionizing particle



$$\sum_{\substack{all\,electrodes \\ (pitch-implantwidth)\to 0}} Q_i \equiv Q_{diode}$$



same polarity

$Q_{hit} < Q_{diode}$

↓

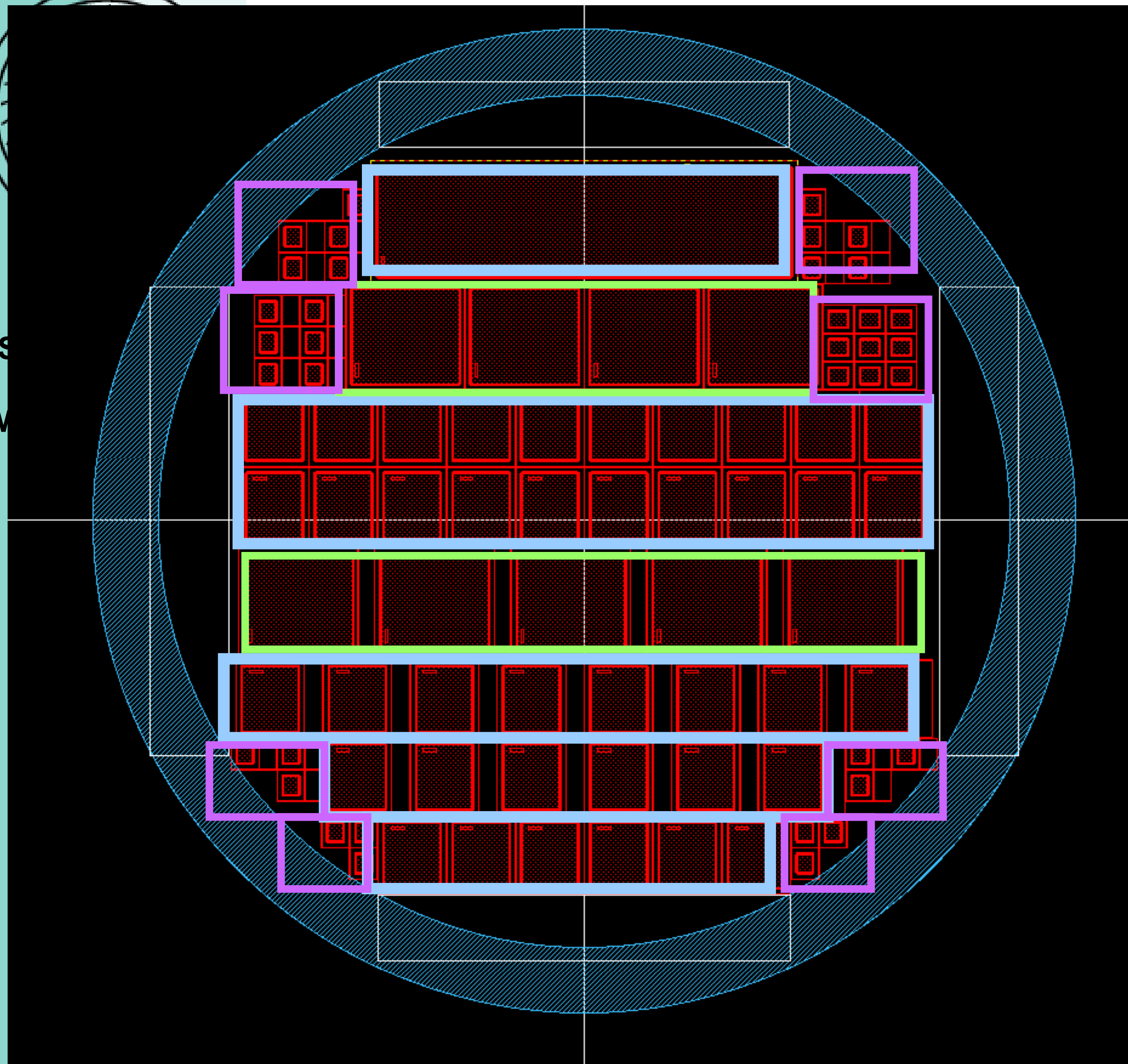
wider clusters

opposite polarity

$Q_{hit} > Q_{diode}$

↓

larger signals



pixels to be read-out by the FE ATLAS Chip and test diodes

pixels to be read-out by the MEDIPIX2 Chip and short strips

pixels to be read-out by the Interon Chip

For each type of read-out chip two different geometries of the pixels cells are foreseen to allow for:

a) standard wire bonding on the pads for the services of the chip

b) access to the pad through a via etched from the backside

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Schedule

- Begin of pre processing July 07 (definition of chips active areas for backside implantation)
- Waferbonding: July-August
- Final design: Aug. 07
- Production start: Sept. 07
- First samples: begin of 2008

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Summary

Thin detectors

- **Keep V_{dep} low.**
- **Keep I_{leak} low (power).**
- **Reduce X_0 (if this is not an issue: backside etching not necessary, simpler fabrication)**

- **Results on radiation hardness and CCE encouraging.**
- **Large scale industrial production possible.**
- **Thickness can be adapted to radius (fluence) -> parameter!**

R&D topics:

- **Make real pixel detectors.**
- **Irradiations, measurement of CCE.**
- **Optimize thickness**
- **Charge sharing.**
- **Optimize production process**

New collaborators are welcome !

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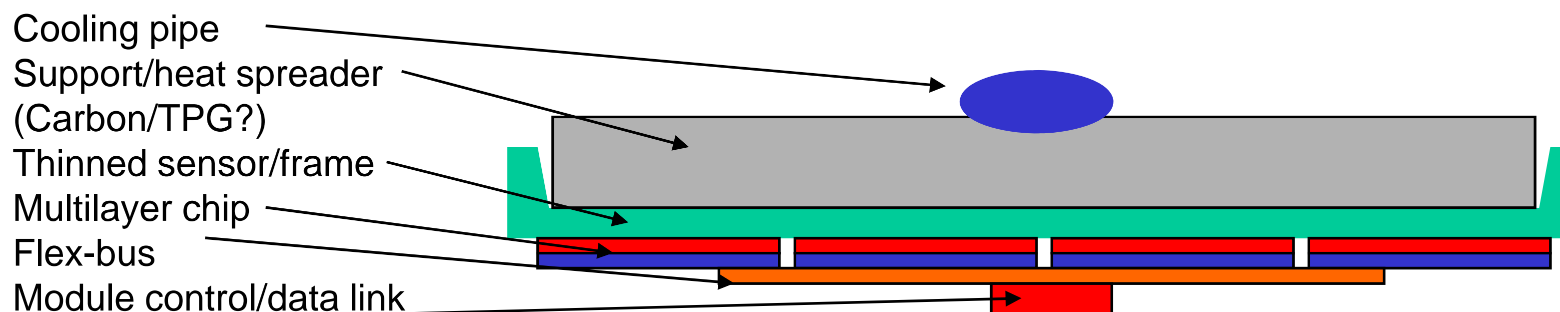
Conceptual Module Design



"Designer's dream"

- **Two layer chip ("analogue" and "digital" layer)**
- **Connected to thin detector using SLID**
  - **small pixel size**
  - **small pitch**

- **Low material budget:**
  - **4-side abuttable ASICs**
  - **large live fraction (-> 100%)**
  - **larger modules**
  - **less services and material overhead**

further advantages if used with edgeless sensors

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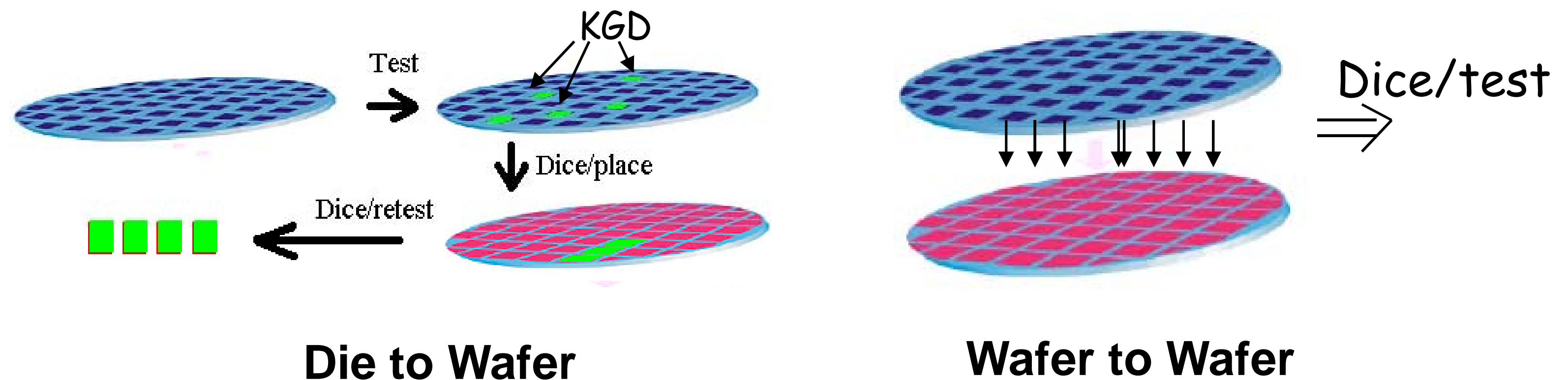
Two Different 3D Approaches

Wafer to Wafer bonding

- Must have same size wafers
- Less material handling but lower overall yield

Die to Wafer bonding

- Permits use of different size wafers
- Lends itself to using KGD (Known Good Die) for higher yields



Die to Wafer **Wafer to Wafer**

Fraunhofer IZM offers Die to Wafer processing -> optimal for prototyping

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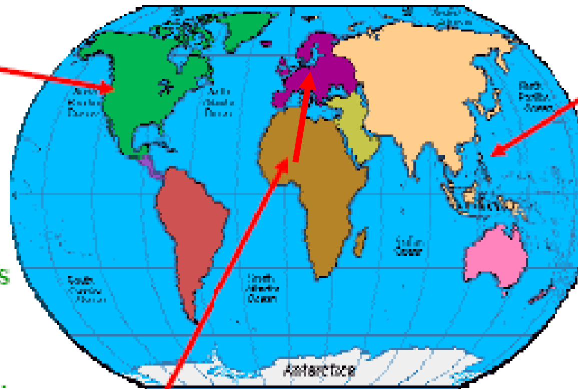
World Wide Interest in 3D

USA:
Albany Nanocenter
U. Of Kansas,
U of Arkansas
Lincoln Labs, AT&T
MIT,RPI, RTI, TI
IBM, Intel, Irvine Sensors
Micron, Sandia Labs
Tessera, Tezzaron,
Vertical Circuits, Ziptronix



Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

Europe: Fraunhofer IZM, IMEC Delft,
Infineon, Phillips, Thales, Alcatel Espace,
NMRC, CEA-LETI, EPFL, TU Berlin

R. Yarema (Fermilab)

3D is discussed in the ITRS (International Technology Roadmap for Semiconductors) as an approach to improve circuit performance and permit continuation of Moore's Law.

R&D driven by industry.
Different approaches (solder, SOI, epoxy).

MPI will work with Fraunhofer IZM, Munich.

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IBM Press Release

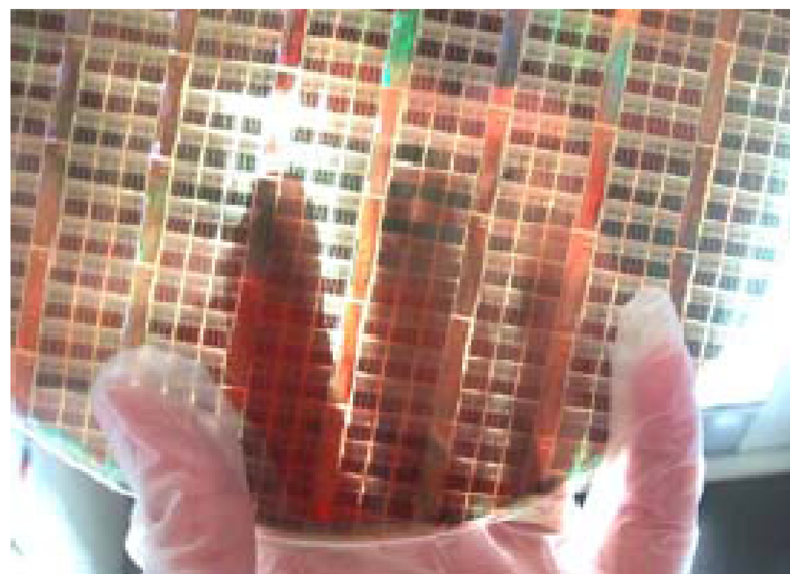
the third-dimension

Breakthrough demonstrates viability of 3-D chip stacking technique for manufacturing

ARMONK, N.Y., April 12, 2007 -- IBM today announced a breakthrough chip-stacking technology in a manufacturing environment that paves the way for three-dimensional chips that will extend Moore's Law beyond its expected limits. The technology – called "through-silicon vias" -- allows different chip components to be packaged much closer together for faster, smaller, and lower-power systems.

The IBM breakthrough enables the move from horizontal 2-D chip layouts to 3-D chip stacking, which takes chips and memory devices that traditionally sit side by side on a silicon wafer and stacks them together on top of one another. The result is a compact sandwich of components that dramatically reduces the size of the overall chip package and boosts the speed at which data flows among the functions on the chip.

"This breakthrough is a result of more than a decade of pioneering research at IBM," said Lisa Su, vice president, Semiconductor Research and Development Center, IBM. "This allows us to move



[High-res image]

IBM extends Moore's Law to the third-dimension: An IBM scientist holds a thinned wafer of silicon computer circuits, which is ready for bonding to another circuit wafer, where IBM's

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Two Different 3D Approaches

Wafer to Wafer bonding

- Must have same size wafers
- Less material handling but lower overall yield

Die to Wafer bonding

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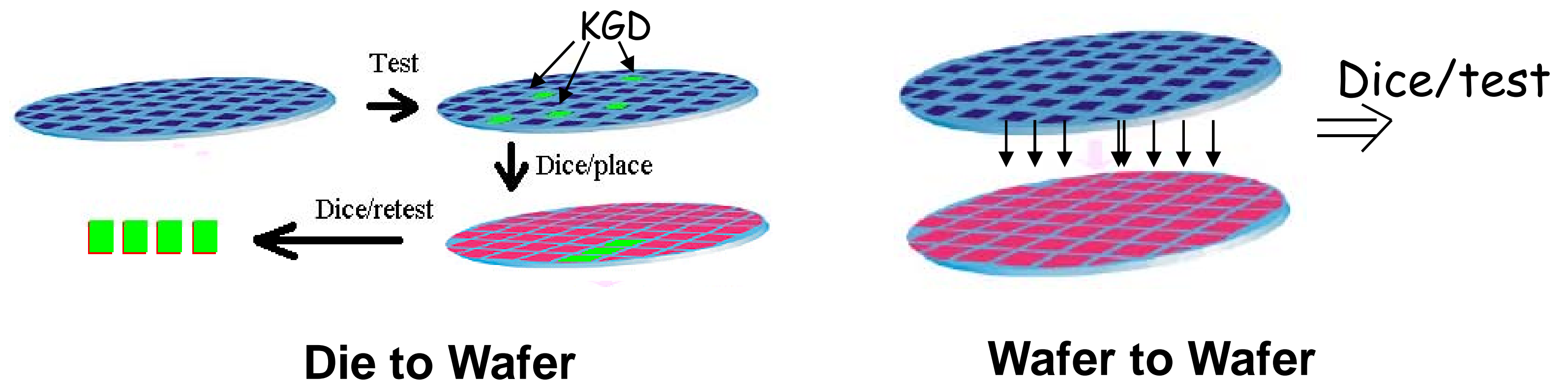

Die to Wafer **Wafer to Wafer**

IZM offers Die to Wafer processing -> optimal for prototyping

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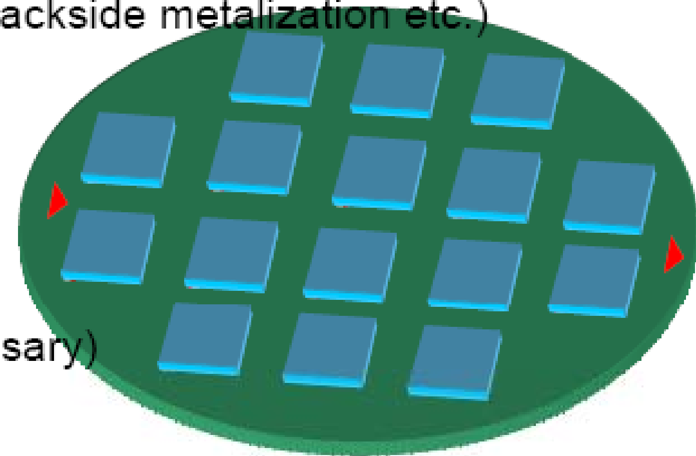
IZM chip to wafer concept

3D System Integration

Handling Concept for Wafer-Level Chip-Scale Processing (1)

- Placement of Chips on Handling Substrate
  - Grid of Aligment Marks according to the Positions on the Target Wafer
- Processing of Chips on Wafer Scale
  (e.g. cleaning prior to bond, thinning, backside metalization etc.)
- Transfer to Target Wafer
  - Adjusted Stack Formation (Wafer-Flip)
  - Removal of Handling Substrate
- Further Processing of new Stack (if necessary)



Dr. A. Klumpp

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

FEE 2006, Perugia, Italy

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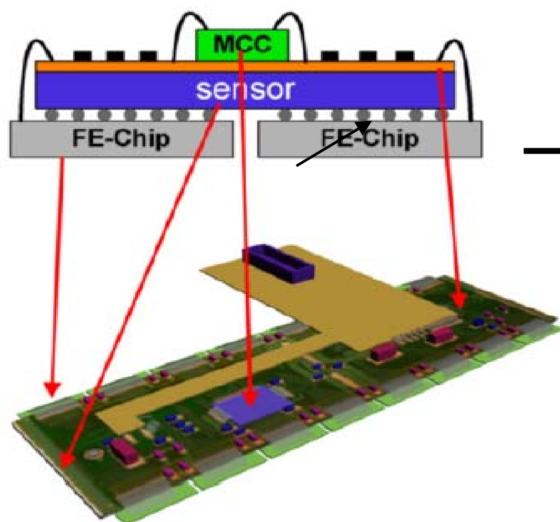
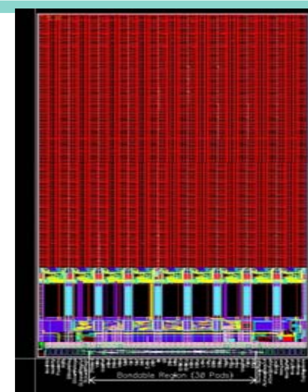
Semiconductor Laboratory
MPI for Physics, Munich

10th RD50 Workshop
Vilnius
4-6th June 07

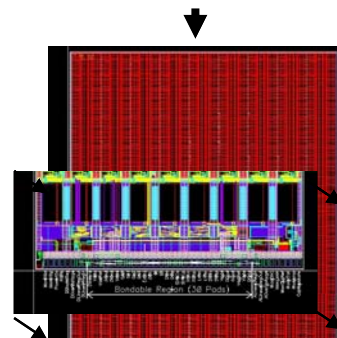
Advantages for Module Design

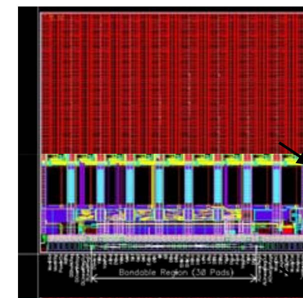




Pixel area
(facing sensor)

Periphery
Pipeline and control
Bond pads
(cantilever)

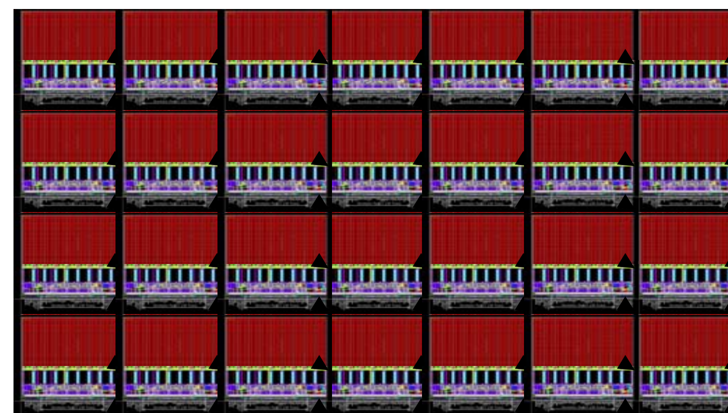




Control on top of pixel area.
External contact from top.
Contact pixels through vias:
-> 4-side buttable.
-> No "cantilever" needed.

Larger module with minimal dead space.

Less support structures & services.
Substantial material savings.



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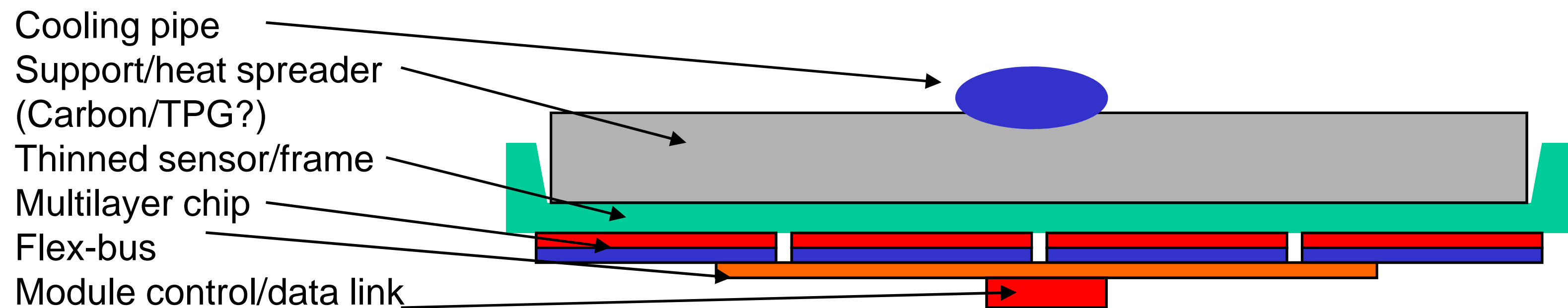
Conceptual Module Design



"Designer's dream"

- **Two layer chip ("analogue" and "digital" layer)**
- **Connected to thin detector using SLID**
  - **small pixel size**
  - **small pitch**

- **Low material budget:**
  - **4-side abuttable ASICs**
  - **large live fraction (-> 100%)**
  - **larger modules**
  - **less services and material overhead**

further advantages if used with edgeless sensors

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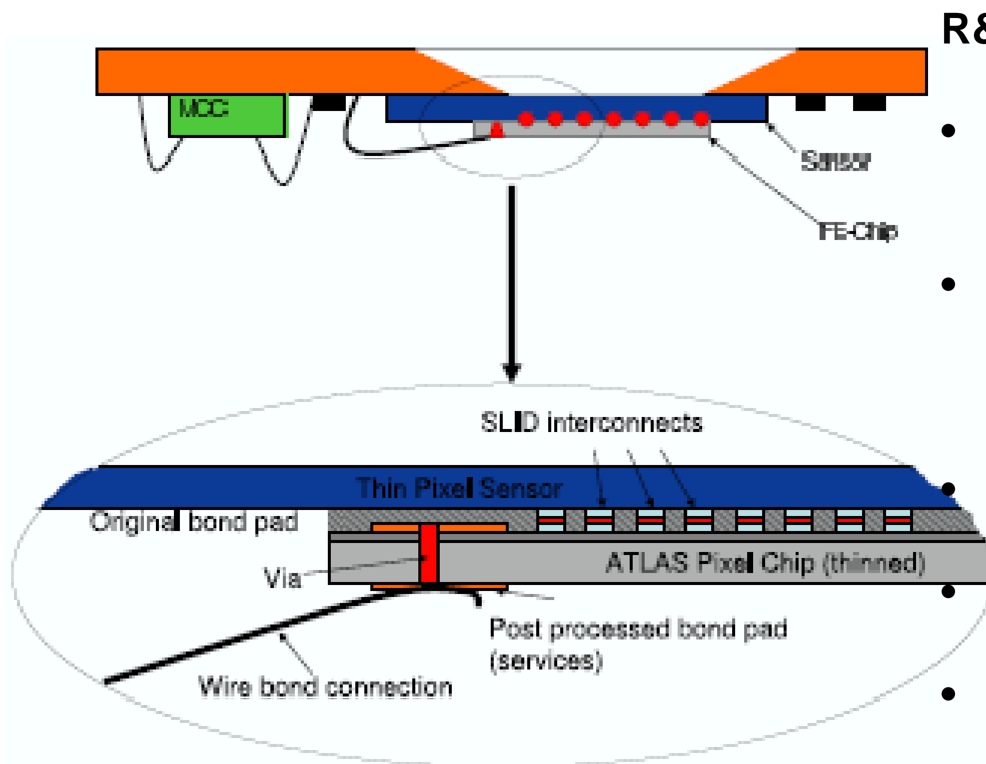
Proposed R&D Program

a) Test interconnection process with diode test structures

b) Build demonstrator using ATLAS pixel chip and pixel sensors made by MPI



R&D Issues:

- Technology: compatible with sensors, ASICs?
- Interconnection quality: e.g. capacitance (face-to-face or die up?).
- Yield & Costs.
- Production in industry.
- Reduce material (copper layer).

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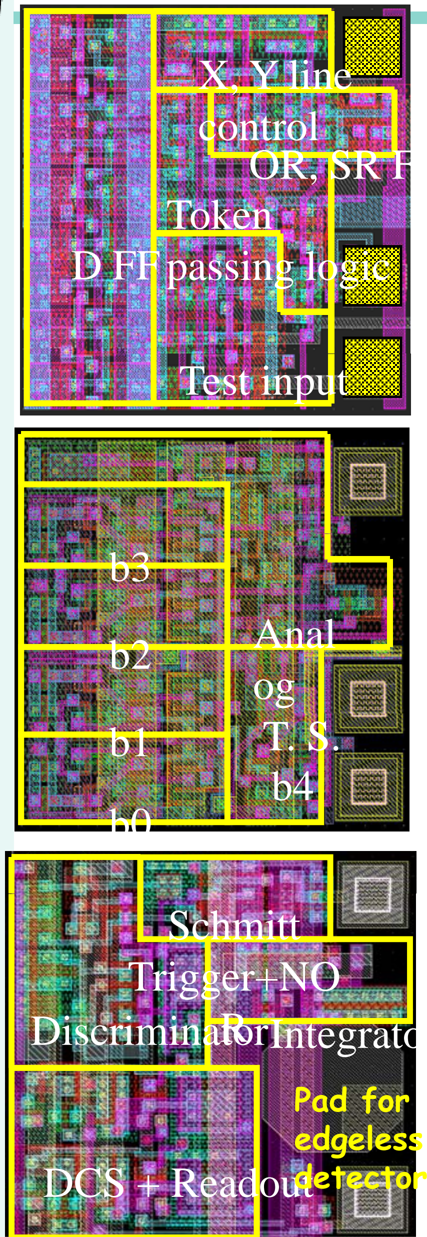
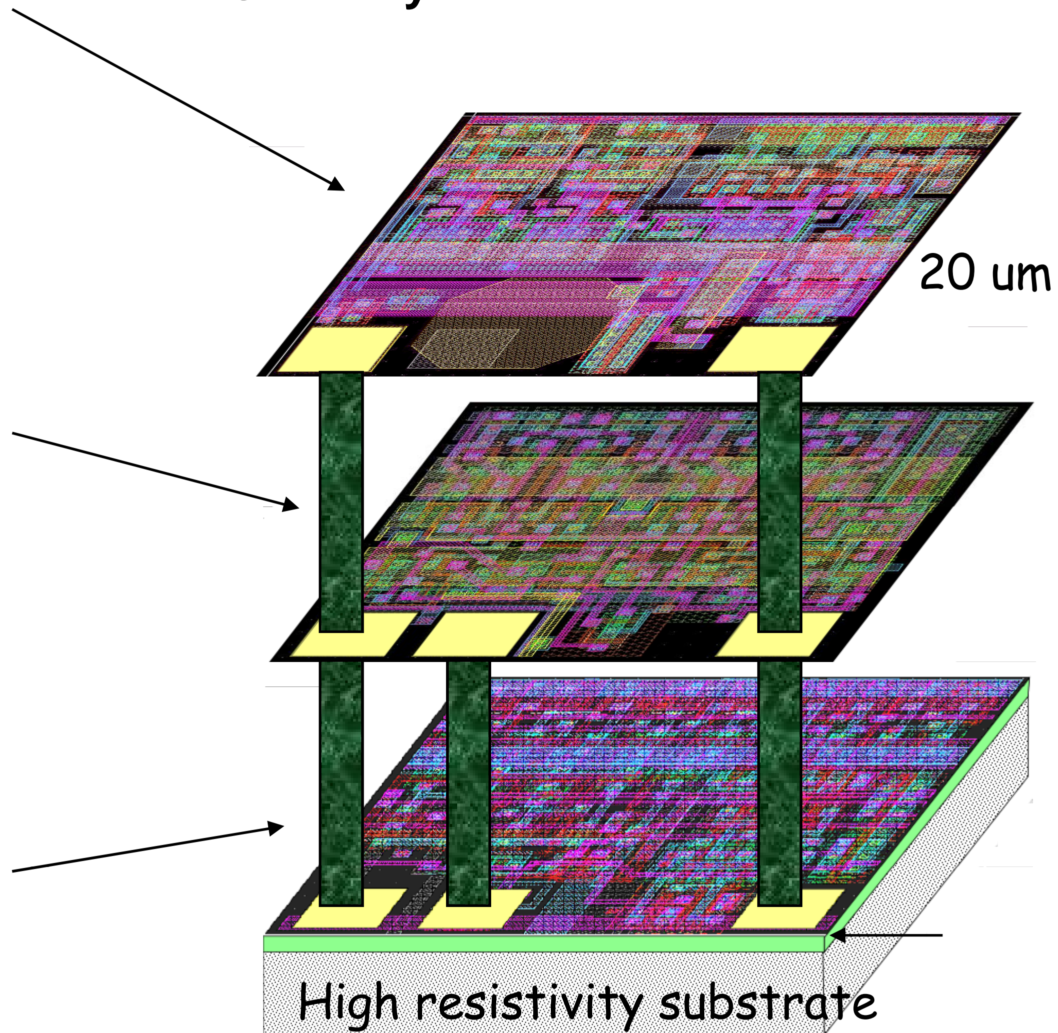
R&D at Fermilab



3 Tier readout chip for ILC – R. Yarema
Submitted at MIT Lincoln Lab
No Sensor yet!



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Summary

3D interconnection offers a solution for highly integrated, complex, high performance pixel detectors

-Could be used with many sensor types (planar, 3D, DEPFET,………)

-Can combine different ASIC technologies

-Backside-connection of 4-side abuttable chips

-Thinning of ASICs is basic ingredient -> low mass!

-R&D driven by industry -> potentially cost effective solutions

-Several HEP groups started to look into 3D (Fermilab, MPI)

-MPI started a R&D program for the ATLAS sLHC upgrade:

- 3D interconnection using IZM SLID and ICV processes
- Thin FZ sensors ("standard" pixel sensors optimized for SLHC).
- 3D Interconnection is an option for other sensor types (e.g. 3D detectors).
- Inviting collaborators (especially ASIC experts)

ATLAS sLHC Upgrade R&D

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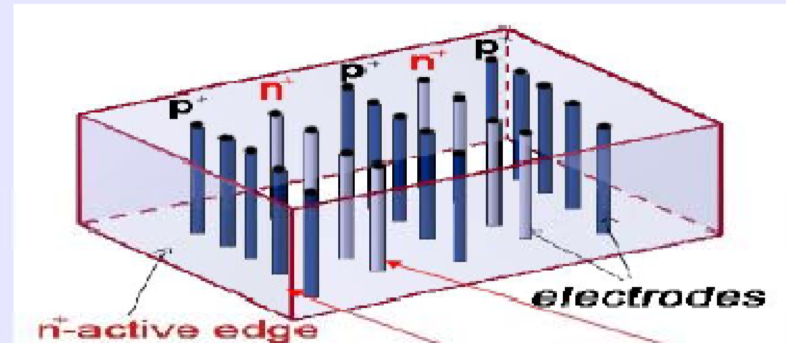
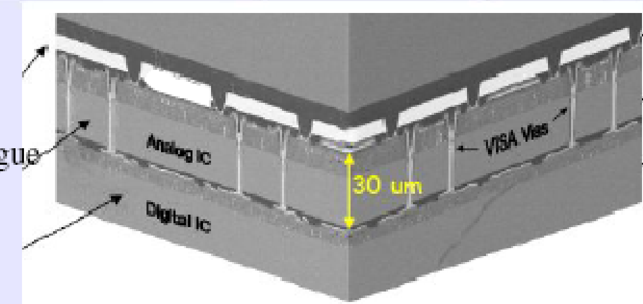
B-layer: Highest radiation damage, look for new technology

- 3D-Silicon (Sherwood Parker, Cinzia Davia, et al):
  - Test-beam results available; R&D proposal under review (currently being improved)

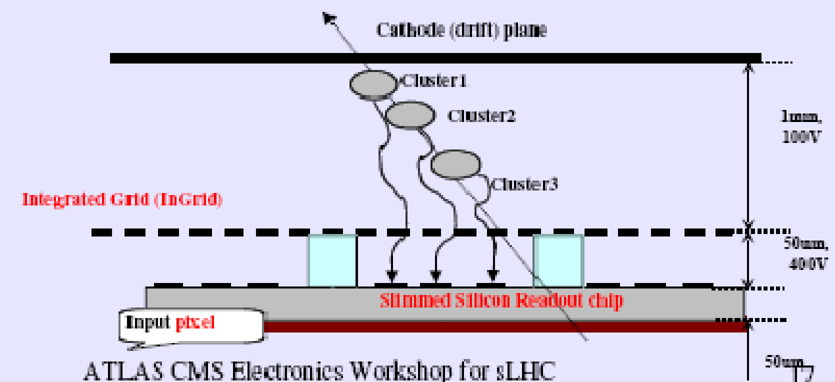


- Thin-silicon combined with 3D-interconnect technologies (Richard Nisius/MPI-Munich et al):
  - Vias through si layers + replace bump bonding with solid-liquid diffusion
  - Low bias V; low C + low signal --> still good S/N

Si pixel sensor
BiCMOS analogue
CMOS digital



- Gossip (Harry van de Graaf/NIKHEF et al)
  - Gas detector on slimmed silicon pixel chip
- PO will set up a group to exploit common items, keep together, look at risk etc.



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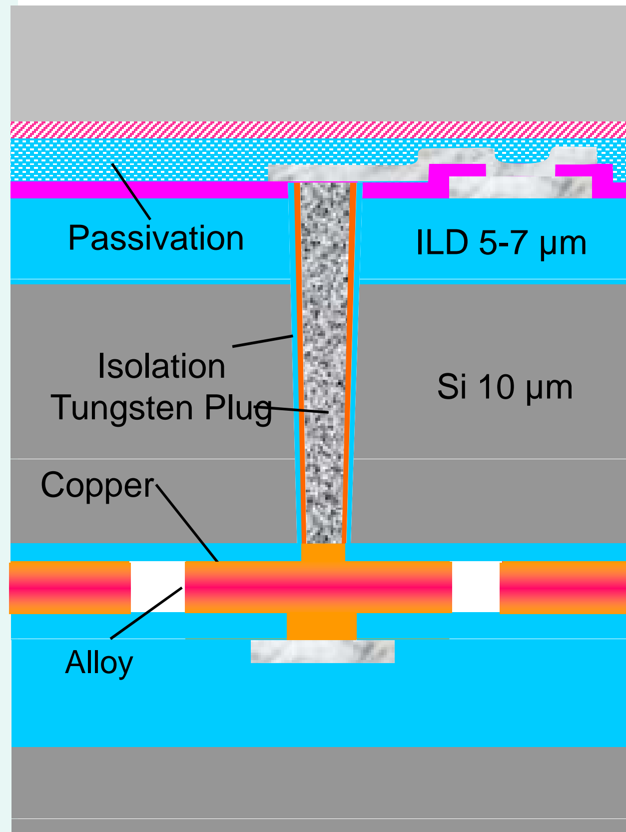
Radiation Length - SLID-ICV



X_0 of

Si: 9.36cm,
W: 0.35cm,
Cu: 1.43 cm,
Sn: 1.21 cm

assuming: -: pixel 50x50 µm², 3 tiers r/o

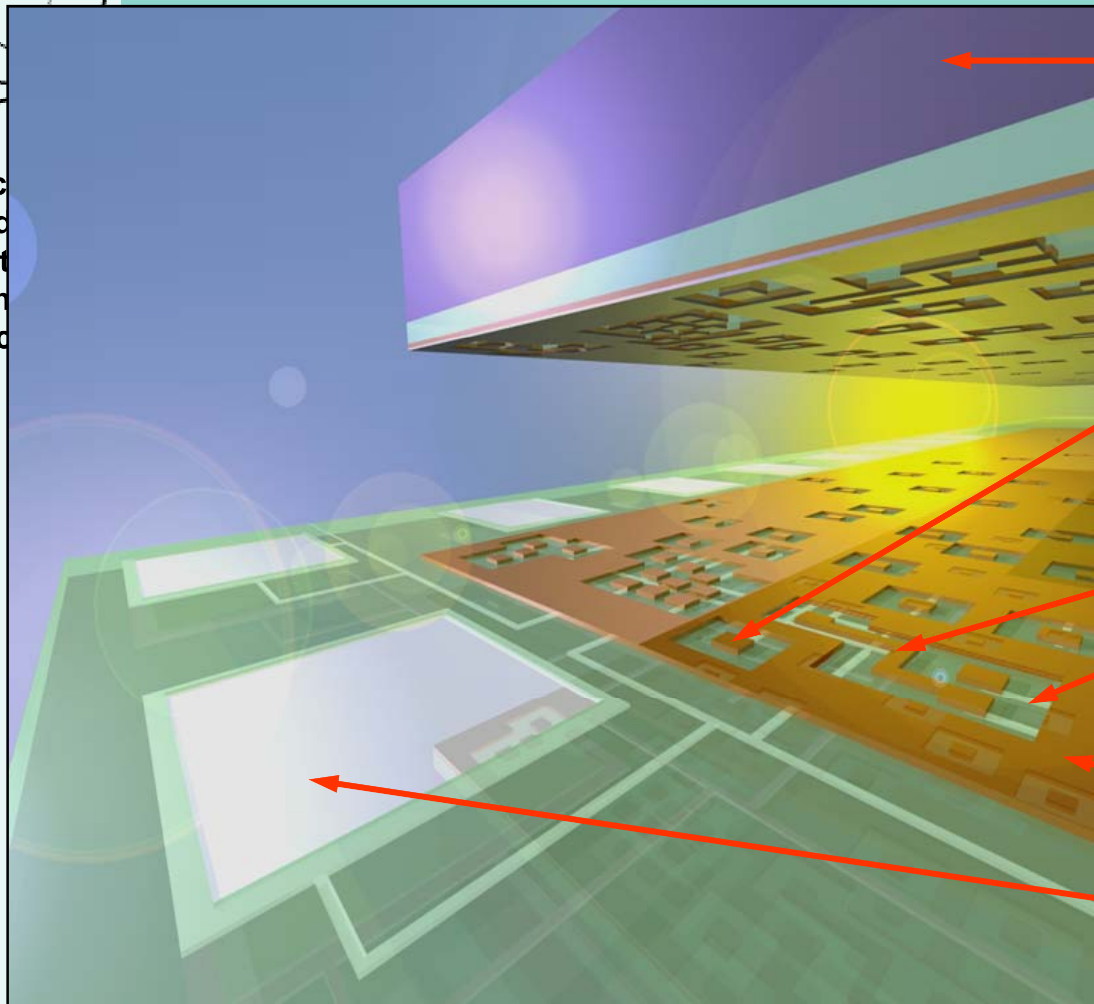
then material per pixel:

sensor	-:	50…100 µm Si
Si r/o	-: 3x20 µm	60 µm Si
3x ICVs, W	-: 20 µm deep, Φ 4 µm →	8 µm Si
3x contact Cu:	A=100 µm², t=6 µm, →	5 µm Si
3x contact Sn:	A=100 µm², t=2 µm, →	2 µm Si

material per pixel → 125…175 µm Si
0.12-0.16% X_0

Face-to-Face SOLID Process (IFX)

R.H. Ric
Semicond
Laborat
MPI for Ph
Munic



Top chip
Cu and Sn coating

Bottom chip
Cu coating, bond pads

No underfill

Inter chip vias
15 x 15 µm²
5 µm vias to LM

Redistribution

Insulation trenches
15 µm

Passive area
heat spreader

External IOs
standard wire bonds

Status of the project: Process defined, tooling exists (Datacon, EVG), ready for prodution
unfortunately, Mr. Huebner is now with Qimonda and they don't make chipcards...

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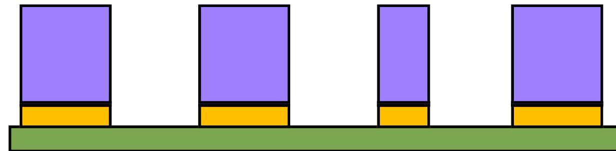
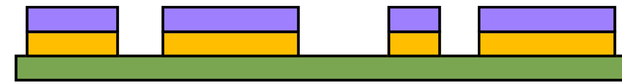
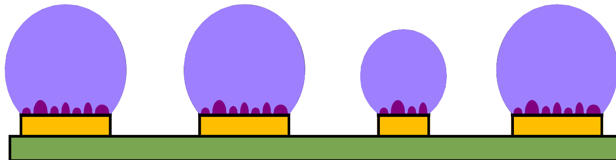
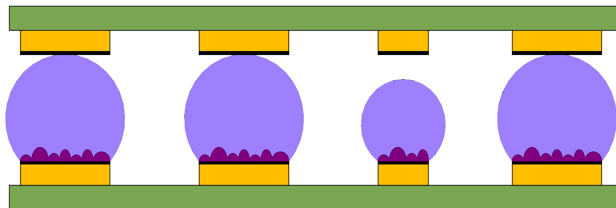
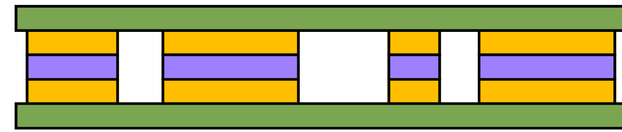
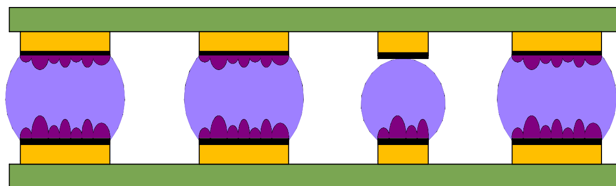
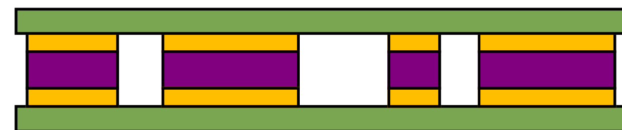
Munich

Comparison of Solder Processes

	FBGA	SOLID
1st step	 Metallization and solder apply	 Metallization and solder apply
2nd step	 Reflow	
3rd step	 Pick & place (flux)	 Pick & place (no flux)
4th step	 Soldering	 Soldering

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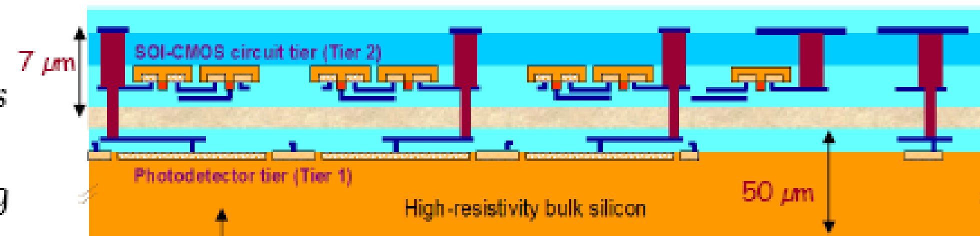
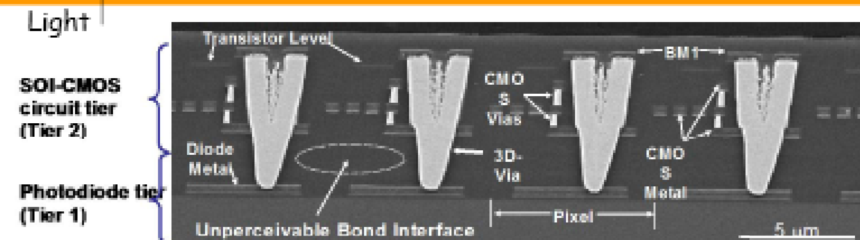
R&D at MIT Lincoln Lab

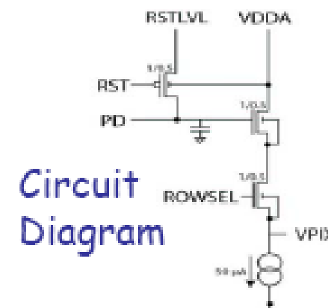
3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p⁺n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 - 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array





Drawing and SEM Cross section



Circuit Diagram

Image

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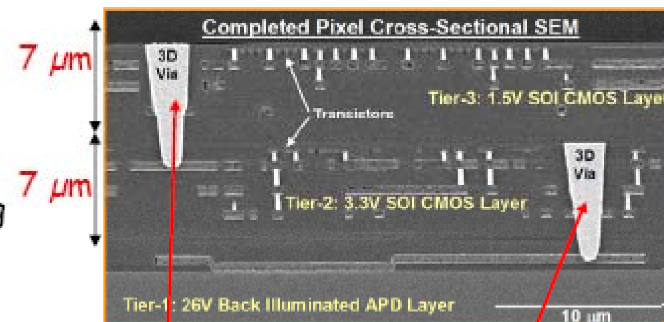
R&D at MIT Lincoln Lab

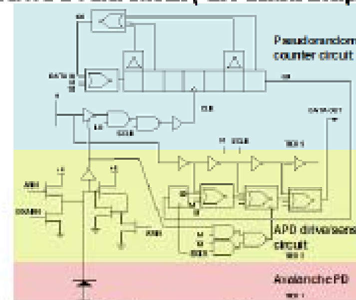
3D Laser Radar Imager

- 64 x 64 array, 30 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel

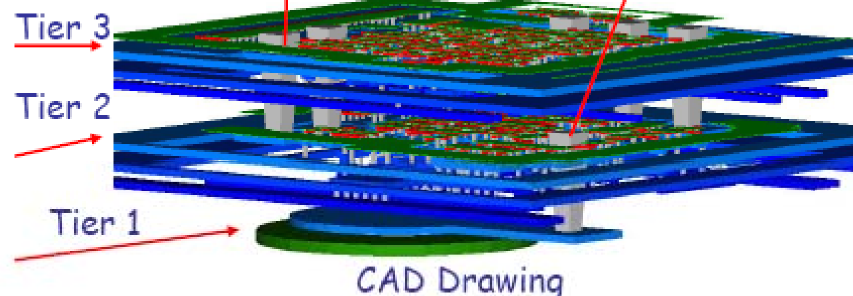


SEM Cross section

VISA APD Pixel Circuit (~250 transistors/pixel)



Schematic



CAD Drawing

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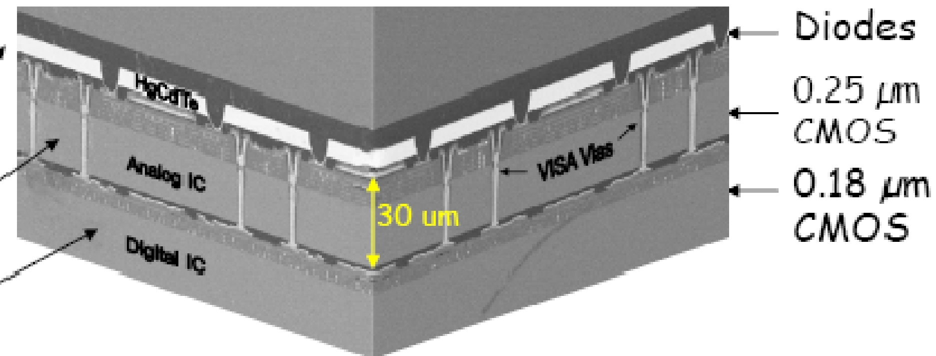
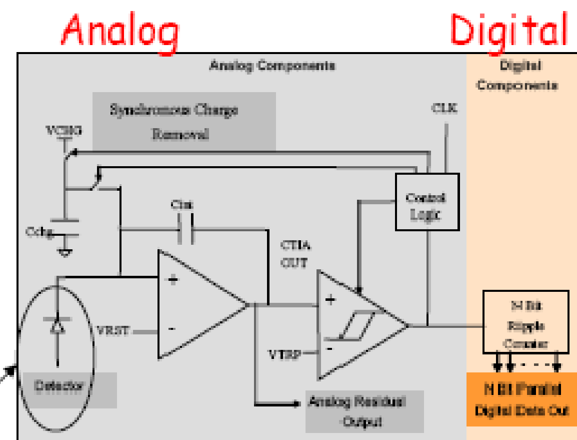
R&D at MIT Lincoln Lab

3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section



3 Tier circuit diagram

Infrared image