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UNIVERSITY of GLASGOW

Simulation results from double-sided and standard 3D detectors

David Pennicard, University of Glasgow Celeste Fleta, Chris Parkes, Richard Bates – University of Glasgow G. Pellegrini, M. Lozano - CNM, Barcelona

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Overview

- Simulations of different 3D detectors in ISE-TCAD
 - Comparison of double-sided 3D and full-3D detectors before irradiation
 - Radiation damage models
 - Preliminary results of radiation damage modelling

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Double-sided 3D detectors

- Proposed by CNM, also being produced by IRST
- Columns etched from opposite sides of the substrate
- Metal layer on back surface connects bias columns
 - Backside biasing
- Medipix configuration (55µm pitch) and 300µm thickness



Double-sided 3D: Depletion behaviour

- ~2V lateral depletion (same as standard 3D)
- ~8V to deplete to back surface of device



Double-sided 3D: Electric field



Double-sided 3D: Electric field at front



Double-sided 3D detectors: Collection time

Simulated particle track passing midway between n+ and p+ columns



Variation in charge collection time with choice of device structure

| Detector | Column length | 90% collection | 99% collection |
|-----------------|---------------|----------------|----------------|
| Double-sided 3D | 250µm | 0.75ns | 2.5ns |
| Double-sided 3D | 270µm | 0.40ns | 1.0ns |
| Double-sided 3D | 290µm | 0.35ns | 0.5ns |
| Standard 3D | 300µm | 0.35ns | 0.5ns |

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University of Perugia trap models

IEEE Trans. Nucl. Sci., vol. 53, pp. 2971–2976, 2006 "Numerical Simulation of Radiation Damage Effects in p-Type and n-Type FZ Silicon Detectors", M. Petasecca, F. Moscatelli, D. Passeri, and G. U. Pignatel



- 2 Acceptor levels: Close to midgap
 - Leakage current, negative charge (N_{eff}) , trapping of free electrons
- Donor level: Further from midgap
 - Trapping of free holes

University of Perugia trap models

- Aspects of model:
 - Leakage current reasonably close to $\alpha = 4.0*10^{-17}$ A/cm
 - Depletion voltage matched to experimental results (M. Lozano et al., IEEE Trans. Nucl. Sci., vol. 52, pp. 1468–1473, 2005)
 - Carrier trapping -
 - Model reproduces CCE tests of $300\mu m$ pad detectors
 - *But* trapping times don't match experimental results

$$\frac{\partial n}{\partial t} = \frac{n}{\tau_e} \qquad \frac{1}{\tau_e} = \beta_e \Phi_{eq} \qquad \frac{1}{\tau_e} = v_{th}^e \sigma_e N \qquad \text{and experiment} \\ = v_{th}^e \sigma_e \Phi_{eq} \eta \qquad \beta_e = v_{th}^e \sigma_e \eta$$

Link between model

 Experimental trapping times for p-type silicon (V. Cindro et al., IEEE NSS, Nov 2006) up to 10¹⁵n_{eq}/cm²

$$- \beta_{e} = 4.0^{*}10^{-7} \text{cm}^{2}\text{s}^{-1} \qquad \beta_{h} = 4.4^{*}10^{-7} \text{cm}^{2}\text{s}^{-1}$$

- Calculated values from p-type trap model
 - $\beta_e = 1.6^* 10^{-7} cm^2 s^{-1} \qquad \beta_h = 3.5^* 10^{-8} cm^2 s^{-1}$

Altering the trap models

- Priorities: Trapping time and depletion behaviour
 - Leakage current should just be "sensible": $\alpha = 2-10 \times 10^{-17}$ A/cm
- Chose to alter cross-sections, while keeping σ_h/σ_e constant
- Carrier trapping: $\beta_{e,h}$ =

$$\beta_{e,h} = v_{th}^{e,h} \sigma_{e,h} \eta$$

Space charge:

$$n_{e,Trap} = N_{trap} f_n \approx N_{trap} \exp\left(\frac{-E_t}{kT}\right) \left(\frac{n}{n_i} + \frac{\sigma_h v_{th}^{\ h}}{\sigma_e v_{th}^{\ e}} \exp\left[\frac{-E_t}{kT}\right]\right)$$

Modified P-type model

| Туре | Energy (eV) | Trap | σ_{e} (cm ²) | $\sigma_{\rm h}$ (cm ²) | η (cm ⁻¹) |
|----------|----------------|------|---------------------------------|-------------------------------------|--------------------------|
| Acceptor | Ec-0.42 | VV | 9.5*10 ⁻¹⁵ | 9.5*10 ⁻¹⁴ | 1.613 |
| Acceptor | Ec-0.46 | VVV | 5.0*10 ⁻¹⁵ | 5.0*10 ⁻¹⁴ | 0.9 |
| Donor | Ec+0.36 | CiOi | 3.23*10 ⁻¹³ | 3.23*10 ⁻¹⁴ | 0.9 |

Modified P-type model and experimental data

| Туре | Energy (eV) | Trap | σ _e (cm²) | σ _h (cm²) | η (cm ⁻¹) |
|----------|----------------|------|------------------------|------------------------|--------------------------|
| Acceptor | Ec-0.42 | VV | 9.5*10 ⁻¹⁵ | 9.5*10 ⁻¹⁴ | 1.613 |
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P-type trap models: Depletion voltages

P-type trap model: Leakage Current



Perugia N-type model

Perugia N-type model (FZ)

| Туре | Energy (eV) | Trap | $\sigma_{e}^{}$ (cm ²) | $\sigma_{\rm h}~(cm^2)$ | η (cm ⁻¹) |
|----------|----------------|------|------------------------------------|-------------------------|--------------------------|
| Acceptor | Ec-0.42 | VV | 2.0*10 ⁻¹⁵ | 1.2*10 ⁻¹⁴ | 13 |
| Acceptor | Ec-0.50 | VVO | 5.0*10 ⁻¹⁵ | 3.5*10 ⁻¹⁴ | 0.08 |
| Donor | Ec+0.36 | CiOi | 2.0*10 ⁻¹⁸ | 2.5*10 ⁻¹⁵ | 1.1 |

Donor removal

 $N_D = N_{D0} \exp(-c_D \Phi)$

$$N_{D0} * c_D = K_C = const$$

$$K_C = (2.2 \pm 0.2) \times 10^{-2} \text{ cm}^{-1}$$

- Works similarly to the p-type model
- Donor removal is modelled by altering the substrate doping directly
- Experimental trapping times for n-type silicon (G. Kramberger et al., NIMA, vol. 481, pp297-305, 2002)

$$- \beta_{e} = 4.0^{*}10^{-7} \text{cm}^{2}\text{s}^{-1} \qquad \beta_{h} = 5.3^{*}10^{-7} \text{cm}^{2}\text{s}^{-1}$$

• Calculated values from n-type trap model

 $- \beta_e = 5.3^* 10^{-7} \text{cm}^2 \text{s}^{-1} \qquad \beta_h = 4.5^* 10^{-8} \text{cm}^2 \text{s}^{-1}$

Modified N-type model

| Туре | Energy (eV) | Trap | $\sigma_{e}^{}$ (cm ²) | σ_{h} (cm ²) | η (cm⁻¹) |
|----------|----------------|------|------------------------------------|---------------------------------|-------------|
| Acceptor | Ec-0.42 | VV | 1.5*10 ⁻¹⁵ | 0.9*10 ⁻¹⁴ | 13 |
| Acceptor | Ec-0.5 | VVO | 5.0*10 ⁻¹⁵ | 3.5*10 ⁻¹⁴ | 0.08 |
| Donor | Ec+0.36 | CiOi | 2.5*10 ⁻¹⁷ | 3.1*10 ⁻¹⁵ | 1.1 |

N-type trap models: Depletion voltages

N-type trap model: Leakage Current



Bug in ISE-TCAD version 7

- Currently using Dessis, in ISE-TCAD v7 (2001)
- Non time-dependent simulations with trapping are OK
- Error occurs in transient simulations with traps
 - Carrier behaviour in depletion region is OK
 - Displacement current is miscalculated
 - This affects currents at the electrodes



Correct behaviour:
$$\nabla .\underline{J}_{tot} = \nabla .\underline{J}_{disp} + \nabla .\underline{J}_n + \nabla .\underline{J}_p = 0$$

Error: $\nabla .\underline{J}_{disp,error} = \nabla .\underline{J}_{tot} = q(R_{e,Trap} - R_{h,Trap}) * (\sim)1.73$

- This bug is not present in the latest release of **Synopsis TCAD** (2007)
 - Synopsis bought ISE TCAD, and renamed Dessis as "Sentaurus Device"
 - Don't know which specific release fixed the problem

Test of charge trapping in Synopsis TCAD

• Simulated a simple diode with carriers generated at its midpoint



Test of charge trapping in Synopsis TCAD

- Simulated a simple diode with carriers generated at its midpoint
- Acceptor and donor traps *further from the midgap*
 - Produces charge trapping but little change in N_{eff}
 - Trap levels should give $\tau_e{\approx}\,\tau_h{\approx}\,1ns$



Test of charge trapping in Synopsis TCAD

- Simulated a simple diode with carriers generated at its midpoint
- Acceptor and donor traps *further from the midgap*
 - Produces charge trapping but little change in N_{eff}
 - Trap levels should give $\tau_e{\approx}\,\tau_h{\approx}\,1ns$



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Full 3D – Depletion voltage (p-type)

- Depletion voltage is low, but strongly dependent on pitch
- Double sided 3D shows the same lateral depletion voltage as full 3D



Full 3D – electric field at 100V

Full depletion is achieved well under 100V, but electric field is altered



Double-sided 3D – front surface

Once again, double-sided devices show different behaviour at front and back surfaces



Double-sided 3D – back surface

Region at back surface depletes more slowly – not fully depleted at 100V bias



Further work

- Simulate charge collection!
- Consider effects of different available pixel layouts
 - CCE, depletion voltage, insensitive area, capacitance



Conclusions

- Double-sided 3D detectors:
 - Behaviour mostly similar to standard 3D
 - Depletion to back surface requires a higher bias
 - Front and back surfaces show slower charge collection
- Radiation damage model
 - Trap behaviour is directly simulated in ISE-TCAD
 - Trap models based on Perugia models, altered to match experimental trapping times
- Preliminary tests of damage model with 3D
 - Relatively low depletion voltages, but electric field pattern is altered
 - Double-sided 3D shows undepleted region at back surface at high fluences

Thank you for listening

Additional slides

3D detectors

- N+ and p+ columns pass through substrate
- Fast charge collection
- Low depletion voltage
- Low charge sharing
- Additional processing (DRIE for hole etching)





Breakdown in double-sided 3D

- Breakdown occurs at column tips around 230V
 - Dependent on shape, e.g. 185V for square columns

Electric field (V/cm) around tip of p+ column at 215V



Breakdown in double-sided 3D

• With 10¹²cm⁻² charge, breakdown at 210V



Example of ISE TCAD bug

Current distribution after 0.06ns



Example of ISE TCAD bug

Current distribution after 1ns



Example of ISE TCAD bug



3D is radiation hard: Tests with baby-Atlas sensors C. DaVia. J. Hasi, 5 Watts, (Brunel/W

C. DaVia. J. Hasi, S Watts, (Brunel/Manchester),V. Linhart, T. Slavicheck, T Horadzof, S. Pospisil (Technical University, Praha), C. Kenney (MBC), S. Parker (Hawaii/LBL)



■ Volume = 1.2 x 1.33 x 0.23 mm³

- 3 electrode Atlas pixel geometry 71 μm IES
- n-electrode readout
- n-type before irradiation -12 kΩ cm
- Irradiated with reactor neutrons (Praha)



Full 3D – Depletion voltage (p-type)

- Depletion voltage is low, but strongly dependent on pitch
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Weighting fields and electrode layouts



Symmetrical layout of n+ and p+

Weighting potential is the same for electrons and holes

Square layout, symmetrical layout of n+ and p+

Square layout, symmetrical layout of p+ and n+

0

10

20

30

40

50

0

5

≻



Weighting fields and electrode layouts



3 bias columns per readout column Weighing potential favours electron collection



Square layout, 3 p+ bias columns per n+ readout column

Future work – Design choices with 3D

- Choice of electrode layout:
 - In general, two main layouts possible



- Second option doubles number of columns
- However, increasing no. of p+ columns means larger electron signal

Future work – Design choices with 3D

- ATLAS pixel (400μm * 50μm) allows a variety of layouts
 - No of n+ electrodes per pixel could vary from ~3-8
 - Have to consider V_{dep}, speed, total column area, capacitance
 - FP420 / ATLAS run at Stanford already has different layouts
- CMS (100 μm * 150μm)

