Implementation of triggered readout mode of VMM3a in RD51 SRS

- Test beam showed that high electronics threshold is necessary with VMM's self-triggered mode
  → High electronics THL leads to high gain operation of detectors to reach full efficiency
- Various expressions of interest from the community for externally triggered mode
  → Collaborative effort to implement it in the SRS
  → Goal today: who can contribute to this development (and maybe how do we organise it)
- Points where help is needed:
  - **Firmware:** the triggered mode needs to be implemented in the SRS firmware (both **hybrid and FEC**)
  - Software: some modifications in the slow control and the reconstruction software are necessary
  - Testing of implementation in the lab from groups that have hardware available
- Different approaches to implement the triggered mode in the firmware:
  https://indico.cern.ch/event/1228120/attachments/2561987/4416074/VMM_ExTrgPlan_Shihai.pdf
- Firmware available here (login and access right needed):
  - https://gitlab.cern.ch/rd51-slow-control/vmm3a-hybrid-firmware
  - https://gitlab.cern.ch/rd51-slow-control/srs-vmm3a-fec
  - Access will be granted to interested developers