CMS Phase-2 Inner Tracker Pixel Chip Prototype Tests

Marijus Ambrozas, on behalf of the CMS Tracker group

Faculty of Physics, Vilnius University

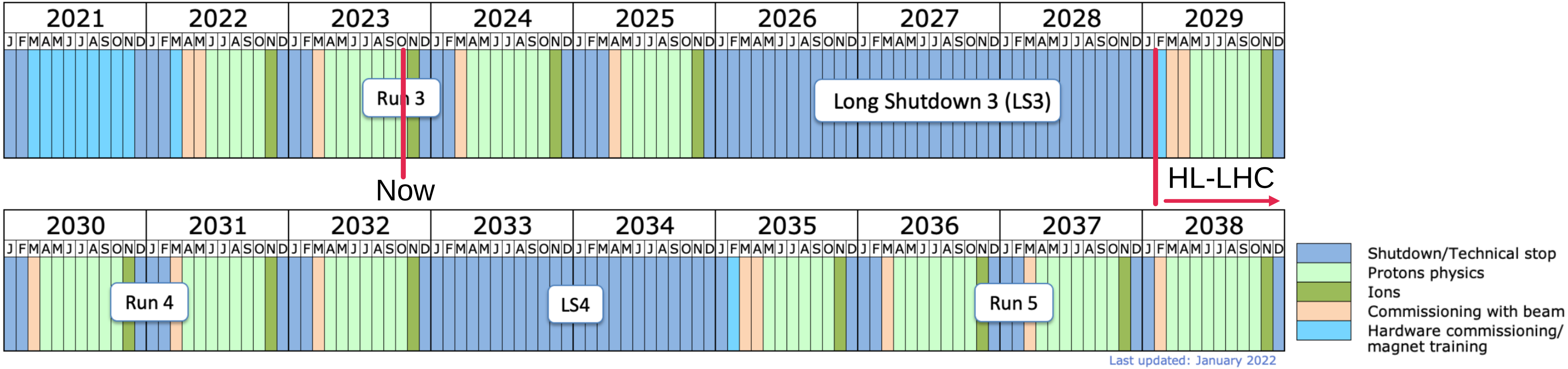
marijus.ambrozas@cern.ch

Fizikos fakultetas

CERN Baltic Conference 2023, Riga
2023-10-10

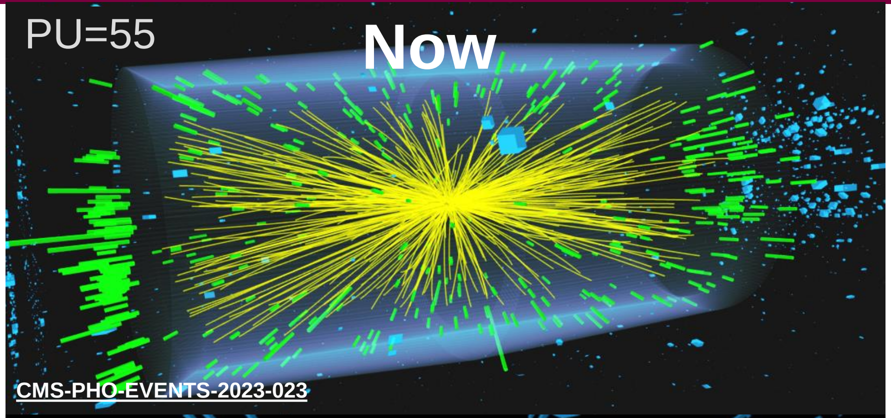
HL-LHC upgrade

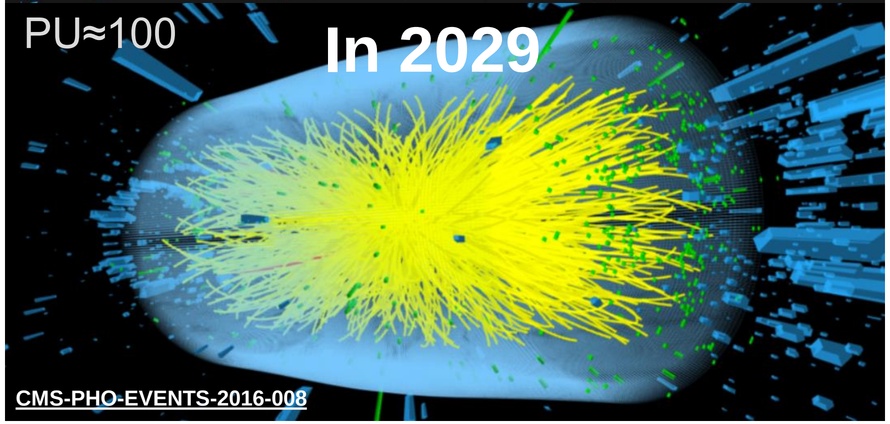
- The High Luminosity LHC is expected to launch at 2029
- Great discovery potential improvement:
  - Proton-proton collision energy: 14 TeV
  - Peak instantaneous luminosity:
    LHC nominal **1×**10^{34} $cm^{-2}s^{-1}$ → LHC current ~**2.1×**10^{34} $cm^{-2}s^{-1}$ → HL-LHC **7.5×**10^{34} $cm^{-2}s^{-1}$
  - Integrated luminosity: LHC nominal ~**300** fb^{-1} → HL-LHC ~**3000** fb^{-1} over 10 years
  - Average pile-up: LHC nominal **25** → LHC current ~**60** → HL-LHC **200**

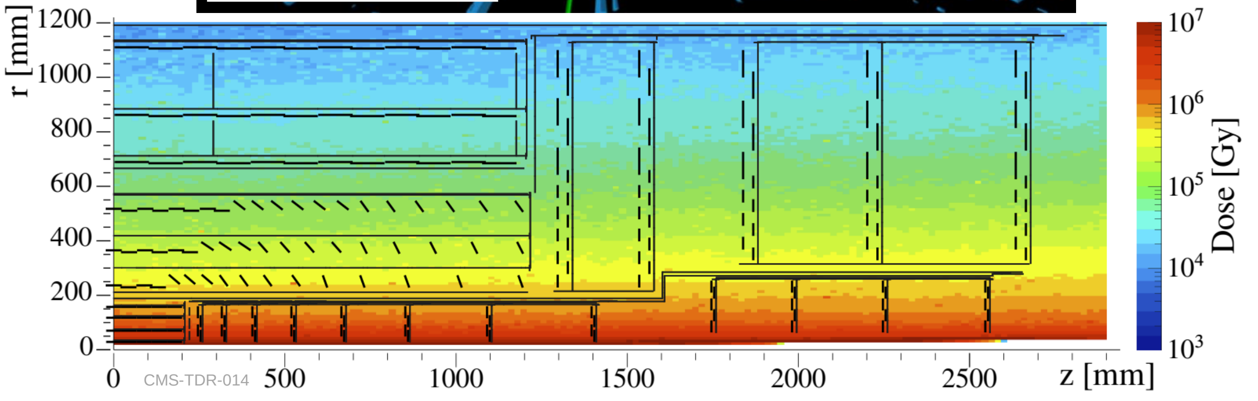


Detector requirements for HL-LHC

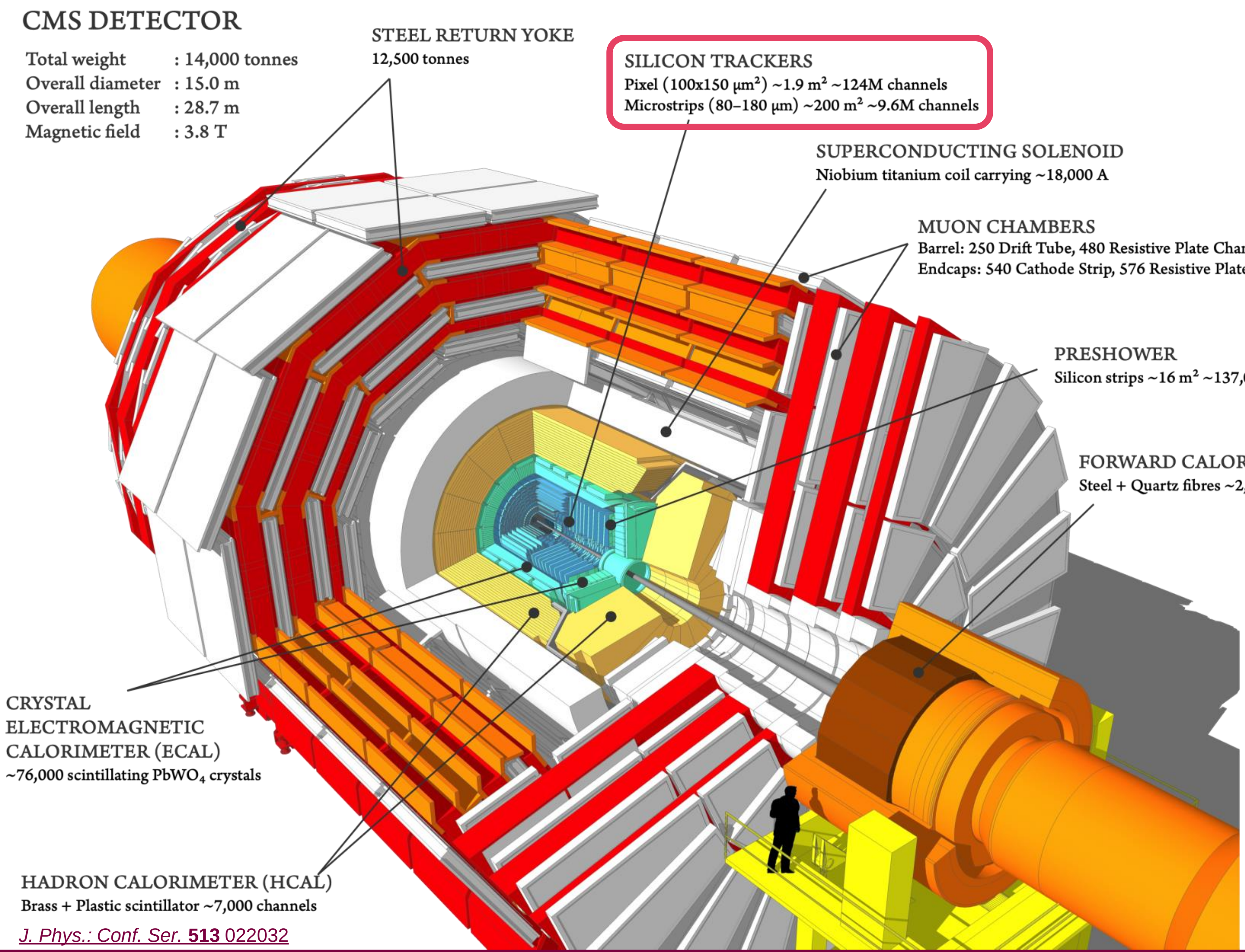
- More collisions will also bring challenges:
  - ~3× more tracks than currently
    → higher trigger rates
    → higher data rates
    → harder to separate tracks
    → bigger radiation doses (up to 1.2 Grad)
- Requirements for the Phase-2 CMS tracker:
  - High granularity
  - High radiation tolerance
  - Contribution to level-1 trigger
  - Extended acceptance range
  - Reduced material budget
- This makes the current CMS tracker not suitable for operation after the HL-LHC upgrade
  - A completely new tracker is in preparation







Current CMS tracker

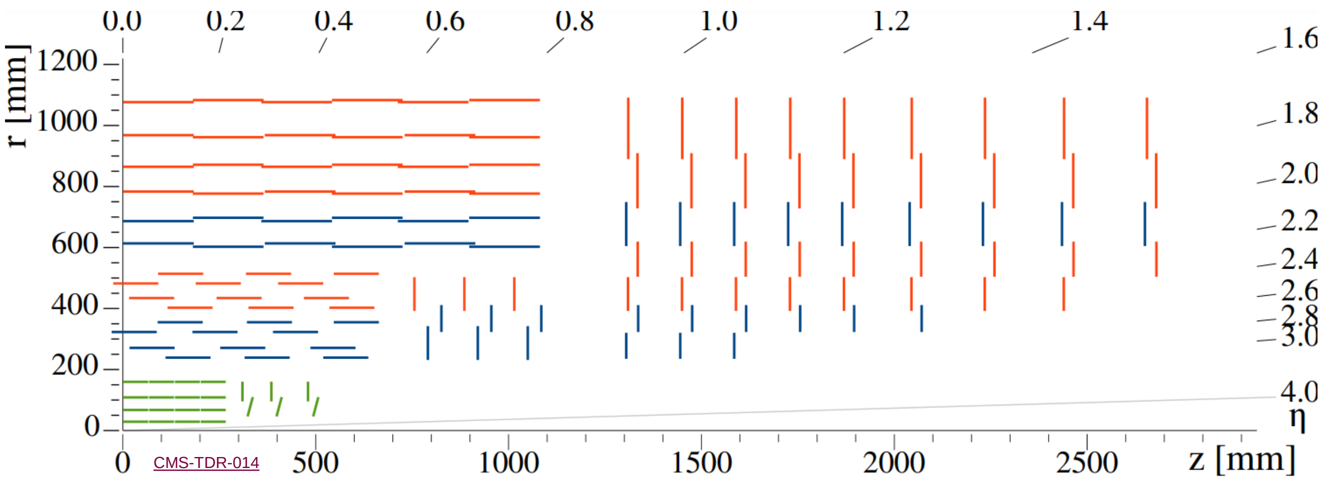


J. Phys.: Conf. Ser. **513** 022032

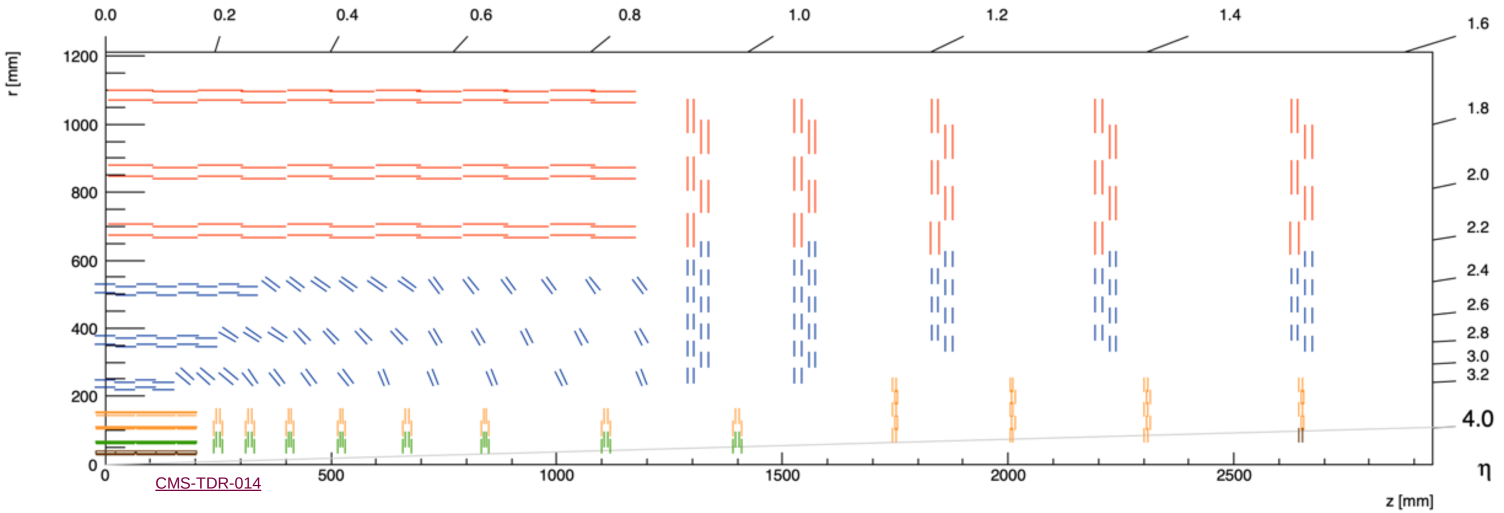
Phase-2 CMS tracker upgrade

- Both CMS Inner and Outer Tracker systems will be completely replaced
- Phase-2 Outer Tracker:
  - 6 barrel layers and 5 endcap disks per side
  - Micro-strip and macro-pixel silicon sensors
  - Contribution to the L1 trigger
- Phase-2 Inner Tracker:
  - 4 barrel layers and 12 endcap/forward disks (instead of the current 3 disks)
  - 25×100 μm^2 silicon pixel sensors with both 3D and planar technologies
  - Tracking acceptance: up to |η| = 4.0 (instead of the current |η| < 3.0)

Current tracker

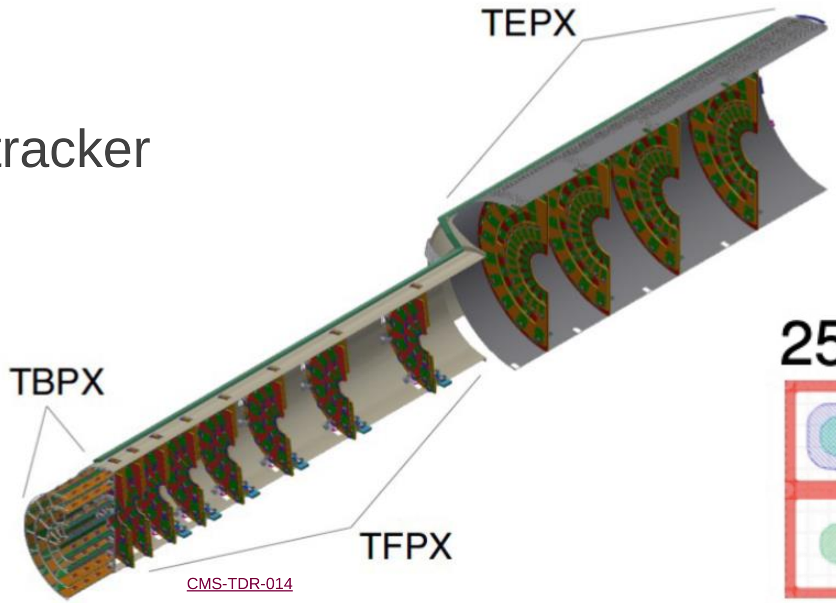


Phase-2 tracker

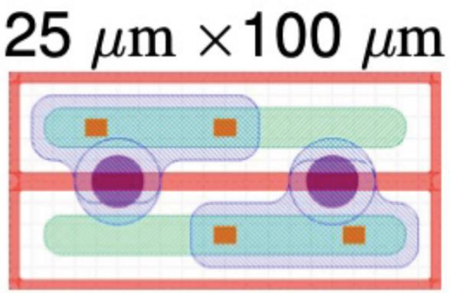


Phase-2 Inner Tracker

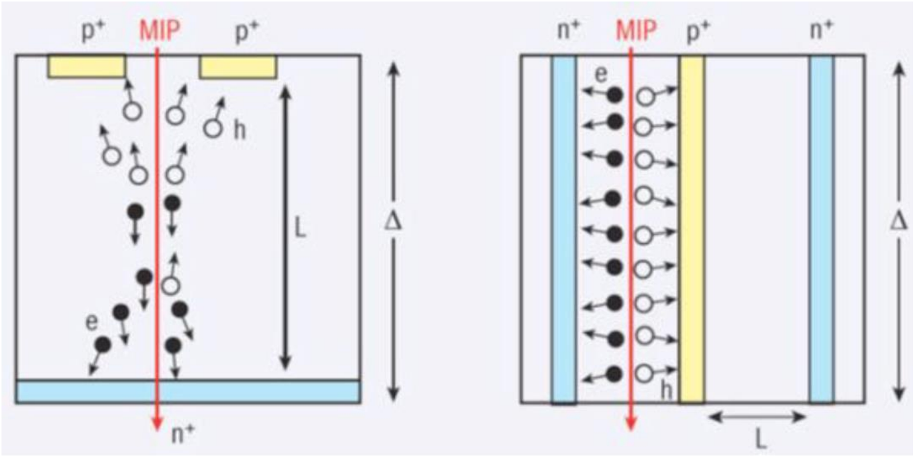
- 6× smaller pixels compared with the current tracker
  - 25×100 μm^2
  - 150 μm active thickness
- Total active surface area ~4.9 m^2
- Total pixel count ~2 billion
- Two different pixel technologies
  - 3D pixel sensors on barrel layer 1
  - n-in-p planar sensors everywhere else
- A readout chip based on 64 nm CMOS technology is developed by RD53 collaboration
  - RD53 is developing chips for both CMS and ATLAS with different features



CMS-TDR-014



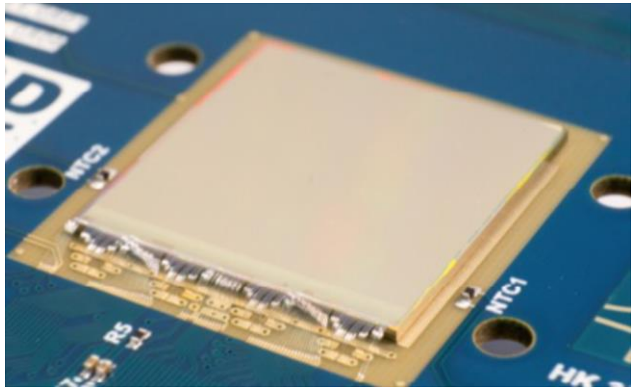
CMS-TDR-014

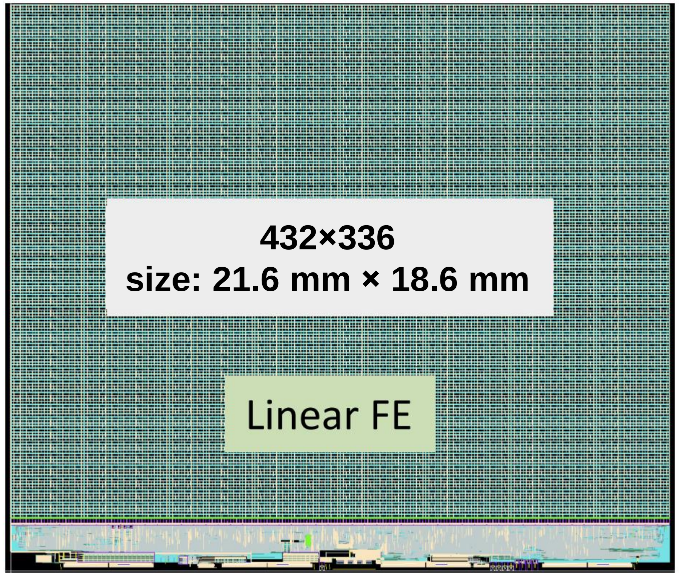


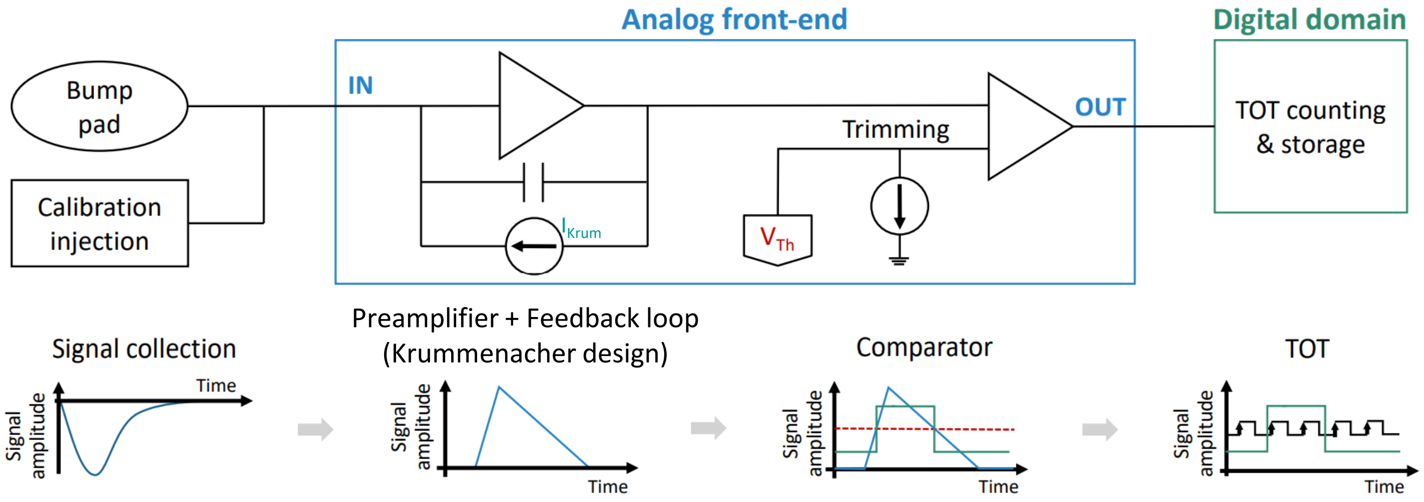
https://cerncourier.com/a/silicon-sensors-go-3d/

The CMS ReadOut Chip

- Features of the chip under development:
  - Able to withstand the radiation up to 1 Grad
  - Low power consumption of < 1 W/cm^2
  - Compatible with serial powering by using on-chip shunt-LDO regulators
- Pre-production prototypes (RD53B) are undergoing many different tests
- The RD53B version for CMS is called CMS ReadOut Chip – CROC_v1
  - 432×336 channels
  - Bump-bonded to the sensor
  - Wire-bonded to the readout
  - Linear analog front-end architecture
  - 4-bit digital readout for signal strength (ToT)
    - Single- or double-slope operation possible





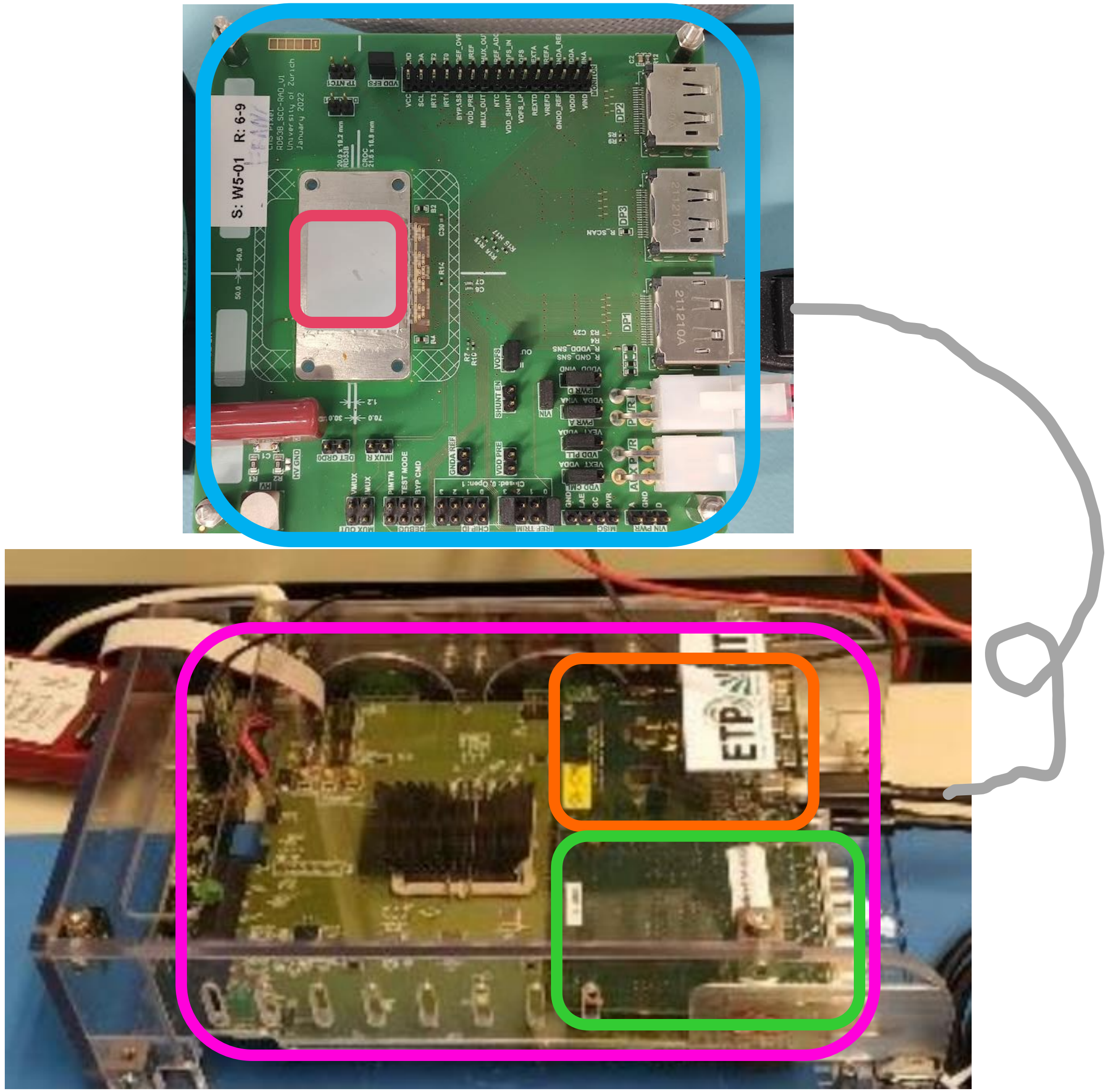


arXiv:2105.00070

Test setup

Our test setup for CROC chips consists of:

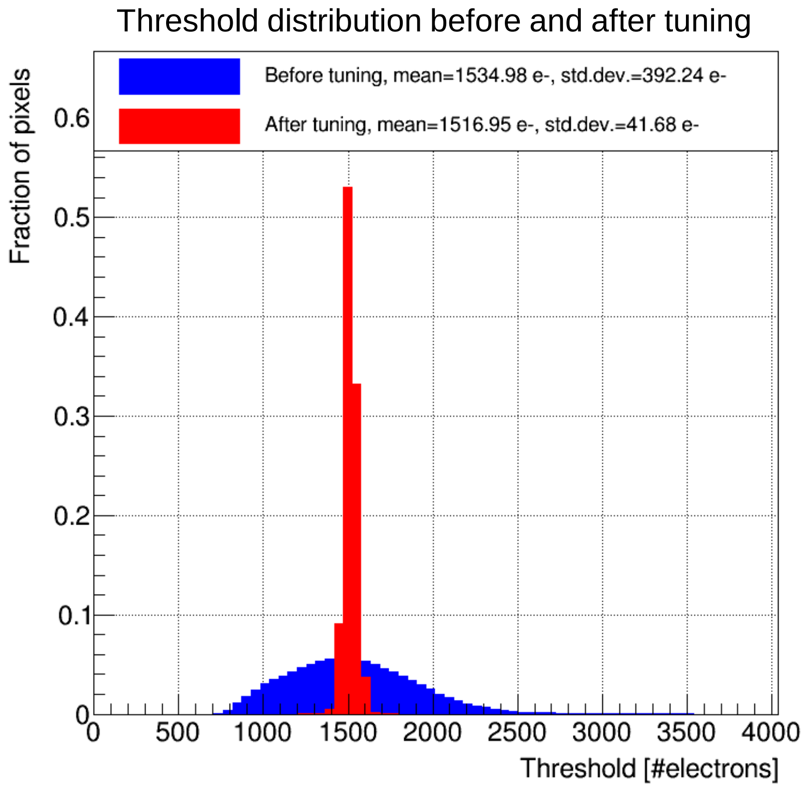
- Custom-made equipment:
  - CROC chip with sensor mounted on a Single Chip Card (SCC)
  - Electrical readout FMC board connected to SCC via DP connection
  - FC7 board with FPGA and 2 FMC connectors
- Standard equipment:
  - DIO5 FMC board (provides external trigger, clock, etc.)
  - Low and high voltage supply
  - Computer connected to the FC7 via IPbus
    - IPbus is a protocol used to communicate between software and firmware via ethernet (https://ipbus.web.cern.ch/)
    - Computer runs the Ph2-ACF software which is designed to perform both Inner and Outer Tracker hardware tests

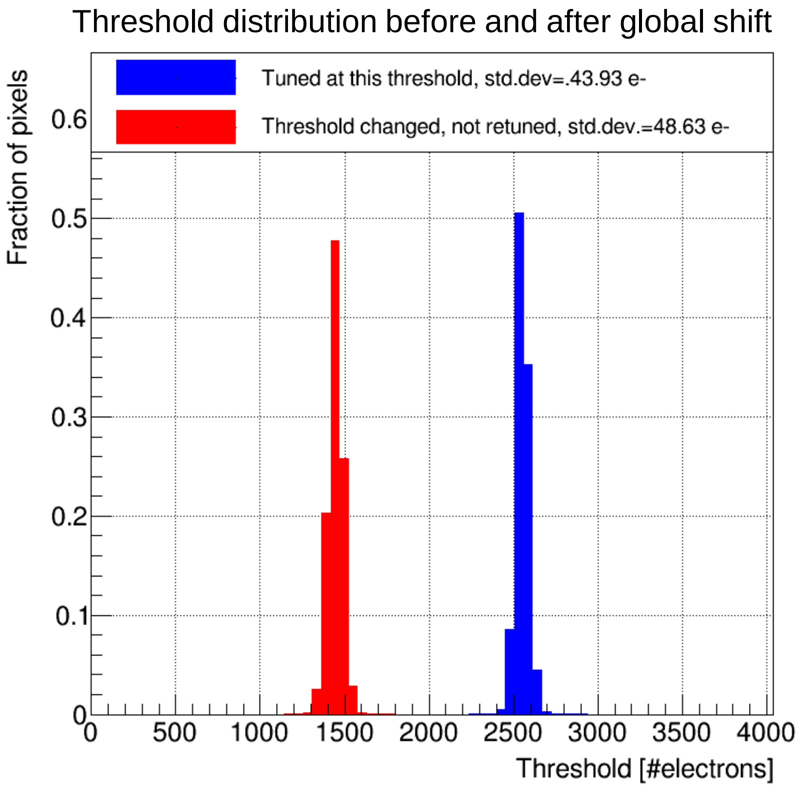


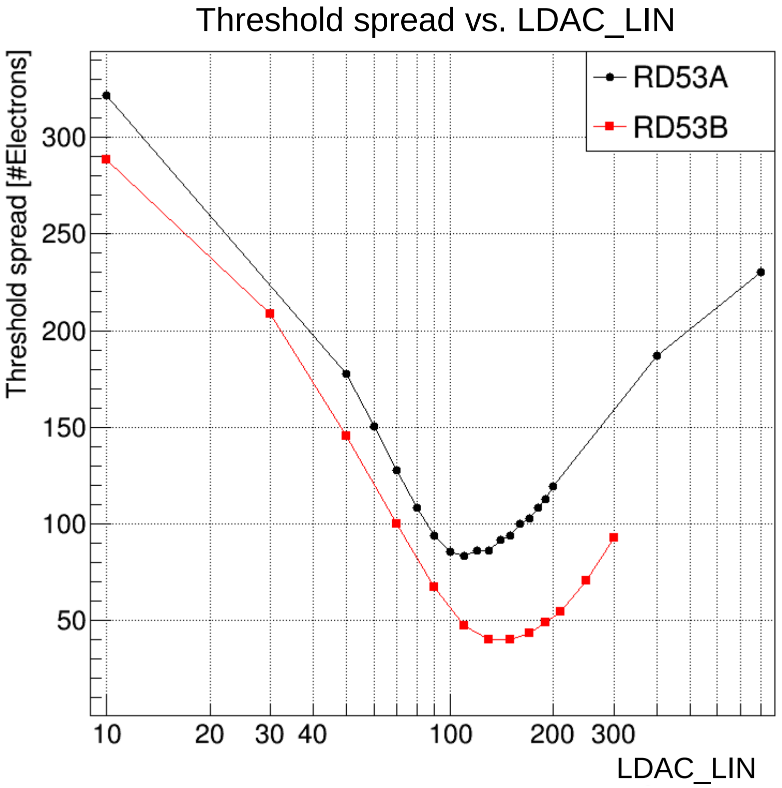
Hit detection threshold tuning

- A hit is registered once the voltage from the preamplifier surpasses the voltage threshold
- Threshold can be tuned globally but varies from pixel-to-pixel due to transistor mismatch
- Each pixel has a dedicated trimming DAC (TDAC, 5 bits) to reduce the threshold variation betwen pixels
  - The trimming DAC strength is controlled by a global DAC (called LDAC_LIN)

- The threshold CROC chip can be successfully tuned with a threshold spread of only ~50 e⁻ between the pixels
  - This is 2× better than the RD53A demonstrator chip
- The threshold spread stays stable after global threshold shift
  - Relevant for real experiment conditions
- This was confirmed with multiple chips



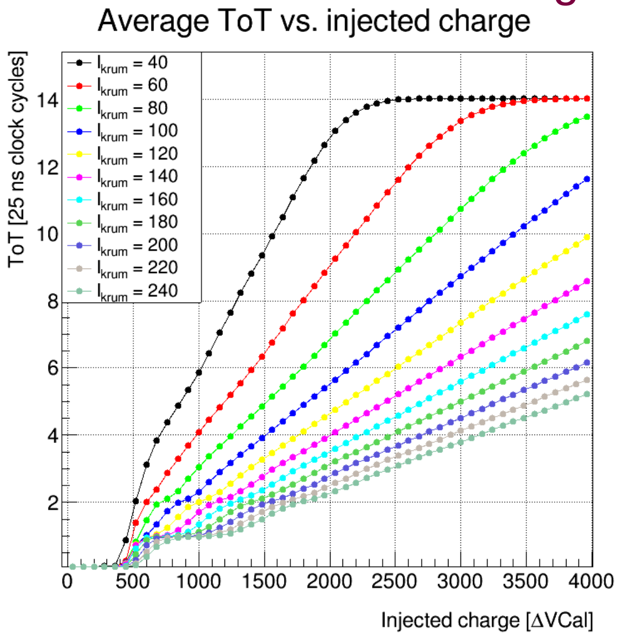


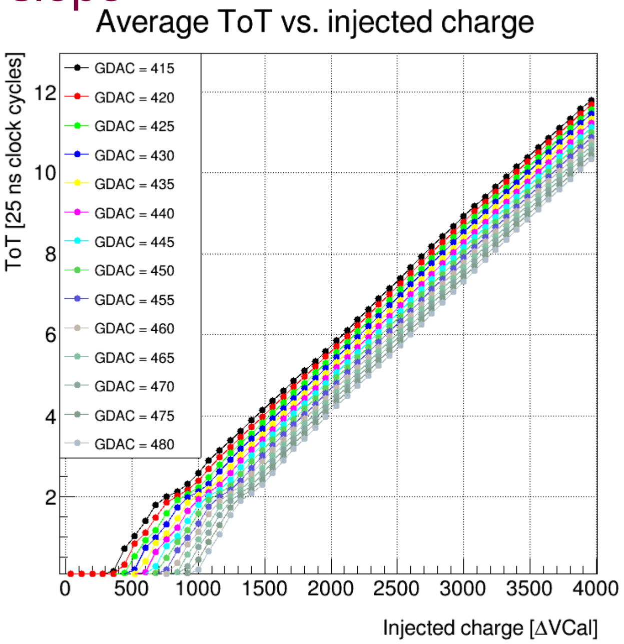


ToT gain tuning

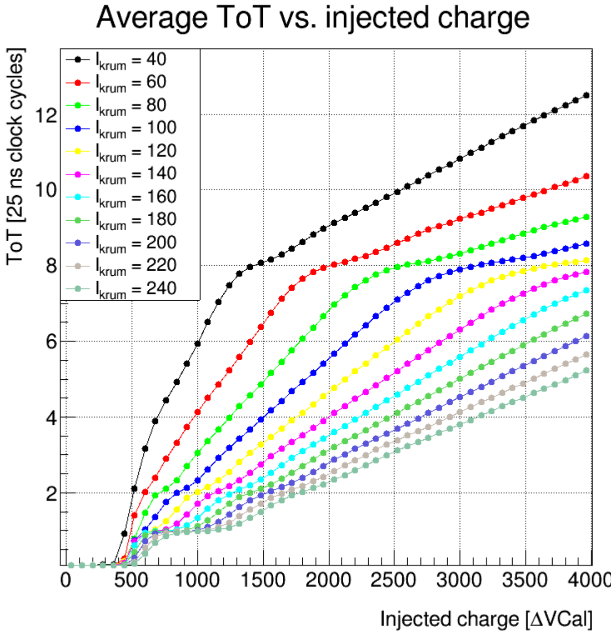
- The signal strength is measured by the time the preamplifier output voltage stays above the comparator threshold
  - Time Over Threshold (ToT) is measured in 25 ns intervals
  - 4 bits, single or dual slope modes available
- Preamplifier feedback (“Krummenacher”) current can be tuned to obtain different ToT gain curves
  - Enables choosing a sweetspot for signal resolution and dynamic range
- ToT gain slope has non-linearities for signal values close to the threshold and becomes linear at higher signal strength
- ToT gain slope does not depend on the threshold itself, as expected with the linear analog front-end

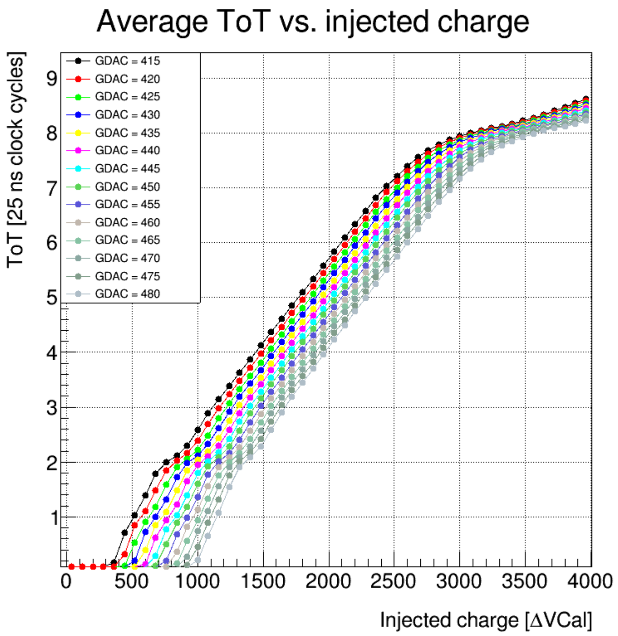
Single slope



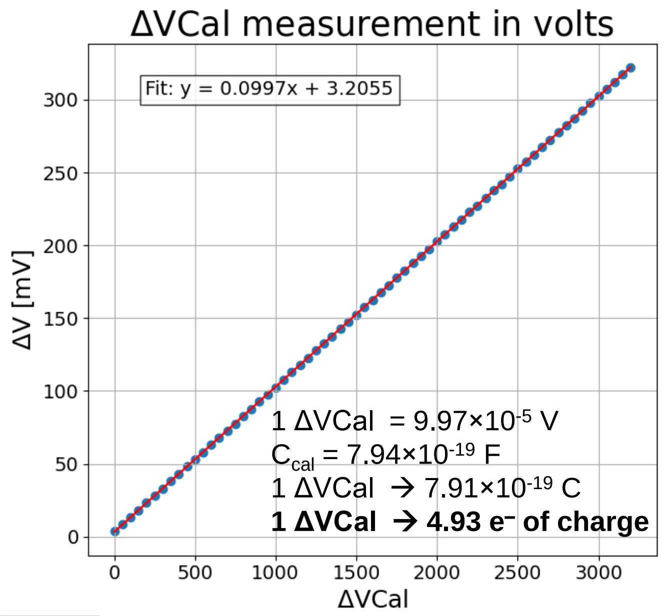


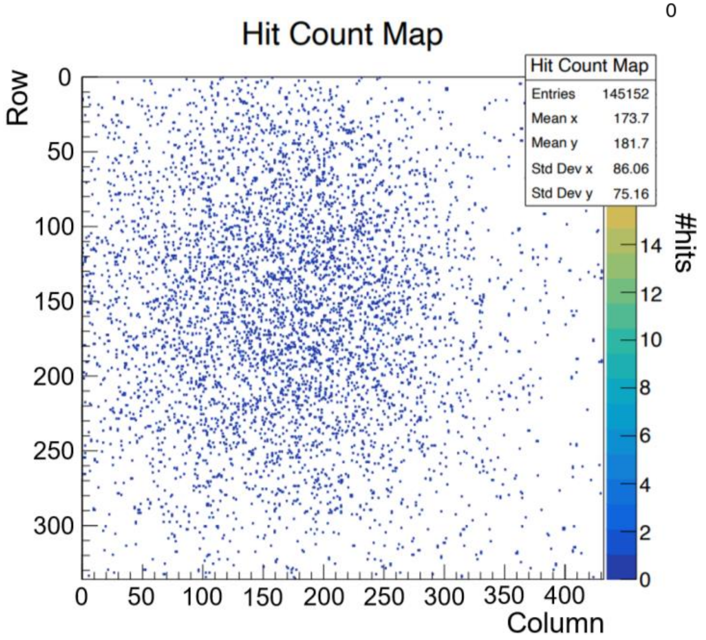
Dual slope (6-to-4 bit compression)

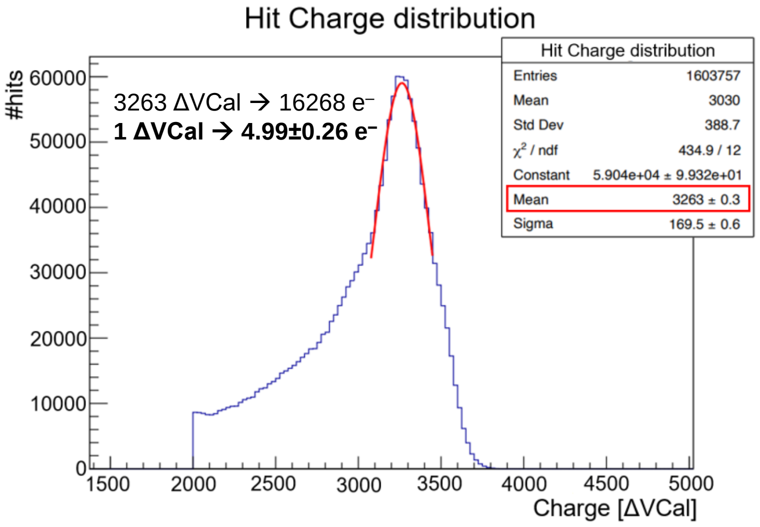




- Threshold is measured using a calibration circuit
- Calibration pulse strength is controlled by DAC units (ΔVCal)
- We have used the internal voltage multiplexer to measure the physical ΔVCal value
- The resultant ΔVCal value corresponds ~5 e^- of signal, confirmed with multiple chips
- The threshold unit value of ~5 e^- was also confirmed by using ^{241}Am x-ray source
  - X-rays are monochromatic (59.54 keV) and always release the same amount of signal in the sensor (16268 e^-)







Wrap-up

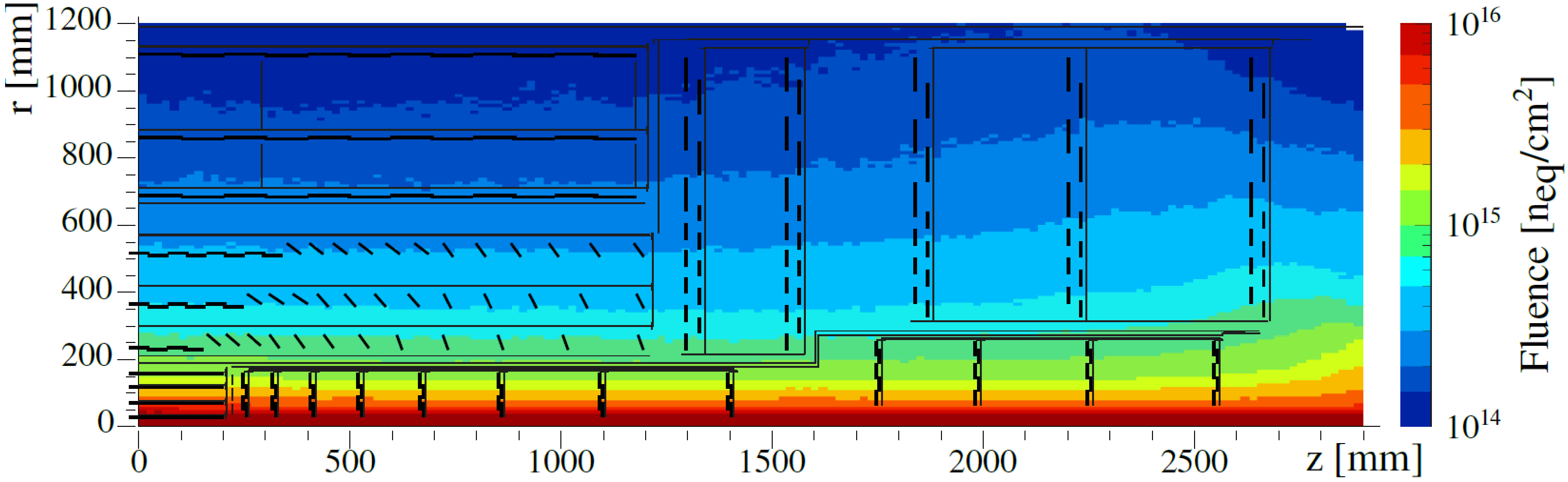
- The HL-LHC upgrade comes in 2029 and brings a big challenge for detector builders but provides big physics opportunities
- The Phase-2 detectors must have higher resolution, higher data output rates, and higher radiation tolerance than the current ones
- A completely new tracker is in preparation prepared for CMS
- Pixel detector chips for the Inner Tracker are developed by the CERN/RD53 collaboration
- Pre-production chips CROC_v1, are still tested extensively and show good performance

Thank you!

Backup

Particle fluence in 1 MeV neutron equivalent

Integrated particle fluence in 1MeV neutron equivalent per cm2, for the Phase-2 tracker. The estimates shown correspond to a total integrated luminosity of 3000 fb^{-1} of pp collisions at 14 TeV.



Outer Tracker contribution to L1 trigger

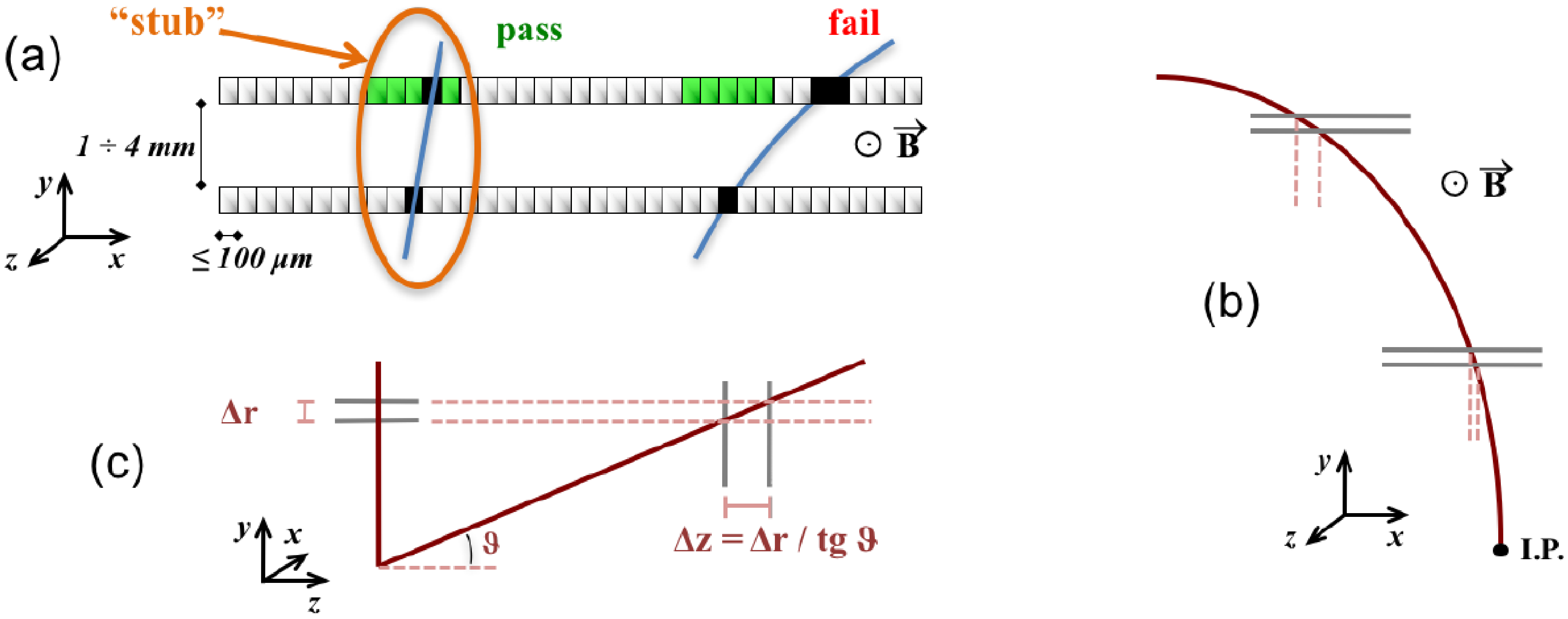


Figure 2.5: Illustration of the p_T module concept. (a) Correlation of signals in closely-spaced sensors enables rejection of low-p_T particles; the channels shown in green represent the selection window to define an accepted stub. (b) The same transverse momentum corresponds to a larger distance between the two signals at large radii for a given sensor spacing. (c) For the end-cap discs, a larger spacing between the sensors is needed to achieve the same discriminating power as in the barrel at the same radius.