Review of the first RD50-HVCMOS Testbeam at CERN SPS

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This contribution reviews the testbeam results of the RD50-MPW3 chip presented at the last workshop. Detailed analysis results are presented and discussed.

The measured efficiency is far beyond expectations, thus; an extensive analog chip-simulation study has been carried out to find the reason. These simulations as well as their outcome are discussed.

In the end, changes in the design for the next prototype Chip, RD50-MPW4 are listed and an update about the submission status as well as future plans are given.