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A real-time demonstrator of track reconstruction with FPGAs at LHCb

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The upgraded LHCb detector has started its Run 3 of data taking in 2022, with a completely overhauled DAQ system, reading out and processing the full detector data at every LHC bunch crossing (30 MHz average rate). At the same, an intense R&D activity is taking place, with the aim of further improving the real-time data processing performance of LHCb, in view of a further luminosity upgrade of the experiment ("Upgrade II").
In this work, we describe the experience gained with a prototype device for a 30 MHz real-time tracking in the LHCb VELO detector, implemented in state-of-art PCIe-hosted FPGA cards interconnected by fast optical links.
The system is capable of processing live LHCb data opportunistically during physics data taking, thanks to a dedicated testbed facility fed by the experiment monitoring system. We describe, amongst other things, the system used to organize and optimize the high-speed distribution of data to the components, and the synchronization with the most updated alignment constants to be used in track reconstruction.

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